PHILIPS

Data handbook

PHILIPS Electronic components and materials

Semiconductors

Part 4b November 1983

High - voltage and switching power transistors

SEMICONDUCTORS

PART 4b - NOVEMBER 1983

HIGH-VOLTAGE AND SWITCHING POWER TRANSISTORS

DATA HANDBOOK SYSTEM

Our Data Handbook System is a comprehensive source of information on electronic components, subassemblies and materials; it is made up of four series of handbooks each comprising several parts.

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The several parts contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where ratings or specifications differ from those published in the preceding edition they are pointed out by arrows. Where application information is given it is advisory and does not form part of the product specification.

If you need confirmation that the published data about any of our products are the latest available, please contact our representative. He is at your service and will be glad to answer your inquiries.

COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks is comprised of the following parts:

C1 **Assemblies for industrial use**
PLC modules, PC20 modules, HNIL FZ/30 series, NORbits 60-, 61-, 90-series, input devices, hybrid ICs

C2 **Television tuners, video modulators, surface acoustic wave filters**

C3 **Loudspeakers**

C4 **Ferroxcube potcores, square cores and cross cores**

C5 **Ferroxcube for power, audio/video and accelerators**

C6 **Electric motors and accessories**
Permanent magnet synchronous motors, stepping motors, direct current motors

C7 **Variable capacitors**

C8 **Variable mains transformers**

C9 **Piezoelectric quartz devices**
Quartz crystal units, temperature compensated crystal oscillators, compact integrated oscillators, quartz crystal cuts for temperature measurements

C10 **Connectors**

C11 **Non-linear resistors**
Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC)

C12 **Variable resistors and test switches**

C13 **Fixed resistors**

C14 **Electrolytic and solid capacitors**

C15 **Film capacitors, ceramic capacitors**

C16 **Piezoelectric ceramics, permanent magnet materials**

ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks is comprised of the following parts:

T1 Tubes for r.f. heating

T2 Transmitting tubes for communications

T3 Klystrons, travelling-wave tubes, microwave diodes

ET3 Special Quality tubes, miscellaneous devices (will not be reprinted)

T4 Magnetrons

T5 Cathode-ray tubes
Instrument tubes, monitor and display tubes, C.R. tubes for special applications

T6 Geiger-Müller tubes

T7 Gas-filled tubes
Segment indicator tubes, indicator tubes, dry reed contact units, thyratrons, industrial rectifying tubes, ignitrons, high-voltage rectifying tubes, associated accessories

T8 Picture tubes and components
Colour TV picture tubes, black and white TV picture tubes, colour monitor tubes for data graphic display, monochrome monitor tubes for data graphic display, components for colour television, components for black and white television and monochrome data graphic display

T9 Photo and electron multipliers
Photomultiplier tubes, phototubes, single channel electron multipliers, channel electron multiplier plates

T10 Camera tubes and accessories, image intensifiers

T11 Microwave semiconductors and components

SEMICONDUCTORS (RED SERIES)

The red series of data handbooks is comprised of the following parts:

S1 **Diodes**
Small-signal germanium diodes, small-signal silicon diodes, voltage regulator diodes(< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes

S2 **Power diodes, thyristors, triacs**
Rectifier diodes, voltage regulator diodes (> 1,5 W), rectifier stacks, thyristors, triacs

S3 **Small-signal transistors**

S4a **Low-frequency power transistors and hybrid modules**

S4b **High-voltage and switching power transistors**

S5 **Field-effect transistors**

S6 **R.F. power transistors and modules**

S7 **Microminiature semiconductors for hybrid circuits**

S8 **Devices for optoelectronics**
Photosensitive diodes and transistors, light-emitting diodes, displays, photocouplers, infrared sensitive devices, photoconductive devices.

S9 Taken into handbook T11 of the blue series

S10 **Wideband transistors and wideband hybrid IC modules**

INTEGRATED CIRCUITS (PURPLE SERIES)

The purple series of data handbooks is comprised of the following parts:

IC1 **Bipolar ICs for radio and audio equipment**

IC2 **Bipolar ICs for video equipment**

IC3 **ICs for digital systems in radio, audio and video equipment**

IC4 **Digital integrated circuits**
CMOS HE4000B family

IC5 **Digital integrated circuits — ECL**
ECL10 000 (GX family), ECL100 000 (HX family), dedicated designs

IC6 **Professional analogue integrated circuits**

IC7 **Signetics bipolar memories**

IC8 **Signetics analogue circuits**

IC9 **Signetics TTL logic**

IC10 **Signetics Integrated Fuse Logic (IFL)**

IC11 **Microprocessors, microcomputers and peripheral circuitry**

INDEX OF TYPE NUMBERS

Data Handbooks S1 to S10

The inclusion of a type number in this publication does not necessarily imply its availability.

FET = Field-effect transistors
GD = Germanium diodes
Mm = Microminiature semiconductors for hybrid circuits
SD = Small-signal diodes
Sm = Small-signal transistors
Sp = Special diodes
T = Tuner diodes
Vrg = Voltage regulator diodes

* = series
FET = Field-effect transistors
Mm = Microminiature semiconductors for hybrid circuits
P = Low-frequency power transistors
Sm = Small-signal transistors

P = Low-frequency power transistors

P = Low-frequency power transistors
Sm = Small-signal transistors

FET = Field-effect transistors
HVP = High-voltage power transistors
Mm = Microminiature semiconductors for hybrid circuits
RFP = R.F. power transistors and modules
Sm = Small-signal transistors
WBT = Wideband hybrid IC transistors

* = series
FET = Field-effect transistors
Mm = Microminiature semiconductors for hybrid circuits
RFP = R.F. power transistors and modules
RT = Tripler
Sm = Small-signal transistors
ThM = Thyristor Modules
WBM = Wideband hybrid IC modules
WBT = Wideband hybrid IC transistors

Mm = Microminiature semiconductors for hybrid circuits
PDT = Photodiodes or transistors
RFP = R.F. power transistors and modules
Sm = Small-signal transistors
Th = Thyristors

* = series
FET = Field-effect transistors
Mm = Microminiature semiconductors for hybrid circuits
R = Rectifier diodes
Sm = Small-signal transistors
SP = Low-frequency switching power transistors
Th = Thyristors
Tri = Triacs

* = series
D = Displays
LED = Light emitting diodes
Mm = Microminiature semiconductors for hybrid circuits
Ph = Photoconductive devices
PhC = Photocouplers
R = Rectifier diodes
TS = Transient suppressor diodes
Vrf = Voltage reference diodes
Vrg = Voltage regulator diodes

* = series
Ar = Arrays
GD = Germanium diodes
I = Infrared devices
LED = Light emitting diodes
P = Low-frequency power transistors
Ph = Photoconductive devices
R = Rectifier diodes
SD = Small-signal diodes
Sm = Small-signal transistors
St = Rectifier stacks
Vrf = Voltage reference diodes
WBM = Wideband hybrid IC modules

A = Accessories
DH = Diecast heatsinks
FET = Field-effect transistors
HE = Heatsink extrusions
I = Infrared devices
Ph = Photoconductive devices
R = Rectifier diodes
RFP = R.F. power transistors and modules
SD = Small-signal diodes
Sm = Small-signal transistors
WBT = Wideband hybrid IC transistors

A = Accessories

TYPE NUMBER SURVEY

TYPE NUMBER SURVEY POWER TRANSISTORS

type number NPN	type number PNP	envelope	P_{tot} W	type number NPN	type number PNP	envelope	P_{tot} W
BD131	BD132	TO-126	15	BD651	BD652	TO-220	62,5
BD135	BD136	TO-126	8	BD675	BD676	TO-126	40
BD137	BD138	TO-126	8	BD677	BD678	TO-126	40
BD139	BD140	TO-126	8	BD679	BD680	TO-126	40
BD201	BD202	TO-220	60	BD681	BD682	TO-126	40
BD203	BD204	TO-220	60	BD683	BD684	TO-126	40
BD226	BD227	TO-126	12,5	BD813	BD814	TO-202	2
BD228	BD229	TO-126	12,5	BD815	BD816	TO-202	2
BD230	BD231	TO-126	12,5	BD817	BD818	TO-202	2
BD233	BD234	TO-126	25	BD825	BD826	TO-202	2
BD235	BD236	TO-126	25	BD827	BD828	TO-202	2
BD237	BD238	TO-126	25	BD829	BD830	TO-202	2
BD239	BD240	TO-220	30	BD839	BD840	TO-202	2
BD239A	BD240A	TO-220	30	BD841	BD842	TO-202	2
BD239B	BD240B	TO-220	30	BD843	BD844	TO-202	2
BD239C	BD240C	TO-220	30	BD845	BD846	TO-202	2
BD241	BD242	TO-220	40	BD847	BD848	TO-202	2
BD241A	BD242A	TO-220	40	BD849	BD850	TO-202	2
BD241B	BD242B	TO-220	40	BD933	BD934	TO-220	30
BD241C	BD242C	TO-220	40	BD935	BD936	TO-220	30
BD243	BD244	TO-220	65	BD937	BD938	TO-220	30
BD243A	BD244A	TO-220	65	BD939	BD940	TO-220	30
BD243B	BD244B	TO-220	65	BD941	BD942	TO-220	30
BD243C	BD244C	TO-220	65	BD943	BD944	TO-220	40
BD329	BD330	TO-126	15	BD945	BD946	TO-220	40
BD331	BD332	SOT-82	60	BD947	BD948	TO-220	40
BD333	BD334	SOT-82	60	BD949	BD950	TO-220	40
BD335	BD336	SOT-82	60	BD951	BD952	TO-220	40
BD337	BD338	SOT-82	60	BD953	BD954	TO-220	40
BD433	BD434	TO-126	36	BD955	BD956	TO-220	40
BD435	BD436	TO-126	36	BDT21	BDT20	TO-220	62,5
BD437	BD438	TO-126	36	BDT29	BDT30	TO-220	30
BD645	BD646	TO-220	62,5	BDT29A	BDT30A	TO-220	30
BD647	BD648	TO-220	62,5	BDT29B	BDT30B	TO-220	30
BD649	BD650	TO-220	62,5	BDT29C	BDT30C	TO-220	30

type number NPN	PNP	envelope	P_{tot} W	type number NPN	PNP	envelope	P_{tot} W
BDT31	BDT32	TO-220	40	BDX43	BDX46	TO-126	5
BDT31A	BDT32A	TO-220	40	BDX44	BDX47	TO-126	5
BDT31B	BDT32B	TO-220	40	BDX63	BDX62	TO-3	90
BDT31C	BDT32C	TO-220	40	BDX63A	BDX62A	TO-3	90
BDT41	BDT42	TO-220	65	BDX63B	BDX62B	TO-3	90
BDT41A	BDT42A	TO-220	65	BDX63C	BDX62C	TO-3	90
BDT41B	BDT42B	TO-220	65	BDX65	BDX64	TO-3	117
BDT41C	BDT42C	TO-220	65	BDX65A	BDX64A	TO-3	117
BDT61	BDT60	TO-220	50	BDX65B	BDX64B	TO-3	117
BDT61A	BDT60A	TO-220	50	BDX65C	BDX64C	TO-3	117
BDT61B	BDT60B	TO-220	50	BDX67	BDX66	TO-3	150
BDT61C	BDT60C	TO-220	50	BDX67A	BDX66A	TO-3	150
BDT63	BDT62	TO-220	90	BDX67B	BDX66B	TO-3	150
BDT63B	BDT62B	TO-220	90	BDX67C	BDX66C	TO-3	150
BDT63C	BDT62C	TO-220	90	BDX69	BDX68	TO-3	200
BDT65	BDT64	TO-220	125	BDX69A	BDX68A	TO-3	200
BDT65A	BDT64A	TO-220	125	BDX69B	BDX68B	TO-3	200
BDT65B	BDT64B	TO-220	125	BDX69C	BDX68C	TO-3	200
BDT65C	BDT64C	TO-220	125	BDX77	BDX78	TO-220	60
BDT91	BDT92	TO-220	90	BDX91	BDX92	TO-3	90
BDT93	BDT94	TO-220	90	BDX93	BDX94	TO-3	90
BDT95	BDT96	TO-220	90	BDX95	BDX96	TO-3	90
BDV65	BDV64	SOT-93	125	BDY90		TO-3	40
BDV65A	BDV64A	SOT-93	125	BDY90A		TO-3	40
BDV65B	BDV64B	SOT-93	125	BDY91		TO-3	40
BDV65C	BDV64C	SOT-93	125	BDY92		TO-3	40
BDV67A	BDV66A	SOT-93	200	BF419		TO-126	6
BDV67B	BDV66B	SOT-93	200	BF457		TO-126	6
BDV67C	BDV66C	SOT-93	200	BF458		TO-126	6
BDV67D	BDV66D	SOT-93	200	BF459		TO-126	6
BDV91	BDV92	SOT-93	100	BF469	BF470	TO-126	1,8
BDV93	BDV94	SOT-93	100	BF471	BF472	TO-126	1,8
BDV95	BDV96	SOT-93	100	BF819		TO-202	6
BDW55	BDW56	TO-126	8	BF857		TO-202	6
BDW57	BDW58	TO-126	8	BF858		TO-202	6
BDW59	BDW60	TO-126	8	BF859		TO-202	6
BDX35		TO-126	15	BF869	BF870	TO-202	5
BDX36		TO-126	15	BF871	BF872	TO-202	5
BDX37		TO-126	15	BU208A		TO-3	80
BDX42	BDX45	TO-126	5	BU208B		TO-3	80

type number NPN	PNP	envelope	P_{tot} W	type number NPN	PNP	envelope	P_{tot} W
BU326;A		TO-3	60	BUV82;83		SOT-93	70
BU426;A		SOT-93	70	BUV89		SOT-93A	125
BU433		SOT-93	70	BUW11;A		SOT-93	100
BU505		TO-220	75	BUW12;A		SOT-93	125
BU508A		SOT-93A	125	BUW13;A		SOT-93	175
BU705		SOT-93A	75	BUW84;85		SOT-82	50
BU806		TO-220	60	BUX46;A		TO-3	85
BU807		TO-220	60	BUX47;A		TO-3	125
BU824		TO-202	2	BUX48;A		TO-3	175
BU826		SOT-93	125	BUX80;81		TO-3	100
BUS11;A		TO-3	100	BUX82;83		TO-3	60
BUS12;A		TO-3	125	BUX84;85		TO-220	40
BUS13;A		TO-3	175	BUX86;87		TO-126	20
BUS14;A		TO-3	250	BUX88		TO-3	160
BUT11;A		TO-220	100	BUX90		TO-3	125
				BUX98;A		TO-3	250
				BUY89		TO-3	80
				PH3055T	PH2955T	TO-220	75

TYPE NUMBER SURVEY ACCESSORIES

type number	description	envelope
56201d	mica washer (up to 500 V)	TO-3
56201j	insulating bushes (up to 500 V)	TO-3
56261a	insulating bushes (up to 500 V)	TO-3
56326	metal washer	TO-126
56339	mica washer (500 to 2000 V)	TO-3
56352	insulating mounting support	TO-3
56353	spring clip	TO-126/SOT-82
56354	mica insulator	TO-126/SOT-82
56359b	mica washer (up to 1000 V)	TO-220
56359c	insulating bush (up to 800 V)	TO-220
56359d	rectangular insulating bush (up to 1000 V)	TO-220
56360a	rectangular washer (brass)	TO-220
56363	spring clip (direct mounting)	TO-220
56364	spring clip (insulated mounting)	TO-220
56367	alumina insulator (up to 2000 V)	TO-220
56368a	mica insulator (up to 800 V)	TO-220
56368b	insulating bush (up to 800 V)	SOT-93
56369	mica insulator (up to 2 kV)	SOT-93
56378	mica insulator (up to 1500 V)	TO-220
56379	spring clip	SOT-93
56387a	mica insulator (up to 300 V)	SOT-93
56387b	insulating bush (up to 300 V)	TO-126
		TO-126

SELECTION GUIDE

GENERAL PURPOSE DARLINGTON TRANSISTORS

I_C A	pol.	collector-emitter voltage (open base) V_{CEO} (V) 45	60	80	100	120	130	150	200			P_{tot} W	case
1	N	BDX42*	BDX43*	BDX44*									
	P	BDX45*	BDX46*	BDX47*								5	TO-126
4	N	BD675	BD677	BD679	BD681	BD683							
	P	BD676	BD678	BD680	BD682	BD684						40	TO-126
	N		BDT61	BDT61A	BDT61B	BDT61C							
	P		BDT60	BDT60A	BDT60B	BDT60C						50	TO-220
6	N		BD331	BD333	BD335	BD337							
	P		BD332	BD334	BD336	BD338						60	SOT-82
8	N		BD645	BD647	BD649	BD651							
	P		BD646	BD648	BD650	BD652						62,5	TO-220
	N												
	N						BDT21	BU807	BU806			60	TO-220
	P						BDT20					62,5	TO-220
	N		BDX63	BDX63A	BDX63B	BDX63C							
	P		BDX62	BDX62A	BDX62B	BDX62C						90	TO-3
10	N		BDT63	BDT63A	BDT63B	BDT63C							
	P		BDT62	BDT62A	BDT62B	BDT62C						90	TO-220
12	N		BDT65	BDT65A	BDT65B	BDT65C							
	P		BDT64	BDT64A	BDT64B	BDT64C						125	TO-220
	N		BDV65	BDV65A	BDV65B	BDV65C							
	P		BDV64	BDV64A	BDV64B	BDV64C						125	SOT-93
	N		BDX65	BDX65A	BDX65B	BDX65C							
	P		BDX64	BDX64A	BDX64B	BDX64C						117	TO-3
16	N		BDV67	BDV67A	BDV67B	BDV67C							
	P		BDV66	BDV66A	BDV66B	BDV66C						200	SOT-93
	N		BDX67	BDX67A	BDX67B	BDX67C							
	P		BDX66	BDX66A	BDX66B	BDX66C						150	TO-3
25	N		BDX69	BDX69A	BDX69B	BDX69C							
	P		BDX68	BDX68A	BDX68B	BDX68C						200	TO-3

* V_{CER}

HIGH-VOLTAGE TRANSISTORS video output - deflection - SMPS - motorcontrol

I_C A	pol.	collector-emitter voltage (open base) V_{CEO} (V) 160	250	300	375	400	450	700	800			P_{tot} W	case
0,05	N		BF469	BF471*								1,8	TO-126
	P		BF470	BF472*									
	N		BF869	BF871*								5	TO-202
	P		BF870	BF872*									
0,1	N		BF419									6	TO-126
	N	BF457	BF458	BF459									
	N		BF819									6	TO-202
	N	BF857	BF858	BF859									
0,5	N					BUX86	BUX87					20	TO-126
2	N					BUW84	BUW85					50	SOT-82
	N					BUX84	BUX85					40	TO-220
3,5	N					BUX46	BUX46A					85	TO-3
5	N					BUT11	BUT11A					100	TO-220
	N					BUW11	BUW11A					100	SOT-93
	N					BUS11	BUS11A					100	TO-3
6	N				BU326	BU326A						60	TO-3
	N				BU426	BU426A						70	SOT-93
	N				BU433							70	SOT-93
	N					BUX82	BUX83					60	TO-3
	N					BUV82	BUV83					70	SOT-93
	N								BUY89			80	TO-3
8	N								BUV89			125	SOT-93
	N					BUW12	BUW12A					125	SOT-93
	N					BUS12	BUS12A					125	TO-3
	N							BU508A				125	SOT-93
9	N					BUX47	BUX47A					125	TO-3
10	N					BUX80	BUX81					100	TO-3
12	N								BUX88			160	TO-3
15	N					BUW13	BUW13A					175	SOT-93
	N					BUS13	BUS13A					175	TO-3
	N					BUX48	BUX48A					175	TO-3
30	N					BUS14	BUS14A					250	TO-3
	N					BUX98	BUX98A					250	TO-3

* V_{CER}

GENERAL PURPOSE POWER TRANSISTORS

I_C A	pol.	collector-emitter voltage (open base) V_{CEO} (V)										P_{tot} W	case
		20	22	32	40	45	60	80	100	120	140		
1	N					BD135	BD137	BD139				8	TO-126
	P					BD136	BD138	BD140					
	N					BD825	BD827	BD829					TO-202
	P					BD826	BD828	BD830					
	N					BDW55	BDW57	BDW59					TO-126
	P					BDW56	BDW58	BDW60					
	N				BDT29		BDT29A	BDT29B	BDT29C			30	TO-220
	P				BDT30		BDT30A	BDT30B	BDT30C				
1,5	N					BD226	BD228	BD230				12,5	TO-126
	P					BD227	BD229	BD231					
	N					BD839	BD841	BD843	BD845	BD847	BD849	10	TO-202
	P					BD840	BD842	BD844	BD846	BD848	BD850		
2	N					BD233	BD235	BD237				25	TO-126
	P					BD234	BD236	BD238					
	N					BD813	BD815	BD817				12,5	TO-202
	P					BD814	BD816	BD818					
3	N					BD239	BD239A	BD239B	BD239C			30	TO-220
	P					BD240	BD240A	BD240B	BD240C				
	N					BD131						15	TO-126
	P					BD132							
	N	BD329											
	P	BD330											
	N					BD933	BD935	BD937	BD939	BD941		30	TO-220
	P					BD934	BD936	BD938	BD940	BD942			
	N				BDT31		BDT31A	BDT31B	BDT31C				
	P				BDT32		BDT32A	BDT32B	BDT32C				
4	N		BD433	BD435	BD437							36	TO-126
	P		BD434	BD436	BD438								

GENERAL PURPOSE POWER TRANSISTORS

I_C A	pol.	collector-emitter voltage (open base) V_{CEO} (V) 20	22	32	40	45	60	80	100	120	140	P_{tot} W	case
5	N					BD241	BD241A	BD241B	BD241C			40	TO-220
	P					BD240	BD240A	BD240B	BD240C				
	N						BDX35					15	TO-126
	N						BDX36						
	N		BD943	BD945		BD947	BD949	BD951	BD955	BD953		40	TO-220
	P		BD944	BD946		BD948	BD950	BD952	BD956	BD954			
6	N					BD243	BD243A	BD243B	BD243C			65	TO-220
	P					BD244	BD244A	BD244B	BD244C				
	N				BDT41		BDT41A	BDT41B	BDT41C			65	TO-220
	P				BDT42		BDT42A	BDT42B	BDT42C				
8	N					BD201	BD203	BDX77				60	TO-220
	P					BD202	BD204	BDX78					
	N						BDX91	BDX93	BDX95			90	TO-3
	P						BDX92	BDX94	BDX96				
10	N						PH3055T					75	TO-220
	P						PH2955T						
	N						BDT91	BDT93	BDT95			90	TO-220
	P						BDT92	BDT94	BDT96				
	N						BDV91	BDV93	BDV95			100	SOT-93
	P						BDV92	BDV94	BDV96				

LOW-VOLTAGE SWITCHING TRANSISTORS

I_C A	pol.	collector-emitter voltage (open base) V_{CEO} (V)					60	80	100			P_{tot} W	case
10	N						BDY92	BDY91	BDY90			40	TO-3
12	N								BDY90A			40	TO-3

ACCESSORIES

CLIP MOUNTING

envelope	direct mounting		insulated mounting			
	clip		mica	alumina	clip	
TO-126 (SOT-32)	56353		56354		56353	
SOT-82	56353		56354		56353	
TO-220 (SOT-78)	56363		56369 or	56367	56364	
SOT-93	56379		56378		56379	

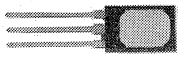
SCREW MOUNTING

envelope	direct mounting		insulated mounting			
	metal washer	mounting material	mica washer	insul. bush	metal washer	mounting material
TO-126 (SOT-32)	56326	M3				
up to 300 V			56387a	56387b	56326	M2,5
TO-220 (SOT-78)	56360a	M3				
up to 800 V			56359b	56359c	56360a	M3
up to 1000 V			56359b	56359d	56360a	M3
SOT-93	-	M4	56368a	56368b		M3
TO-3 (SOT-3)	-	M4				
up to 500 V			56201d	56201j or 56261a		M3
up to 2000 V			56339	56352		M3

The accessories mentioned can be supplied on request.

See also chapter Mounting Instructions.

TO-126
(SOT-32)

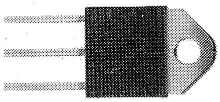


type number		P_{tot}	V_{CEO}
NPN	PNP	W	V
BF469	BF470	1,8	250
BF471	BF472		300*
BDX42	BDX45	5	45*
BDX43	BDX46		60*
BDX44	BDX47		80*
BF419		6	250
BF457			160
BF458			250
BF459			300
BD135	BD136	8	45
BD137	BD138		60
BD139	BD140		80
BDW55	BDW56	8	45
BDW57	BDW58		60
BDW59	BDW60		80
BD226	BD227	12,5	45
BD228	BD229		60
BD230	BD231		80
BD131	BD132	15	45
BD329	BD330		20
BDX35			60
BDX36			60
BDX37			80
BUX86		20	400
BUX87			450
BD233	BD234	25	45
BD235	BD236		60
BD237	BD238		80
BD433	BD434	36	22
BD435	BD436		32
BD437	BD438		45
BD675	BD676	40	45
BD677	BD678		60
BD679	BD680		80
BD681	BD682		100
BD683	BD684		120

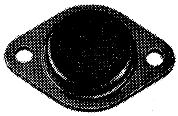
* V_{CER}

type number		P_{tot}	V_{CEO}
NPN	PNP	W	V
BUW84		50	400
BUW85			450
BD331	BD332	60	60
BD333	BD334		80
BD335	BD336		100
BD337	BD338		120

SOT-93
(SOT-93)



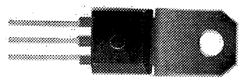
type number		P_{tot}	V_{CEO}
NPN	PNP	W	V
BU426		70	375
BU426A			400
BU433			375
BUV82			400
BUV83			450
BDV91	BDV92	100	60
BDV93	BDV94		80
BDV95	BDV96		100
BUW11			400
BUW11A			450
BDV65	BDV64	125	60
BDV65A	BDV64A		80
BDV65B	BDV64B		100
BDV65C	BDV64C		120
BUW12			400
BUW12A			450
BU508A			700
BUV89			800
BUW13		175	400
BUW13A			450
BDV67	BDV66	200	60
BDV67A	BDV66A		80
BDV67B	BDV66B		100
BDV67C	BDV66C		120



TO-3
(SOT-3)

type number NPN	type number PNP	P_{tot} W	V_{CEO} V
BDY90		40	100
BDY90A			100
BDY91			80
BDY92			60
BU326		60	375
BU326A			400
BUX82		60	400
BUX83			450
BUY89		80	800
BUX46		85	400
BUX46A			450
BDX63	BDX62	90	60
BDX91	BDX92		60
BDX63A	BDX62A		80
BDX93	BDX94		80
BDX63B	BDX62B		100
BDX95	BDX96		100
BDX63C	BDX62C		120
BUS11		100	400
BUS11A			450
BUX80		100	400
BUX81			450
BDX65	BDX64	117	60
BDX65A	BDX64A		80
BDX65B	BDX64B		100
BDX65C	BDX64C		120
BUS12		125	400
BUS12A			450
BUX47			400
BUX47A			450
BDX67	BDX66	150	60
BDX67A	BDX66A		80
BDX67B	BDX66B		100
BDX67C	BDX66C		120
BUX88		160	800

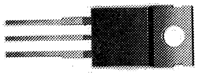
type number NPN	type number PNP	P_{tot} W	V_{CEO} V
BUS13		175	400
BUS13A			450
BUX48			400
BUX48A			450
BDX69	BDX68	200	60
BDX69A	BDX68A		80
BDX69B	BDX68B		100
BDX69C	BDX68C		120
BUS14		250	400
BUS14A			450
BUX98			400
BUX98A			450



TO-202
(SOT-128)

type number NPN	type number PNP	P_{tot} W	V_{CEO} V
BF869	BF870	5(1,6)	250
BF871	BF872		300*
BF819		6(1,2)	250
BF857		6(2)	160
BF858			250
BF859			300
BD825	BD826	8(2)	45
BD827	BD828		60
BD829	BD830		80
BD839	BD840	10(2)	45
BD841	BD842		60
BD843	BD844		80
BD845	BD846		100
BD847	BD848		120
BD849	BD850		140
BD813	BD814	12,5 (2)	45
BD815	BD816		60
BD817	BD818		80

* V_{CER}
( ) free air dissipation



TO-220
(SOT-78)

type number		P_{tot}	V_{CEO}
NPN	PNP	W	V
BD239	BD240	30	45
BD239A	BD240A		60
BD239B	BD240B		80
BD239C	BD240C		100
BD933	BD934	30	45
BD935	BD936		60
BD937	BD938		80
BD939	BD940		100
BD941	BD942		120
BDT29	BDT30		40
BDT29A	BDT30A		60
BDT29B	BDT30B		80
BDT29C	BDT30C		100
BD241	BD240	40	45
BD241A	BD241A		60
BD241B	BD241B		80
BD241C	BD241C		100
BD943	BD944	40	22
BD945	BD946		32
BD947	BD948		45
BD949	BD950		60
BD951	BD952		80
BD953	BD954		100
BD955	BD956		120
BDT31	BDT32		45
BDT31A	BDT32A		60
BDT31B	BDT32B		80
BDT31C	BDT32C		100
BUX84		40	400
BUX85			450
BDT61	BDT60	50	60
BDT61A	BDT60A		80
BDT61B	BDT60B		100
BDT61C	BDT60C		120
BD201	BD202	60	45
BD203	BD204		60
BDX77	BDX78		80
BU807		60	150
BU806			200

type number		P_{tot}	V_{CEO}
NPN	PNP	W	V
BD645	BD646	62,5	60
BD647	BD648		80
BD649	BD650		100
BD651	BD652		120
BDT21	BDT20	62,5	130
BD243	BD244	65	45
BD243A	BD244A		60
BD243B	BD244B		80
BD243C	BD244C		100
BDT41	BDT42	65	40
BDT41A	BDT42A		60
BDT41B	BDT42B		80
BDT41C	BDT42C		100
PH3055T	PH2955T	75	60
BDT91	BDT92	90	60
BDT93	BDT94		80
BDT95	BDT96		100
BDT63	BDT62	90	60
BDT63A	BDT62A		80
BDT63B	BDT62B		100
BDT63C	BDT62C		120
BUT11		100	400
BUT11A			450
BDT65	BDT64	125	60
BDT65A	BDT64A		80
BDT65B	BDT64B		100
BDT65C	BDT64C		120

GENERAL

Rating systems
Transistor ratings
Letter symbols
SOAR curves

TRANSISTOR RATINGS

The ratings are presented as voltage, current, power and temperature ratings. The list of these ratings and their definitions is given as follows:

Transistor voltage ratings

Collector to base voltage ratings

V_{CBmax} — The maximum permissible instantaneous voltage between collector and base terminals. The collector voltage is negative with respect to base in PNP transistors and positive with respect to base in NPN types.

V_{CBmax} (IE = 0) — The maximum permissible instantaneous voltage between collector and base terminals, when the emitter terminal is open circuited.

Emitter to base voltage ratings

V_{EBmax} — The maximum permissible instantaneous reverse voltage between emitter and base terminal. The emitter voltage is negative with respect to base for PNP transistor and positive with respect to base for NPN types.

V_{EBmax} ($I_C = 0$) — The maximum permissible instantaneous reverse voltage between emitter and base terminals when the collector terminal is open circuited.

Collector to emitter voltage ratings

V_{CEmax} — The maximum permissible instantaneous voltage between collector and emitter terminals. The collector voltage is negative with respect to emitter in PNP transistors and positive with respect to emitter in NPN types. This rating is very dependent on circuit conditions and collector current and it is necessary to refer to the curve of V_{CE} versus I_C for the appropriate circuit condition in order to obtain the correct rating.

V_{CEmax} (Cut-off) — The maximum permissible instantaneous voltage between collector and emitter terminals when the emitter current is reduced to zero by means of a reverse emitter base voltage, i.e. the base voltage is normally positive with respect to emitter for PNP transistor and negative with respect to emitter for NPN types.

NOTE: The term "cut-off" is sometimes replaced by $V_{BE} > x$ volts, or $\frac{R_B}{R_E}$, $\leqslant y$ which are equivalent conditions under which the device may be cut-off.

V_{CEmax} ($I_C = x$ mA) — The maximum permissible instantaneous voltage between collector and emitter terminals when the collector current is at a high value, often the max. rated value.

V_{CEmax} ($I_B = 0$) — The maximum permissible instantaneous voltage between collector and emitter terminals when the base terminal is open circuited or when a very high resistance is in series with the base terminal. Special care must be taken to ensure that thermal runaway due to excessive collector leakage current does not occur in this condition.

Due to the current dependency of V_{CE} it is usual to present this information as a voltage rating chart which is a curve of collector current versus collector to emitter voltage (see Fig. 1).

This curve is divided into two areas:

A permissible area of operation under all conditions of base drive provided the dissipation rating is not exceeded (area 1) and an area where operation is allowable under certain specified conditions (area 2). To assist in determining the rating in this second area, further curves are provided relating the voltage rating to external circuit conditions, for example:

$$\frac{R_B}{R_E},\ R_B,\ Z_{Bg},\ V_{BE},\ I_B \text{ or } \frac{V_{BB}}{R_B}.$$

An example of this type of curve is given in Fig. 2 as V_{CE} versus $\frac{R_B}{R_E}$ for two different values of collector current.

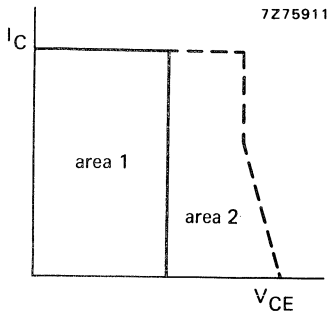


Fig. 1.

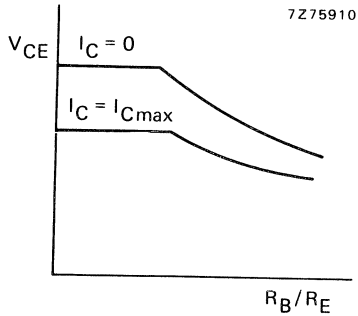


Fig. 2.

It should be noted that when R_E is shunted by a capacitor, the collector voltage V_{CE} during switching must be restricted to a value which does not rely on the effect of R_E.
In the case of an inductive load and when an energy rating is given, it may be permissible to operate outside the rated area provided the spcified energy rating is not exceeded.

Transistor current ratings

Collector current ratings

I_{Cmax}	The maximum permissible collector current. Without further qualification, the d.c. value is implied.
$I_{C(AV)max}$	The maximum permissible average value of the total collector current
I_{CM}	The maximum permissible instantaneous value of the total collector current.

Emitter current ratings

I_{Emax}	The maximum permissible emitter current. Without further qualification, the d.c. value is implied.
$I_{E(AV)max}$	The maximum permissible average value of the total emitter current.
$I_{ER(AV)max}$	The maximum permissible average value of the total emitter current when operating in the reverse emitter-base breakdown region.
I_{EM}	The maximum permissible instantaneous value of the total emitter current.
I_{ERM}	The maximum permissible instantaneous value of the total reverse emitter current allowable in the reverse breakdown region.

Base current ratings

I_{Bmax}	The maximum permissible base current. Without further qualification, the d.c. value is implied.
$I_{B(AV)max}$	The maximum permissible average value of the total base current.
$I_{BR(AV)max}$	The maximum permissible average value of the total reverse base current allowable in the reverse breakdown region.
I_{BM}	The maximum permissible instantaneous value of the total base current. The rating also includes the switch off current.
I_{BRM}	The maximum permissible instantaneous value of the total reverse current allowable in the reverse breakdown region.

Transistor power ratings

P_{tot} max: The total maximum permissible continuous power dissipation in the transistor and includes both the collector-base dissipation and the emitter-base dissipation. Under steady state conditions the total power is given by the expression:

$$P_{tot} = V_{CE} \times I_C + V_{BE} \times I_B.$$

In order to distinguish between "steady state" and "pulse" conditions the terms "steady state power (P_S)" and "pulse power (P_P)" are often used. The permissible total power dissipation is dependent upon temperature and its relationship is shown by means of a chart as shown in Fig. 3.

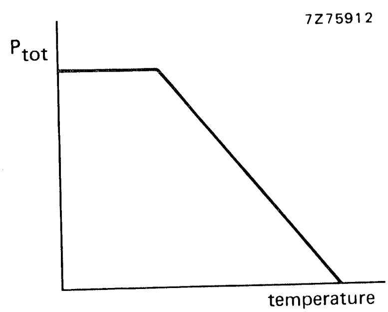


Fig. 3.

The temperature may be ambient, case or mounting base temperatures. Where a cooling clip or a heatsink is attached to the device, the allowable power dissipation is also dependent on the efficiency of the heatsink.

The efficiency of this clip or heatsink is measured in terms of its thermal resistance ($R_{th\ h}$) normally expressed in degrees kelvin per watt (K/W). For mounting base rated devices, the added effect of the contact resistance ($R_{th\ i}$) must be taken into account.

The effect of heatsinks of various thermal resistance and contact resistance is often included in the above chart.

Thus for any heatsink of known thermal resistance and any given ambient temperature, the maximum permissible power dissipation can be established. Alternatively, knowing the power dissipation which will occur and the ambient temperature, the necessary heatsink thermal resistance can be calculated.

A general expression from which the total permissible steady state power dissipation can be calculated is:

$$P_{tot} = \frac{T_j - T_{amb}}{R_{th\ j\text{-}a}}$$

where $R_{th\ j\text{-}a}$ is the thermal resistance from the transistor junction to the ambient. For case rated or mounting base rated devices, the thermal resistance $R_{th\ j\text{-}a}$ is made up of the thermal resistance junction to case or mounting base $(R_{th\ j\text{-}mb})$, the contact thermal resistance $(R_{th\ i})$ and the heatsink thermal resistance $R_{th\ h}$.

For the calculation of pulse power operation P_p, the maximum pulse power is obtained by the aid of a chart as shown in Fig. 4.

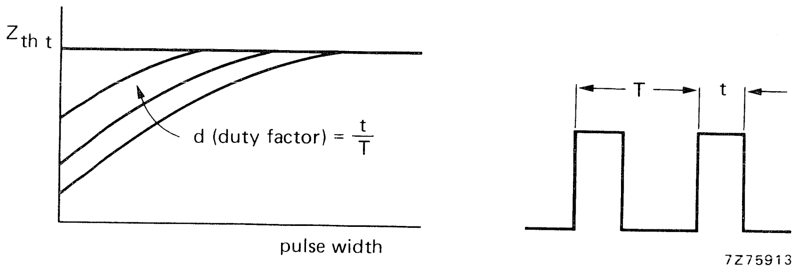


Fig. 4.

The general expression from which the maximum pulse power dissipation can be calculated is:

$$P_p = \frac{T_j - T_{amb} - P_s \times R_{th\ j\text{-}a}}{Z_{th\ t} + d\ (R_{th\ c\text{-}a})}$$

where $Z_{th\ t}$ and d are given in the above chart and $R_{th\ c\text{-}a}$ is the thermal resistance between case and ambient for case rated device. For mounting base rated device, it is equal to $R_{th\ h} + R_{th\ i}$ and is zero for free air rated device because the effect of the temperature rise of the case over the ambient for a pulse train is already included in $Z_{th\ t}$.

Temperature ratings

T_{jmax}	The maximum permissible junction temperature which is used as the basis for the calculation of power ratings. Unless otherwise stated, the continuous value is implied.
T_{jmax} (continous operation)	The maximum permissible continuous value.
T_{jmax} (intermittent operation)	The maximum permissible instantaneous junction temperature usually allowed for a total duration of 200 hours.
T_{mb}	The temperature of the surface making contact with a heatsink. This is confined to devices where a flange or stud for fixing onto a heatsink forms an integral part of the envelope.
T_{case}	The temperature of the envelope. This is confined to devices to which may be attached a clip-on cooling fin.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

LETTER SYMBOLS FOR TRANSISTORS AND SIGNAL DIODES

based on IEC Publication 148

LETTER SYMBOLS FOR CURRENTS, VOLTAGES AND POWERS

Basic letters

The basic letters to be used are:

I, i = current
V, v = voltage
P, p = power.

Lower-case basic letters shall be used for the representation of instantaneous values which vary with time.
In all other instances upper-case basic letters shall be used.

Subscripts

A, a	Anode terminal
(AV), (av)	Average value
B, b	Base terminal, for MOS devices: Substrate
(BR)	Breakdown
C, c	Collector terminal
D, d	Drain terminal
E, e	Emitter terminal
F, f	Forward
G, g	Gate terminal
K, k	Cathode terminal
M, m	Peak value
O, o	As third subscript: The terminal not mentioned is open circuited
R, r	As first subscript: Reverse. As second subscript: Repetitive. As third subscript: With a specified resistance between the terminal not mentioned and the reference terminal.
(RMS), (rms)	R.M.S. value
S, s	As first or second subscript: Source terminal (for FETS only) As second subscript: Non-repetitive (not for FETS) As third subscript: Short circuit between the terminal not mentioned and the reference terminal
X, x	Specified circuit
Z, z	Replaces R to indicate the actual working voltage, current or power of voltage reference and voltage regulator diodes.

Note: No additional subscript is used for d.c. values.

Upper-case subscripts shall be used for the indication of:

a) continuous (d.c.) values (without signal)

Example I_B

b) instantaneous total values

Example i_B

c) average total values

Example $I_{B(AV)}$

d) peak total values

Example I_{BM}

e) root-mean-square total values

Example $I_{B(RMS)}$

Lower-case subscripts shall be used for the indication of values applying to the varying component alone:

a) instantaneous values

Example i_b

b) root-mean-square values

Example $I_{b(rms)}$

c) peak values

Example I_{bm}

d) average values

Example $I_{b(av)}$

Note: If more than one subscript is used, subscript for which both styles exist shall either be all upper-case or all lower-case.

Additional rules for subscripts

Subscripts for currents

Transistors: If it is necessary to indicate the terminal carrying the current, this should be done by the first subscript (conventional current flow from the external circuit into the terminal is positive).

Examples: I_B, i_B, i_b, I_{bm}

Diodes: To indicate a forward current (conventional current flow into the anode terminal) the subscript F or f should be used; for a reverse current (conventional current flow out of the anode terminal) the subscript R or r should be used.

Examples: I_F, I_R, i_F, $I_{f(rms)}$

Subscripts for voltages

Transistors: If it is necessary to indicate the points between which a voltage is measured, this should be done by the first two subscripts. The first subscript indicates the terminal at which the voltage is measured and the second the reference terminal or the circuit node. Where there is no possibility of confusion, the second subscript may be omitted.

Examples: V_{BE}, v_{BE}, v_{be}, V_{bem}

Diodes: To indicate a forward voltage (anode positive with respect to cathode), the subscript F or f should be used; for a reverse voltage (anode negative with respect to cathode) the subscript R or r should be used.

Examples: V_F, V_R, v_F, V_{rm}

Subscripts for supply voltages or supply currents

Supply voltages or supply currents shall be indicated by repeating the appropriate terminal subscript.

Examples: V_{CC}, I_{EE}

Note: If it is necessary to indicate a reference terminal, this should be done by a third subscript

Example : V_{CCE}

Subscripts for devices having more than one terminal of the same kind

If a device has more than one terminal of the same kind, the subscript is formed by the appropriate letter for the terminal followed by a number; in the case of multiple subscripts, hyphens may be necessary to avoid misunderstanding.

Examples: I_{B2} = continuous (d.c.) current flowing into the second base terminal

V_{B2-E} = continuous (d.c.) voltage between the terminals of second base and emitter

Subscripts for multiple devices

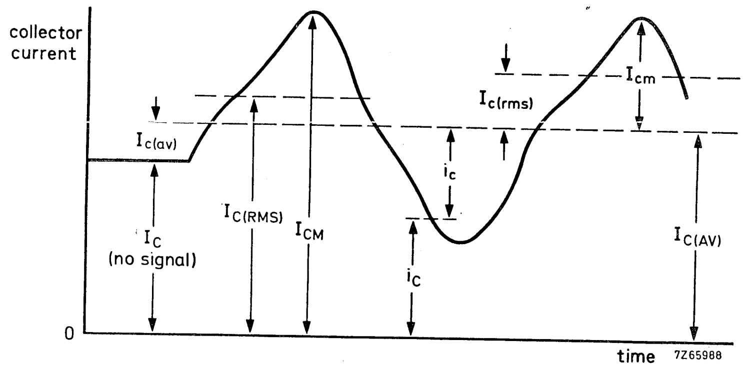
For multiple unit devices, the subscripts are modified by a number preceding the letter subscript; in the case of multiple subscripts, hyphens may be necessary to avoid misunderstanding.

Examples: I_{2C} = continuous (d.c.) current flowing into the collector terminal of the second unit

V_{1C-2C} = continuous (d.c.) voltage between the collector terminals of the first and the second unit.

Application of the rules

The figure below represents a transistor collector current as a function of time. It consists of a continuous (d.c.) current and a varying component.



LETTER SYMBOLS FOR ELECTRICAL PARAMETERS

Definition

For the purpose of this Publication, the term "electrical parameter" applies to four-pole matrix parameters, elements of electrical equivalent circuits, electrical impedances and admittances, inductances and capacitances.

Basic letters

The following is a list of the most important basic letters used for electrical parameters of semiconductor devices.

B, b = susceptance; imaginary part of an admittance

C = capacitance

G, g = conductance; real part of an admittance

H, h = hybrid parameter

L = inductance

R, r = resistance; real part of an impedance

X, x = reactance; imaginary part of an impedance

Y, y = admittance;

Z, z = impedance;

Upper-case letters shall be used for the representation of:

a) electrical parameters of external circuits and of circuits in which the device forms only a part;

b) all inductances and capacitances.

Lower-case letters shall be used for the representation of electrical parameters inherent in the device (with the exception of inductances and capacitances).

Subscripts

General subscripts

The following is a list of the most important general subscripts used for electrical parameters of semiconductor devices:

F, f = forward; forward transfer
I, i (or 1) = input
L, l = load
O, o (or 2) = output
R, r = reverse; reverse transfer
S, s = source

Examples: Z_S, h_f, h_F

The upper-case variant of a subscript shall be used for the designation of static (d.c.) values.

Examples : h_{FE} = static value of forward current transfer ratio in common-emitter configuration (d.c. current gain)

R_E = d.c. value of the external emitter resistance.

Note: The static value is the slope of the line from the origin to the operating point on the appropriate characteristic curve, i.e. the quotient of the appropriate electrical quantities at the operating point.

The lower-case variant of a subscript shall be used for the designation of small-signal values.

Examples: h_{fe} = small-signal value of the short-circuit forward current transfer ratio in common-emitter configuration

$Z_e = R_e + jX_e$ = small-signal value of the external impedance

Note: If more than one subscript is used, subscripts for which both styles exist shall either be all upper-case or all lower-case

Examples: h_{FE}, y_{RE}, h_{fe}

Subscripts for four-pole matrix parameters

The first letter subscript (or double numeric subscript) indicates input, output, forward transfer or reverse transfer

Examples: h_i (or h_{11})
h_o (or h_{22})
h_f (or h_{21})
h_r (or h_{12})

A further subscript is used for the identification of the circuit configuration. When no confusion is possible, this further subscript may be omitted.

Examples: h_{fe} (or h_{21e}), h_{FE} (or h_{21E})

Distinction between real and imaginary parts

If it is necessary to distinguish between real and imaginary parts of electrical parameters, no additional subscripts should be used. If basic symbols for the real and imaginary parts exist, these may be used.

Examples: $Z_i = R_i + jX_i$
$y_{fe} = g_{fe} + jb_{fe}$

If such symbols do not exist or if they are not suitable, the following notation shall be used:

Examples: Re (h_{ib}) etc. for the real part of h_{ib}
Im (h_{ib}) etc. for the imaginary part of h_{ib}

TRANSISTOR SAFE OPERATING AREA

If a power transistor is to give reliable service, four operating limits must be observed:

- Maximum collector current.
- Maximum collector-emitter voltage.
- Maximum power dissipation.
- Second breakdown limit.

These limits are all specified in the data sheets; the purpose here is to enable designers to make the best use of that information.

Collector current

Maximum collector current I_{Cmax} is specified in the data sheets for d.c. operation. For pulsed operation a higher collector current I_{Cmax} is permitted, for a defined maximum pulse length (usually 10 ms) and duty factor (usually 0,01).

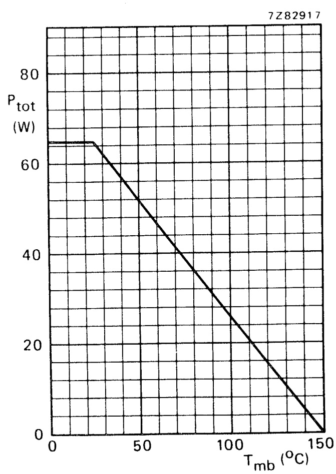
For power switching transistors I_{Csat} is given; this is the value at which switching times and saturation voltage is measured.

Collector-emitter voltage

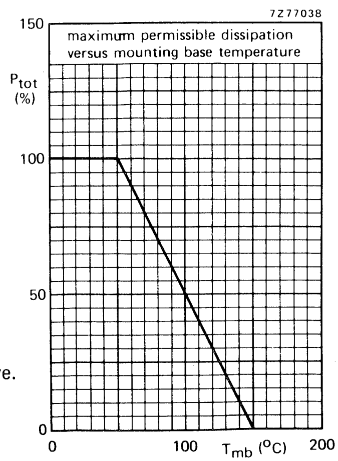
Maximum collector-emitter voltage V_{CEO} is also specified in the data sheets, but no extension is allowed for pulsed operation. In the case of power transistors specifically designed for switching inductive loads some extension may be allowed, but then only under specified conditions of collector current, base-emitter voltage and emitter-base resistance as stated in the relevant data sheets.

Power dissipation

Maximum power dissipation $P_{tot\,max}$ is specified in the data sheets for a given mounting base temperature. This is usually 25 °C but may be any, much higher temperature. $P_{tot\,max}$ applies up to the stated temperature; above it derating must be applied. A power derating curve of the form shown in Fig. 1a and 1b given in the data sheets. With it, maximum allowable power dissipation can be calculated for any mounting base temperature up to $T_{j\,max}$.



(a)



(b)

Fig. 1 Power derating curve.

Total power dissipation is given by

$$P_{tot} = I_C V_{CE} + I_B V_{BE}.$$

The second term can usually be disregarded, so $P_{tot} \approx I_C V_{CE}$.
Heat dissipated in the collector-base junction flows through the thermal resistance between junction and mounting base, see Fig. 2.

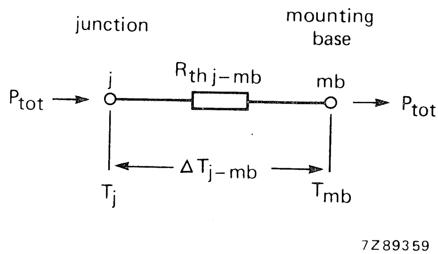


Fig. 2 Heat transport in a transistor with power dissipation constant with respect to time.

By analogy with Ohm's law, under steady-state conditions (d.c. operation)

$$P_{tot} = \frac{T_j - T_{mb}}{R_{th\,j\text{-}mb}}.$$

There are two limitations to P_{tot}
– When $T_{mb} \leqslant T_{mb\,spec}$

$$P_{tot\,max} = \frac{\Delta T_{j\text{-}mb\,max}}{R_{th\,j\text{-}mb}}.$$

– when $T_{mb} > T_{mb\,spec}$

$$P_{tot\,max} = \frac{\Delta T_{j\,max} - T_{mb}}{R_{th\,j\text{-}mb}}$$

$T_{mb\,spec}$ being the mounting base temperature at which $P_{tot\,max}$ is specified in the data sheets, and

$$\Delta T_{j\text{-}mb\,max} = T_{j\,max} - T_{mb\,spec}.$$

For pulsed operation a higher dissipation is permitted, because
– the junction does not have time to heat up fully unless the pulses are so long as to approximate steady-state conditions;
– the junction has time wholly or partly to cool down in the interval between pulses, except with very high duty factors.

Analogy with

$$P_{tot} = \frac{T_j - T_{mb}}{R_{th\,j\text{-}mb}}$$

yields

$$P_{tot\,M} = \frac{T_j - T_{mb}}{Z_{th\,j\text{-}mb}}$$

where $P_{tot\,M}$ is the total pulsed power and $Z_{th\,j\text{-}mb}$ is the thermal impedance between junction and mounting base. Thermal impedance depends on pulse duration t_p and duty factor $\delta = t_p/T$. T is the pulse period. A family of curves of thermal impedance against pulse duration with duty factor as parameter is shown in Fig. 3.

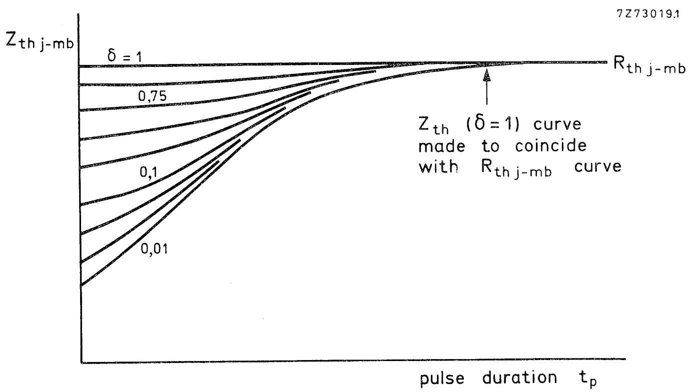


Fig. 3 A typical family of $Z_{th\,j\text{-}mb}$ curves for a power transistor.

Similar limitations apply as in the steady-state conditions:

(a) When $T_{mb} \leqslant T_{mb\,spec}$

$$P_{tot\,M\,max} = \frac{T_{j\text{-}mb\,max}}{Z_{th\,j\text{-}mb}}$$

(b) When $T_{mb} > T_{mb\,spec}$

$$P_{tot\,M\,max} = \frac{T_{j\,max} - T_{mb}}{Z_{th\,j\text{-}mb}}.$$

In essence, at or below $T_{mb\,spec}$ there is a fixed limit to $P_{tot\,M\,max}$; above $T_{mb\,spec}$, $P_{tot\,M\,max}$ declines linearly with increasing mounting base temperature. As illustrated in Fig. 4, for non-rectangular pulses

$$P_{tot\,max} \cdot t_p = \int_{t_1}^{t_2} P \cdot t_p.$$

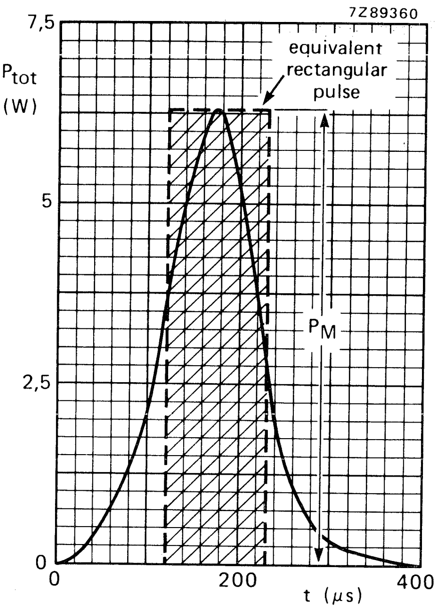


Fig. 4.

Second breakdown

In the forward-biased condition second breakdown is thermally triggered. Consider the chip as a large number of elemental transistors in parallel, some of which will have a lower forward voltage drop than others. Current will tend to concentrate in these, raising their temperature and further lowering their forward voltage drop. Current will concentrate still further, leading to local overheating and eventually to a short circuit between emitter and collector. This effect is independent of mounting base temperature, which is related to the average junction temperature. Under reverse-bias conditions, when V_{CE} is greater than V_{CEOmax}, the chance of second breakdown is always present. This is a particular hazard in timebase and converter applications.

THE SOAR BOUNDARIES

The four limits just described form the boundaries of the Safe Operating ARea. Figure 5 shows a SOAR plotted on a log-log grid. The right-hand boundary is formed by V_{CEOmax}, which extends up to a collector current of about 300 mA. Above this point, as I_C is increased V_{CE} must be reduced to prevent second breakdown.

The upper boundary is formed by I_{Cmax}, which extends to where the product of I_{Cmax} and V_{CE} equals the maximum allowable power dissipation. From this point I_C must be reduced with increasing V_{CE}, thus forming the maximum power dissipation boundary. The maximum power dissipation boundary normally intersects the second breakdown boundary at some point. However, for values of T_{mb} above $T_{mb\,spec}$, $P_{tot\,max}$ must be reduced (as shown by the broken line in Fig. 5), so that the boundary of maximum power dissipation intersects the second breakdown boundary at a lower point. With high values of T_{mb}, the second breakdown boundary may be excluded altogether.

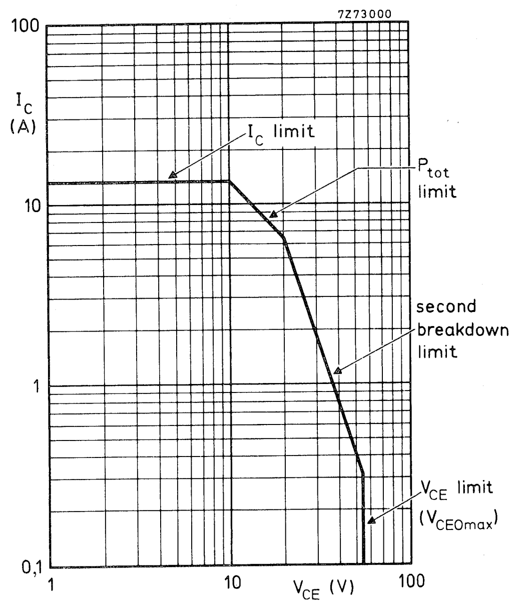


Fig. 5 A typical SOAR graph with boundaries named.

EXTENDING THE SOAR FOR SINGLE-SHOT AND REPETITIVE PULSED OPERATION

The data sheets for power transistors contain, apart from the d.c. SOAR, a set of curves that apply under specific pulse conditions. These will cover some 90% of applications. In addition to these, SOAR curves can be constructed by the circuit designer for specific operating conditions. The various extensions dealt with below will refer to Figs 5, 6 and 8.

I_{CMmax}

The extent to which the I_C boundary can be extended for pulse operation depends on pulse duration and duty factor, the limit being I_{CMmax}, which applies at a duty factor of 0,01 and a pulse length of 20 ms or less. Together the I_{CMmax} and V_{CEOmax} boundaries form a rectangle that in no circumstance should be exceeded. Moreover, the rectangle may be reduced by further restrictions imposed by power dissipation and second breakdown. The example shown in Fig. 6 is for an I_{CMmax} of 12 A and a V_{CEOmax} of 60 V.

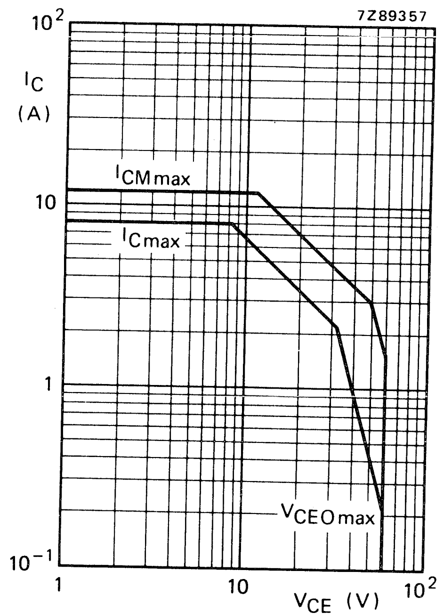


Fig. 6 Maximum collector current and collector-emitter voltage boundaries.

$P_{tot\,max}$

The $P_{tot\ max}$ boundary given in the data sheet usually applies to:

T_{mb} = 25 °C; δ = 0,01 and t_p = a range of values, say, 5 μs to 2 ms.

For any deviations from these values a new $P_{tot\ max}$ boundary must be constructed.
From

$$P_{tot\,M\,max} = \frac{T_{j\,max} - T_{mb}}{Z_{th\ j\text{-}mb}};$$

$T_{j\ max}$ is stated in the data sheets; $Z_{th\ j\text{-}mb}$ can be read from the curve, similar to Fig. 3, also given in the data sheets. Thus $P_{tot\,M\,max}$ can be calculated and an appropriate boundary can be drawn in the SOAR curve parallel to the $P_{tot\ max}$ line. An example will illustrate this. Assume:

$T_{j\ max}$ = 150 °C; $T_{mb\ spec}$ = 25 °C; t_p = 0,2 ms and δ = 0,1.

From Fig. 7, $Z_{th\ j\text{-}mb}$ = 0,42 K/W for the given values of t_p and δ.

$$P_{tot\,M\,max} = \frac{150 - 80}{0,42} = 166\ \text{W}.$$

Thus from an arbitary point (say 8,3 A, 20 V) we can draw a line parallel to the $P_{tot\ max}$ line (see Fig. 6).

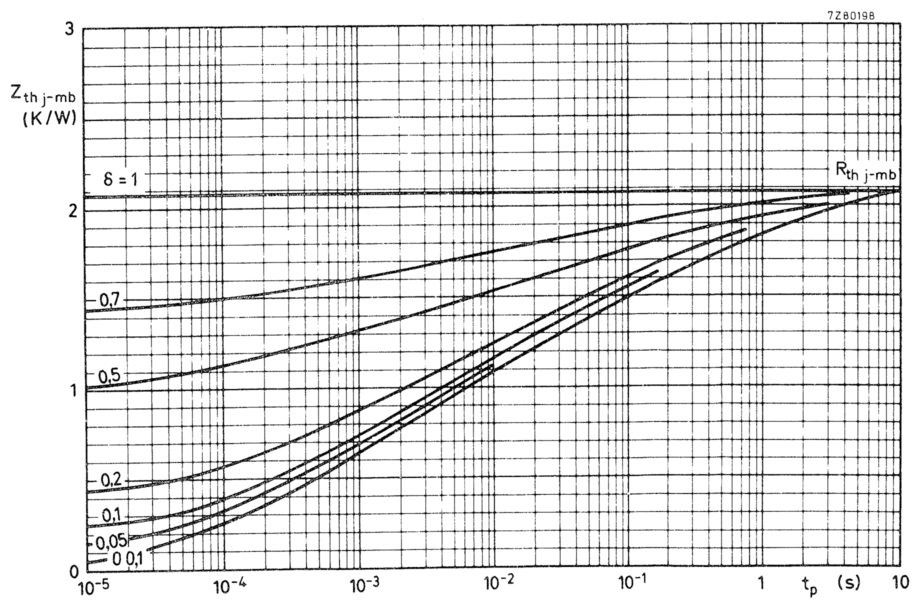


Fig. 7 Transient thermal impedance for example.

Second breakdown

The permissible extension to the second breakdown boundary is found with the aid of two multiplying factors:

M_V – the voltage multiplying factor
M_I – the current multiplying factors.*

Curves for these two factors are given in the data sheets as functions of pulse time with duty factor as parameter (see Fig. 8).

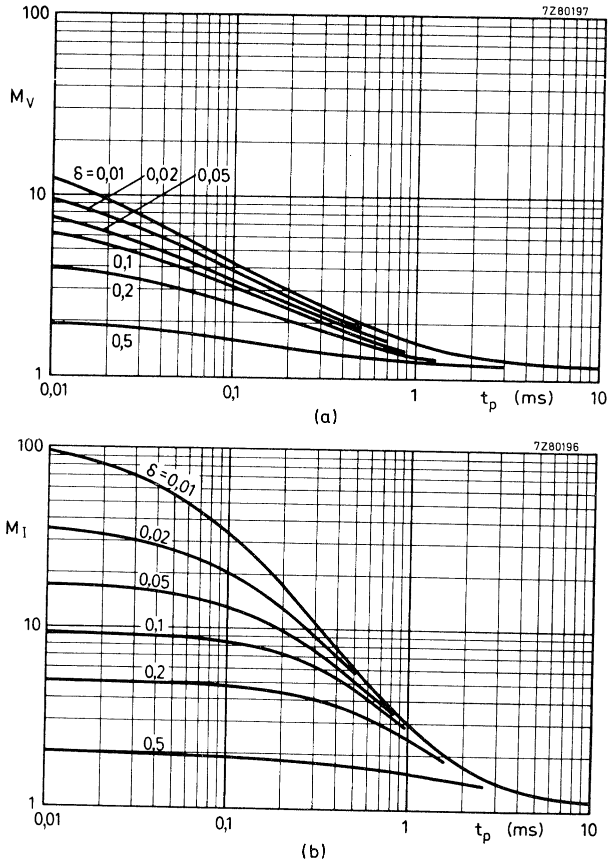


Fig. 8 Second breakdown multiplying factors as a function of pulse time, with duty factor as a parameter.

M_V is used to calculate the point on the V_{CEOmax} boundary at which voltage derating must commence as I_C increases. Similarly, M_I is used to calculate the point on the I_{CMmax} line at which current derating must commence as V_{CE} increases.

* Prior to 1973 M_V was known as $M_{SB(I)}$ and M_I as $M_{SB(V)}$.

Referring to Fig. 9, where B is the point on the V_{CEOmax} boundary at which voltage derating commences, B′ can be calculated by:

$I_{C(B')} = I_{C(B)} \times M_I$.

Similarly for I_C; although here A, the point on the I_C curve at which current derating commences, is first determined by extending the second breakdown boundary to where the two would intersect if $P_{tot\,max}$ did not intervene. A′ is then given by

$V_{CA(S')} = V_{CE(A)} \times M_V$.

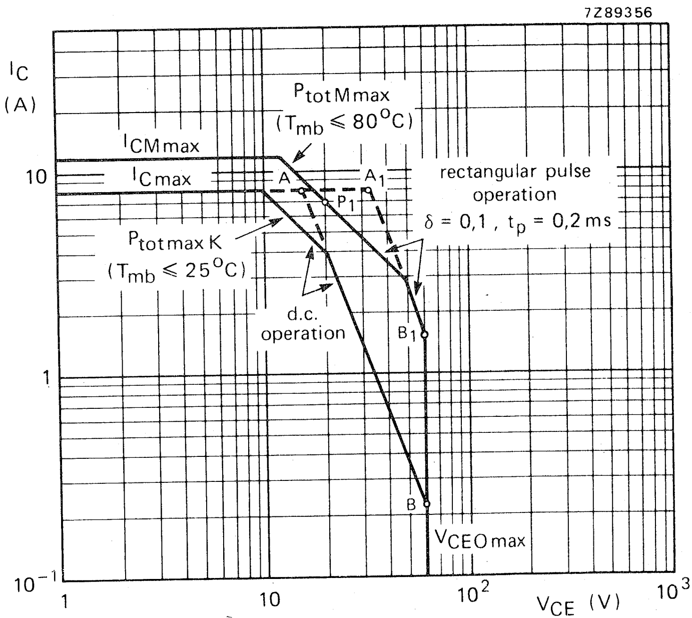


Fig. 9 Construction of the pulse operating area.

An example is worked in Fig. 9 for t_p = 0,2 ms and δ = 0,1.
From Fig. 8, M_V = 2,4 and M_I = 7,3:

$I_{C(B')}$ = 0,22 x 7,3 = 1,6 A
$V_{CE(A')}$ = 13 x 2,4 = 31 V.

These two points are then joined as in Fig. 9.

PULSE TRAINS AND COMPOSITE WAVEFORMS

Straightforward techniques exist for calculating the thermal and second breakdown effects of pulse trains and composite waveforms.

Thermal considerations

Consider a train of rectangular pulses as shown in Fig. 10. The junction will alternately heat and partly cool until a steady-state temperature is reached as shown in the lower part of Fig. 10. To approximate the final junction temperature only the effects of the first two or three pulses need be considered.

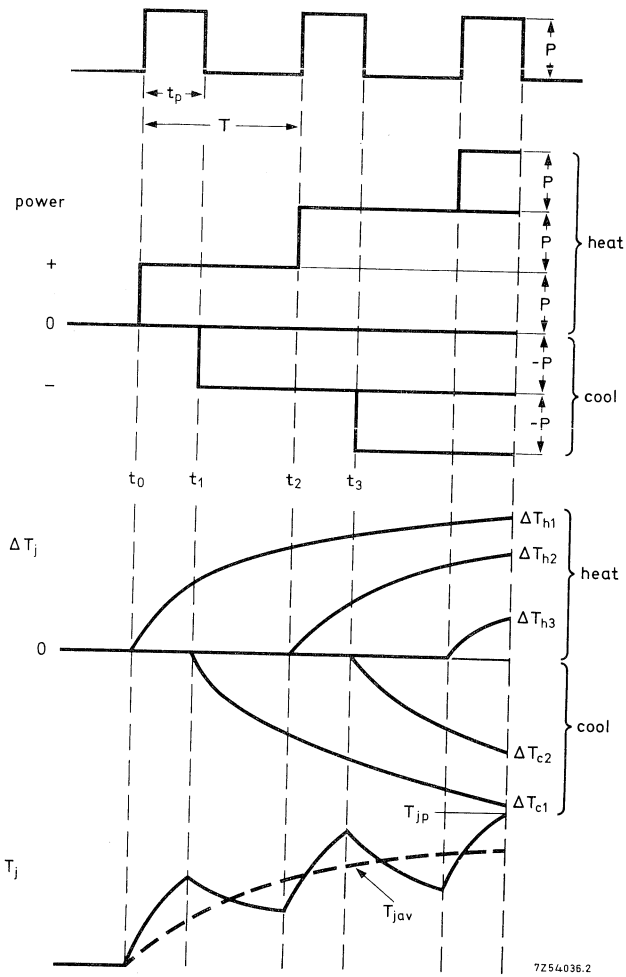


Fig. 10 The heating effect of three equidistant, equal-magnitude pulses. $T_{j\,av}$ is the average junction temperature. P = 100 W, t_p = 100 μs; T = 1 ms and δ = 0,1.

Referring to Fig. 10, where P = 100 W, t_p = 100 μs and δ = 0,1, the first pulse causes the junction to heat up; at the end of the pulse it starts to cool down until the second pulse recommences the heating cycle. We can replace the first pulse with a *continuous* heating pulse at t_0 and a *continuous* cooling pulse starting at t_1. Similarly for the second pulse, we can superimpose a continuous heating pulse starting at t_2 and a cooling pulse starting at t_3. Repeating this for successive pulses allows us to calculate T_j for any point in the pulse train. For instance, the cumulative change in junction temperature at the end of the third pulse is:

$$\Delta T_j = \Delta T_{h1} - \Delta T_{c1} + \Delta T_{h2} - \Delta T_{c2} + \Delta T_{h3},$$

where the subscripts h and c refer to heating and cooling respectively. With times taken from Fig. 10,

$T_{h1} = PZ_{th}(2{,}1\ \text{ms})$

$T_{h2} = PZ_{th}(1{,}1\ \text{ms})$

$T_{h3} = PZ_{th}(0{,}1\ \text{ms})$

and

$T_{c1} = -PZ_{th}(2{,}0\ \text{ms})$

$T_{c2} = -PZ_{th}(1{,}0\ \text{ms})$

Taking values for Z_{th} from Fig. 11 we get

$$\Delta T_j = 100(0{,}58 - 0{,}56 + 0{,}51 - 0{,}51 + 0{,}32) = 34\ ^{\circ}\text{C}.$$

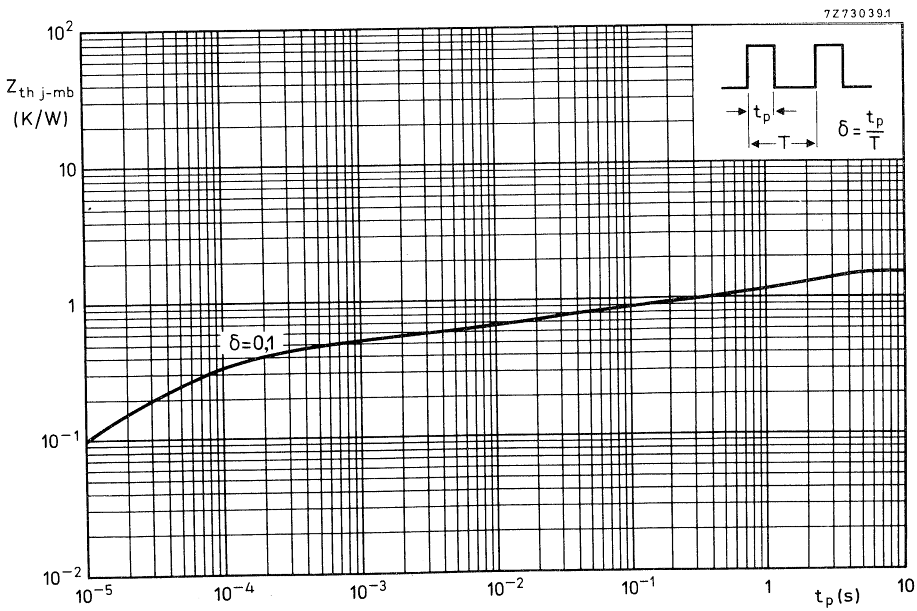


Fig. 11 Curve of $Z_{th\ j\text{-}mb} = f(t_p)$.

The same procedure can be used for long or continuous pulse trains, but calculating for a large number of pulses is very tedious. A sufficiently close approximation can be made by calculating for two pulses, assuming that the first is preceded by a continuous pulse of P_{av} as shown in Fig. 12. By this method

$$\Delta T_j = \Delta T_{h\,av} + \Delta T_{h1} - \Delta T_{c1} + \Delta T_{h2}.$$

The calculations are then made as before. To remove any doubt as to the closeness of the approximation the effect of a third pulse can be calculated. Composite waveforms can be treated similarly: divide the composite waveform into equivalent rectangular pulses and calculate the junction temperature accordingly.

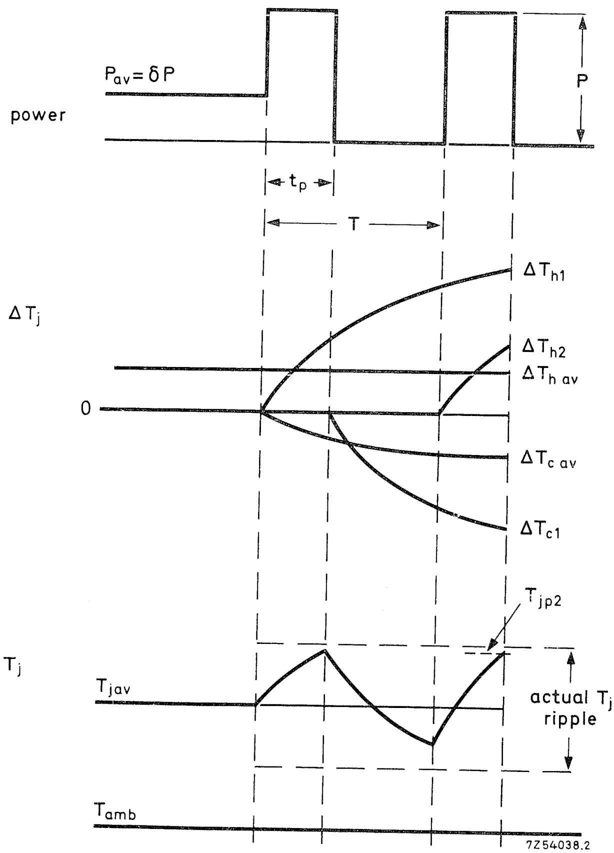


Fig. 12.

Figure 13 shows the current, voltage and power waveforms of the out put transistor in a television receiver vertical output stage. P_{tot} has been divided into four equivalent rectangular parts having the same peak values and energy content as the original waveform.

$$P_{tot\,av} = P_1\delta_1 + P_2\delta_2 + P_3\delta_3 + P_4\delta_4$$
$$= (16 \times 0{,}003) + (13 \times 0{,}11) +$$
$$+ (5{,}2 \times 0{,}66) + (40 \times 0{,}0007)$$
$$= 4{,}936 \text{ W}.$$

Assuming that the $R_{th\ j\text{-}mb}$ for the transistor is 2,5 K/W, the average rise in mounting base temperature will be about 12,5 °C.

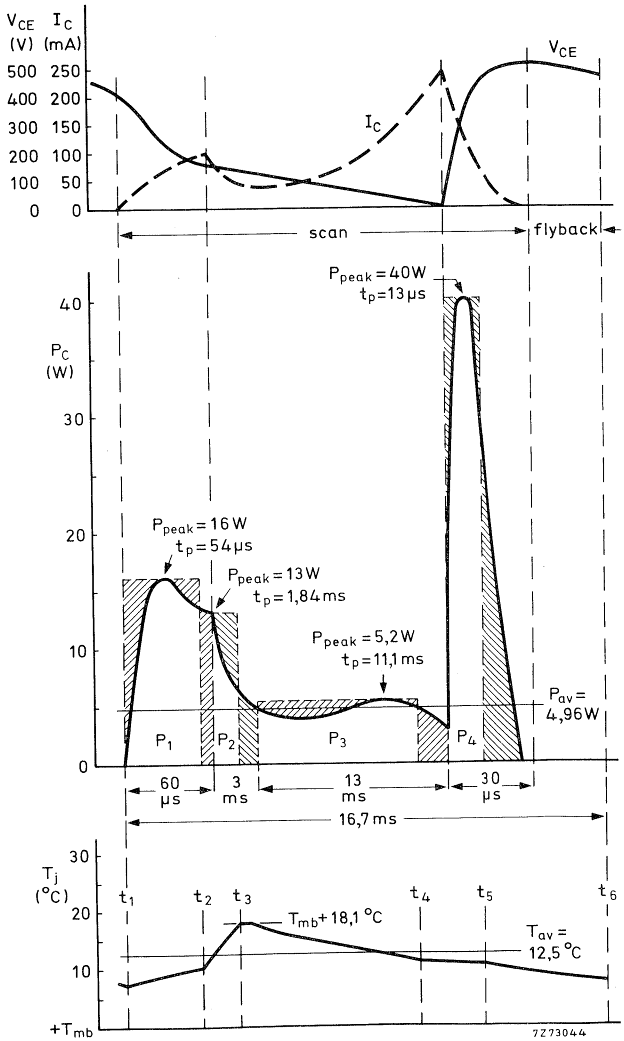


Fig. 13 Power waveforms showing their division into rectangular pulses and the junction temperature variations which they cause.

Using the same method as for pulse trains, peak temperatures at the end of each pulse can be calculated by

$$T_{j\text{-}mb(t1)} = P_{av}R_{th\,j\text{-}mb} - P_{av}Z_{th\,j\text{-}mb(16,1\text{ ms})} + P_1Z_{th(16,1\text{ ms})}.$$

For the temperature at the end of the second pulse (t_2) two further terms are added:

$$-P_1Z_{th(16,04\text{ ms})} + P_2Z_{th(16,04\text{ ms})}.$$

For t_3 yet another two terms:

$$-P_3Z_{th(13,02\text{ ms})} + P_4Z_{th(13,03\text{ ms})}.$$

For each successive pulse a negative term (end of the previous pulse) and a positive term (start of the succeeding pulse) are added. Calculated temperatures are shown in Table 1: note that the highest temperature is reached at the end of pulse 2 (t_3). Even assuming a T_{mb} of 100 °C, T_j will remain within the $T_{j\,max}$ of 150 °C specified for this transistor.

TABLE 1 Calculated temperatures for the power waveform of Fig. 13.

time	t_1	t_2	t_3	t_4	t_5	$t_6(t_s)$	
$\Delta T_{j\text{-}mb}$	8,54	11,34	18,1	12,76	12,3	8,54	°C

EXAMPLE OF A SOAR CALCULATION

To illustrate the foregoing we will take the example of a BU426A transistor operating in a 200 W switched-mode power supply (SMPS).

Waveforms of collector current, collector-emitter voltage and power dissipation are shown in Figs 14, 15 and 16. These are translated into an equivalent rectangular pulse train in Fig. 17. This will enable us to calculate peak junction temperature at any instant.

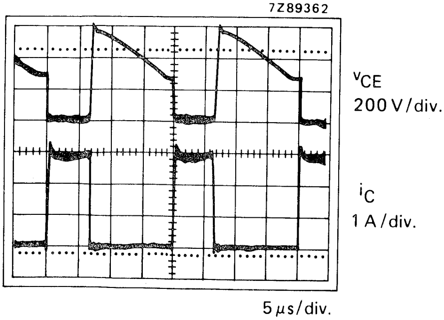


Fig. 14 Collector-current and collector-emitter voltage waveforms of a BU426A transistor in a 200 W SMPS.

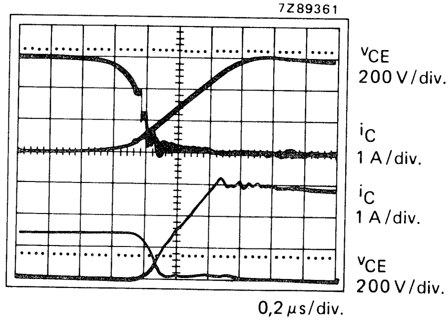


Fig. 15 Waveforms during turn-on and turn-off (lower part).

The duration of this equivalent pulse train is then given by

$$t_p' = \frac{P_{tot\,av} \times T}{P'_M} \text{ and } \delta' = \frac{t'_p}{T}.$$

First, from Fig. 17, heating and cooling pulses are plotted as in Fig. 18. Parameters are then tabulated as shown:

$P_{turn\text{-}on}$	= 66 W	P_{sat}	= 10 W	$P_{turn\text{-}off}$	= 56 W
$t_{p\,on}$	= 0,8 μs	$t_{p\,sat}$	= 2,2 μs	$t_{p\,off}$	= 0,6 μs
δ_{on}	= 0,04	δ_{sat}	= 0,11	δ_{off}	= 0,03

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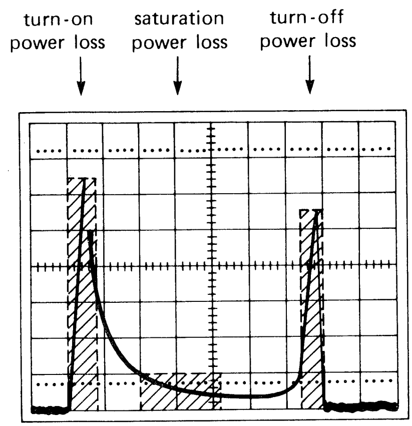


Fig. 16 Power loss and resultant rectangular power pulses.

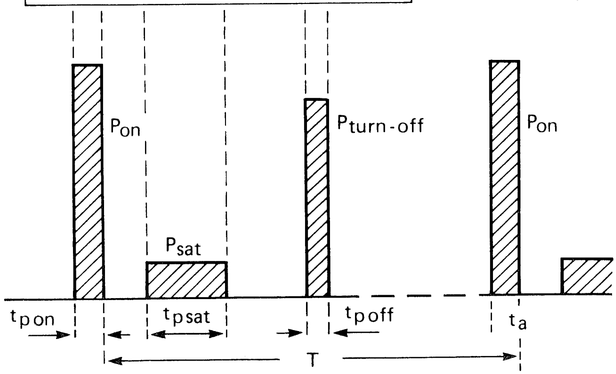


Fig. 17.

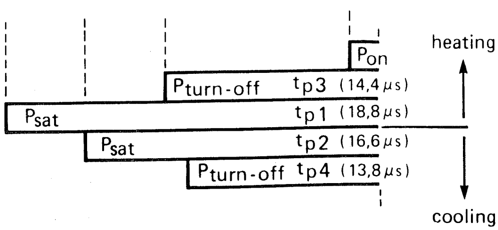


Fig. 18.

From Fig. 17 we can determine δ_p and t_p for each condition and from the BU426 data sheets the relevant Z_{th}.

	p1	p2	p3	p4	p5	unit
t	18,8	16,6	14,4	13,8	0,8	μs
δ	0,94	0,83	0,72	0,7	0,04	
Z_{th}	1,05	0,95	0,85	0,8	0,06	K/W

From

$$\Delta T_j = \Delta T_{h1} - \Delta T_{c1} + \Delta T_{h2} - \Delta T_{c2} + \Delta T_{h3}$$

$$\Delta T_{j\text{-}mb(ta)} = (P_{sat} \times Z_{th(tp1)}) - (P_{sat} \times Z_{th(tp2)}) +$$
$$+ (P_{turn\text{-}off} \times Z_{th(tp3)}) - (P_{turn\text{-}off} \times Z_{th(tp4)}) + (P_{on} \times Z_{th(tp\,on)})$$

$$\Delta T_{j\text{-}mb(ta)} = 10(1,05 - 0,95) + 56(0,83 - 0,8) + 66(0,06) = 7,76\text{ K.}$$

Thus, at time t_a the peak junction temperature is 7,76 K higher than the average mounting base temperature. The $\Delta T_{j\text{-}mb}$ arising from the other power pulses can be calculated in the same way.

Average mounting base temperature depends on the size of the heatsink, ambient temperature (T_a) and average dissipation.

From

$$P_{tot\,av} = P_1\delta_1 + P_2\delta_2 + P_3\delta_3 + P_4\delta_4$$

$$P_{tot\,av} = \delta_{on} \times P_{on} + \delta_{sat} \times P_{sat} + \delta_{turn\text{-}off} \times P_{off}$$

$$= 0,04 \times 66 + 0,11 \times 10 + 0,03 \times 56 = 5,4\text{ W.}$$

Assuming a maximum mounting base temperature of 100 °C and an ambient temperature of 60 °C the thermal resistance of the heatsink required will be

$$R_{th\,mb\text{-}a} = \frac{T_{mb} - T_a}{P_{tot\,av}} = \frac{100 - 60}{5,4} = 7,4\text{ K/W.}$$

If this is the case, the peak junction temperature at the end of the turn-on power pulse will be 107,76 °C, which is well within the maximum allowable junction temperature of 150 °C.

The pulse SOAR can be calculated using M_I, M_V and Z_{th} factors as described earlier. The turn-on, saturation and turn-off power pulses should be combined into a single pulse of amplitude P′ equal to the highest amplitude power pulse (here, P_{on}) and duration t'_p.

$$P_{tot\,av} = P' = 66\text{ W.}$$

$$\delta' = \frac{5,4}{66} = 0,082.$$

$$t'_p + \delta' T = 1,64\,\mu s.$$

From the BU426A data, for this power pulse $Z_{th\,j\text{-}mb} = 0,10$ K/W; $M_I \approx 12$; $M_V \approx 7,5$; $V_{CE(A')} = 7,5 \times 12 = 90$ V; $I_{C(B')} = 12 \times 40 = 480$ mA.

$$P_{tot\,max} = \frac{T_j - T_{mb}}{Z_{th\,j\text{-}mb}} = \frac{150 - 100}{0,1} = 500\ W.$$

The relevant pulse SOAR is shown in Fig. 19, in which the operating point for the full cycle has also been plotted. It can be seen that it remains well within the SOAR.

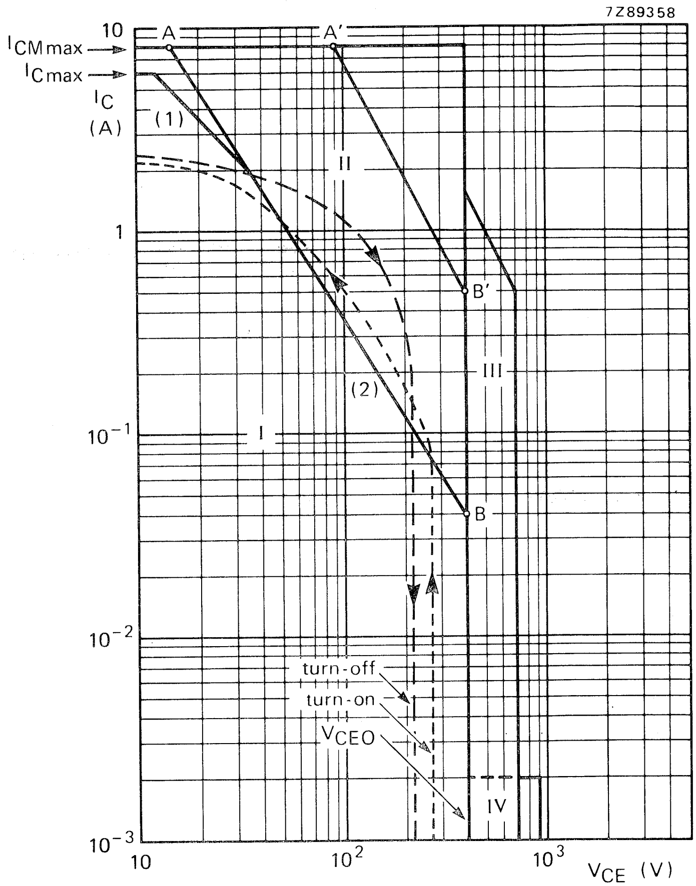


Fig. 19 Safe Operating ARea BU426A at $T_{mb} \leqslant 73\ ^oC$.

I Region of permissible d.c. operation.

II Permissible extension for repetitive pulse operation.

III Area of permissible operation during turn-on in single-transistor converters, provided $R_{BE} \leqslant 100\ \Omega$ and $t_p \leqslant 0,6\ \mu s$.

IV Repetitive pulse operation in this region is permissible, provided $V_{BE} \leqslant 0$ and $t_p \leqslant 2$ ms.

(1) $P_{tot\,max}$ and $P_{peak\,max}$ lines.

(2) Second-breakdown limits (independent of temperature).

TRANSISTOR DATA

HIGH–VOLTAGE TRANSISTOR

Silicon n-p-n transistor in TO-126 plastic envelope intended for use as a driver for line output transistors in colour tv receivers.

QUICK REFERENCE DATA

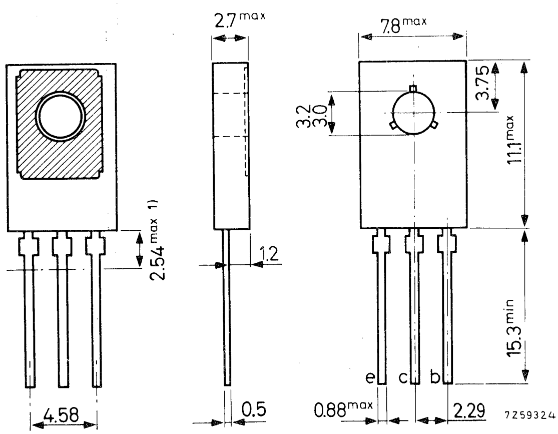
Collector-base voltage (open emitter)	V_{CBO}	max.	300	V
Collector-emitter voltage (open base)	V_{CEO}	max.	250	V
Collector current (peak value)	I_{CM}	max.	300	mA
Total power dissipation up to T_{mb} = 90 °C	P_{tot}	max.	6	W
Junction temperature	T_j	max.	150	°C
D.C. current gain I_C = 20 mA; V_{CE} = 10 V	h_{FE}	typ.	45	
Storage time	t_s	typ.	0.5	μs

MECHANICAL DATA

Dimensions in mm

Fig.1 TO-126 (SOT-32)

Collector connected to mounting base



(1) Within this region the cross-section of the leads is uncontrolled

See also chapters Mounting Instructions and Accessories.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-base voltage (open emitter)	V_{CBO}	max.	300	V
Collector-emitter voltage ($R_{BE} \leq 1$ kΩ)	V_{CER}	max.	300	V
Collector-emitter voltage (open base)	V_{CEO}	max.	250	V
Emitter-base voltage (open collector)	V_{EBO}	max.	5	V
Collector current (continuous)	I_C	max.	100	mA
Collector current (peak value) *	I_{CM}	max.	300	mA
Total power dissipation up to T_{mb} = 90 °C	P_{tot}	max.	6	W
up to T_{amb} = 70 °C	P_{tot}	max.	0.8	W
Storage temperature	T_{stg}		−65 to +150	°C
Operating junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	10	K/W
From junction to ambient	$R_{th\ j\text{-}a}$	=	100	K/W

* Precautions should be taken during switch-on of the BF419 where an overshoot of current is likely to occur. The amplitude of the overshoot depends on the relative magnitude of stray external capacities to the transistor collector capacity. It is desirable to keep the stray capacities to a minimum by short lead lengths etc. so as to minimise the area of the switching path.

CHARACTERISTICS

$T_j = 25\ ^oC$

Collector cut-off current $I_E = 0; V_{CB} = 250\ V$	I_{CBO}	<	50	nA
Emitter cut-off current $I_C = 0; V_{EB} = 3\ V$	I_{EBO}	<	50	nA
D.C. current gain $I_C = 20\ mA; V_{CE} = 10\ V$	h_{FE}	typ.	45	
Collector-emitter saturation voltage $I_C = 200\ mA; I_B = 20\ mA$ *	V_{CEsat}	<	11	V
Collector output capacitance at f = 1 MHz $I_E = 0; V_{CB} = 30\ V$	C_{Tc}	<	4.5	pF
Storage time (in the typical circuit below)	t_s	typ.	0.5	μs

* The BF419 is controlled to V_{CEsat} max. 11.0 V and is thermally stable under all operating conditions where T_j max of 150 °C is not exceeded. For the typical circuit shown below, a heatsink is not required for operation with $T_{amb} \leqslant 70\ ^oC$.

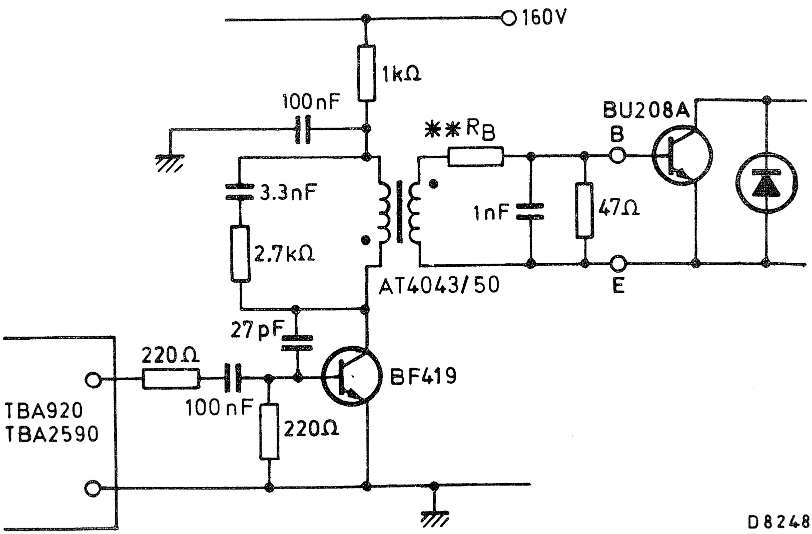


Fig.2 Typical circuit.

** R_B is chosen so that the end-of-scan base current for the BU208A is 1.4 A under nominal conditions. Typical value of R_B is 0.5 Ω plus 0.1 Ω lead resistance.

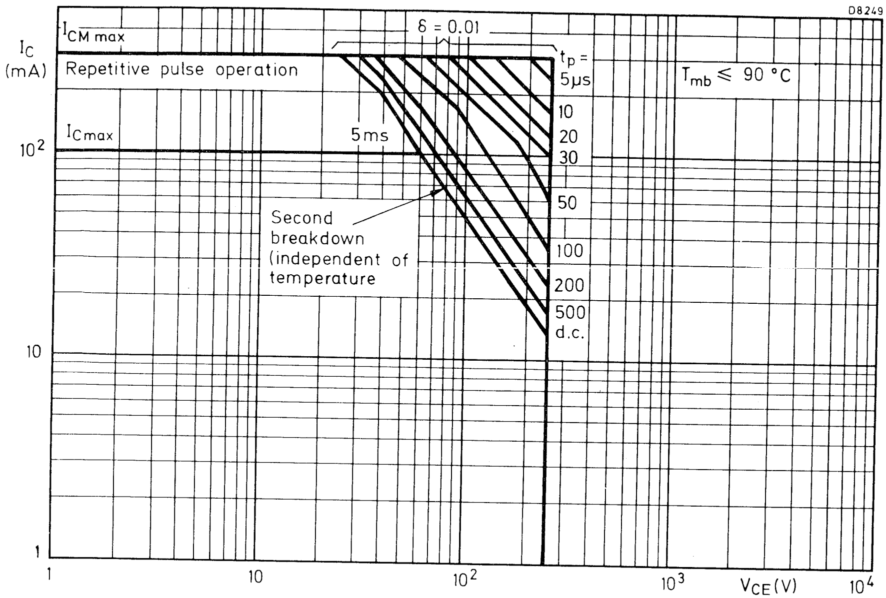


Fig.3 Safe Operating AReas with the transistor forward biased.

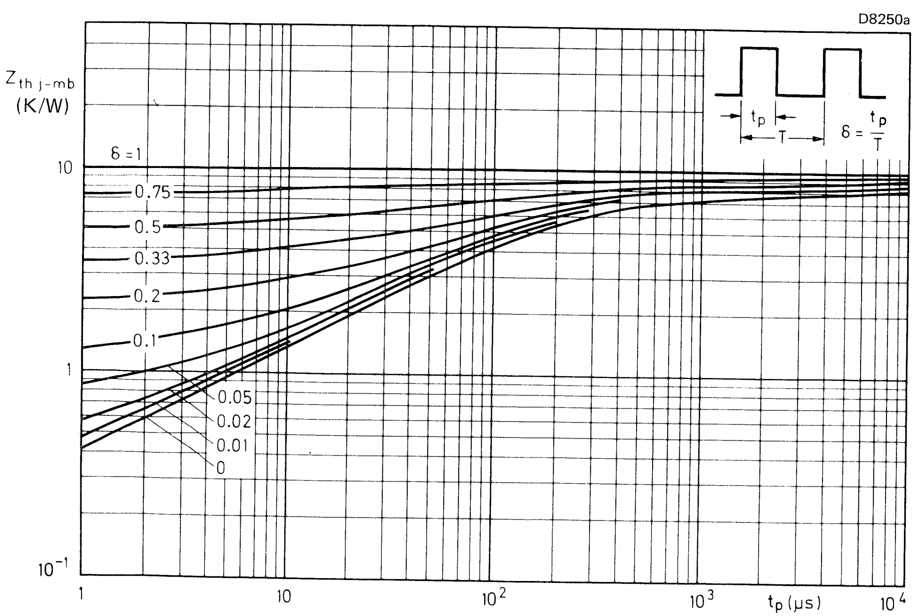


Fig. 4.

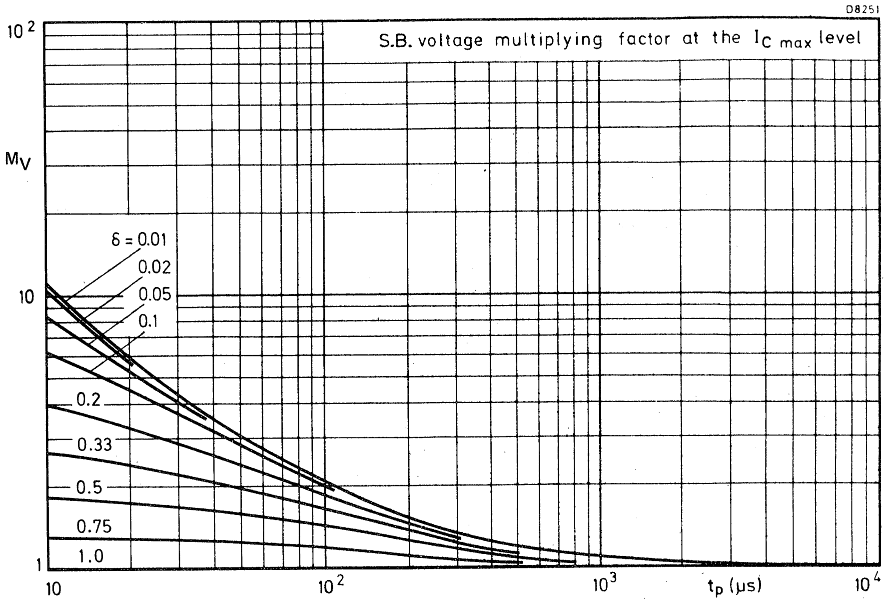

D8251
S.B. voltage multiplying factor at the $I_{C\,max}$ level
10^2
M_V
δ = 0.01
0.02
0.05
0.1
10
0.2
0.33
0.5
0.75
1.0
1
10
10^2
10^3
t_p (μs)
10^4

Fig. 5.

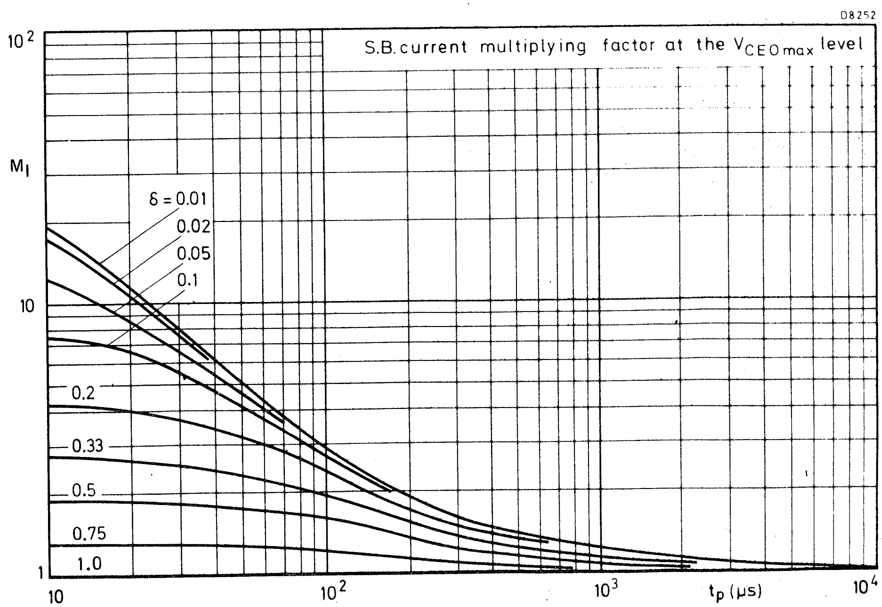

D8252
S.B. current multiplying factor at the $V_{CEO\,max}$ level
10^2
M_I
δ = 0.01
0.02
0.05
0.1
10
0.2
0.33
0.5
0.75
1.0
1
10
10^2
10^3
t_p (μs)
10^4

Fig. 6.

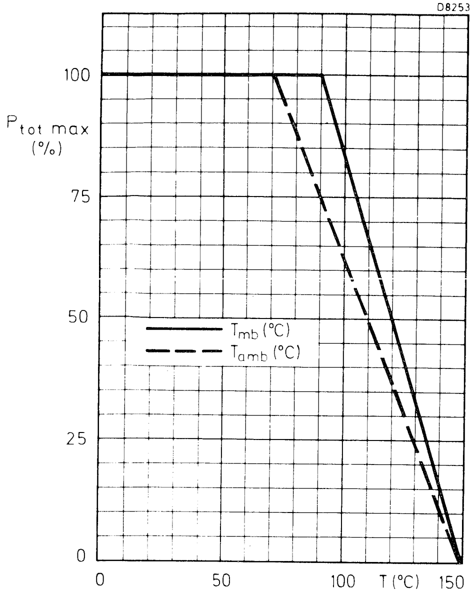


Fig. 7.

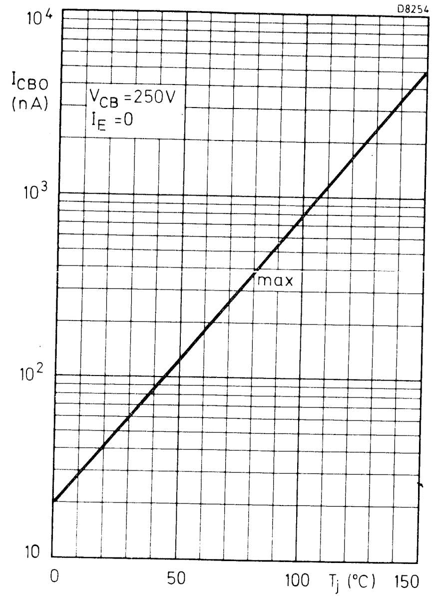


Fig. 8.

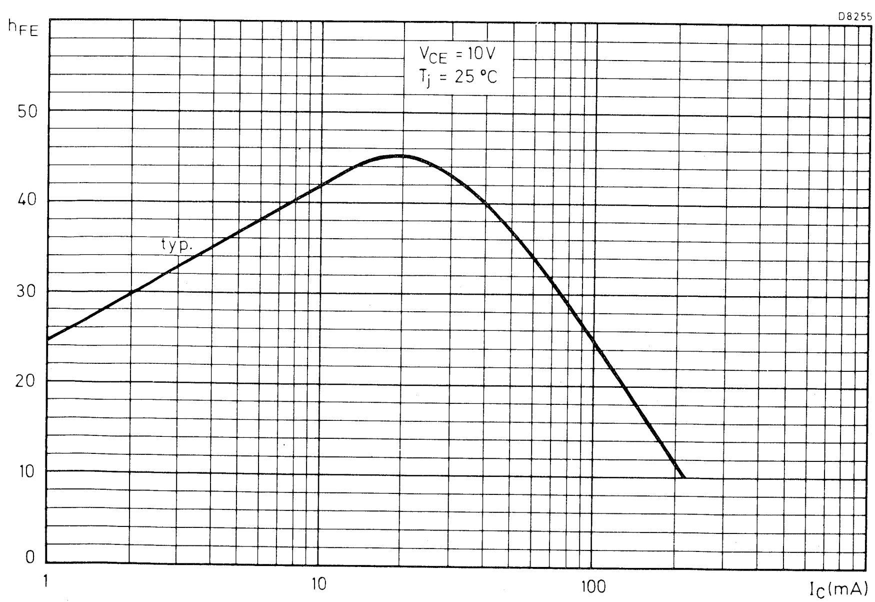


Fig. 9.

SILICON PLANAR TRANSISTORS

for video output stages

N-P-N transistors in a SOT-32 plastic envelope intended for video output stages in black-and-white and in colour television receivers.

QUICK REFERENCE DATA

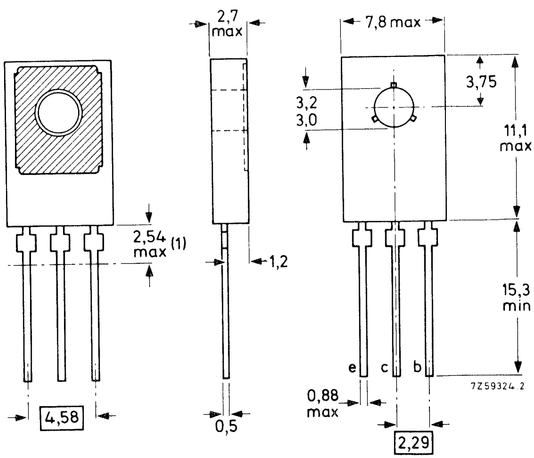
			BF457	BF458	BF459	
Collector-base voltage (open emitter)	V_{CBO}	max.	160	250	300	V
Collector-emitter voltage (open base)	V_{CEO}	max.	160	250	300	V
Collector current (peak value)	I_{CM}	max.		300		mA
Total power dissipation up to T_{mb} = 90 °C	P_{tot}	max.		6		W
Junction temperature	T_j	max.		150		°C
D.C. current gain at T_j = 25 °C I_C = 30 mA; V_{CE} = 10 V	h_{FE}	>		26		
Transition frequency I_C = 15 mA; V_{CE} = 10 V	f_T	typ.		90		MHz
Feedback capacitance at f = 1 MHz I_E = 0; V_{CB} = 30 V	C_{re}	<		3,5		pF

MECHANICAL DATA

Dimensions in mm

Collector connected to metal part of mounting surface

TO-126 (SOT-32)



(1) Within this region the cross-section of the leads is uncontrolled.

See also chapters Mounting instructions and Accessories.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltage

			BF457	BF458	BF459	
Collector-base voltage (open emitter)	V_{CBO}	max.	160	250	300	V
Collector-emitter voltage (open base)	V_{CEO}	max.	160	250	300	V
Emitter-base voltage (open collector)	V_{EBO}	max.	5	5	5	V

Current

Collector current (d.c.)	I_C	max.	100	mA
Collector current (peak value)	I_{CM}	max.	300	mA
Base current (d.c.)	I_B	max.	50	mA

Power dissipation

Total power dissipation up to T_{mb} = 90 °C	P_{tot}	max.	6	W

Temperature

Storage temperature	T_{stg}		−55 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

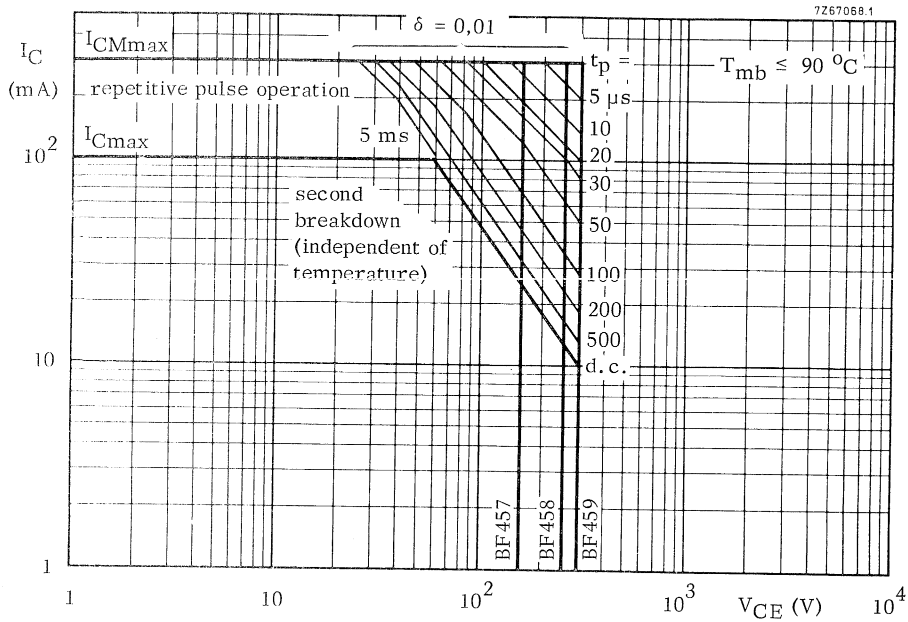
From junction to ambient	$R_{th\ j-a}$	=	104	K/W
From junction to mounting base	$R_{th\ j-mb}$	=	10	K/W

CHARACTERISTICS $T_j = 25\ ^oC$ unless otherwise specified

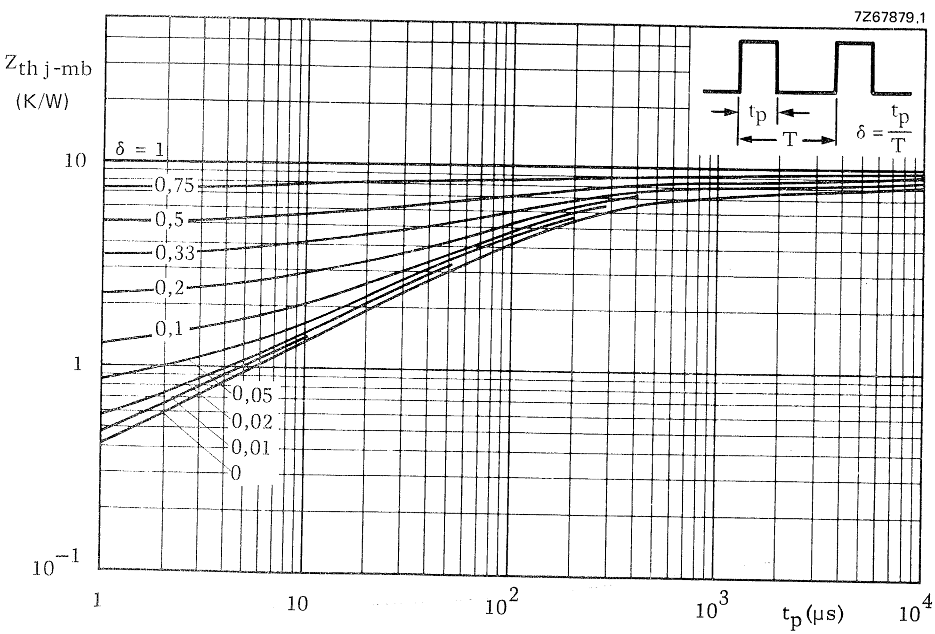
Collector cut-off current				
$I_E = 0$; $V_{CB} = 100$ V for BF457				
$I_E = 0$; $V_{CB} = 200$ V for BF458	I_{CBO}	<	50	nA
$I_E = 0$; $V_{CB} = 250$ V for BF459				
Emitter cut-off current				
$I_C = 0$; $V_{EB} = 3$ V	I_{EBO}	<	50	nA
D.C. current gain				
$I_C = 30$ mA; $V_{CE} = 10$ V	h_{FE}	>	26	
Collector-emitter saturation voltage				
$I_C = 30$ mA; $I_B = 6$ mA	V_{CEsat}	<	1	V
High frequency knee voltage at $T_j = 150\ ^oC$				
$I_C = 50$ mA	V_{CEK}	typ.	15	V

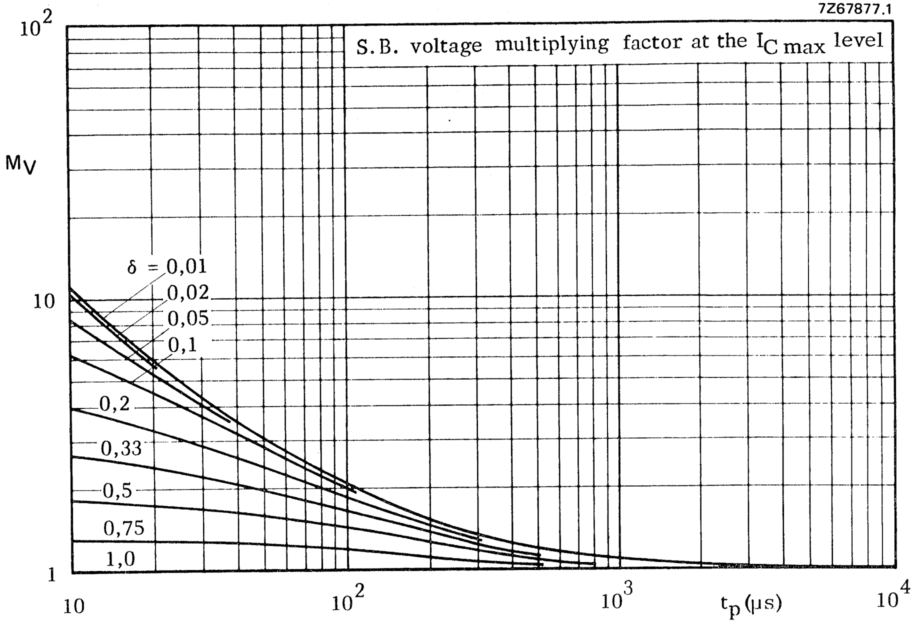
The high frequency knee voltage of a transistor is that value of the collector-emitter voltage at which the small signal gain, measured in a practical circuit, has dropped to 80% of the gain at $V_{CE} = 50$ V. A further reduction of the collector-emitter voltage results in a rapid increase of the distortion of the signal.

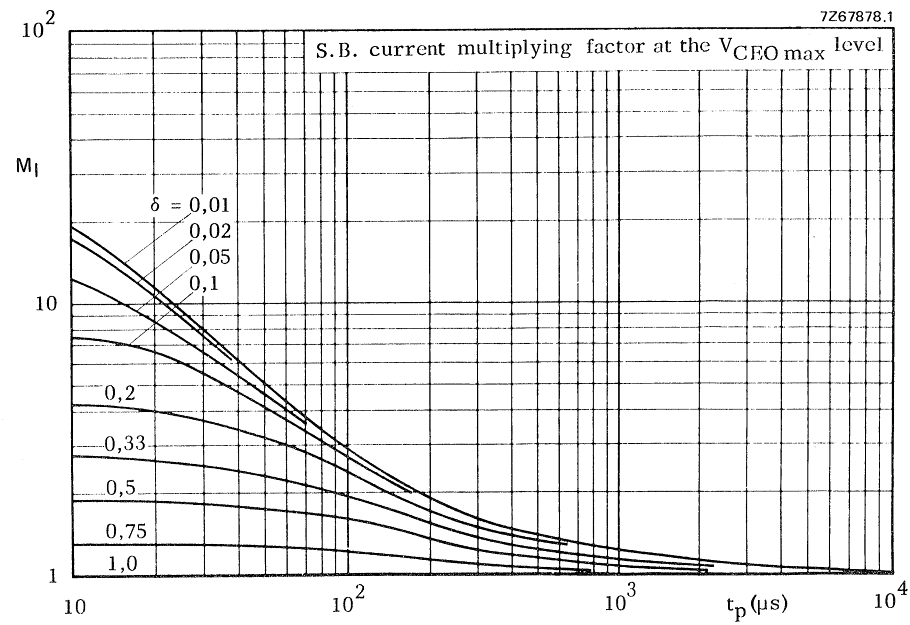
Transition frequency at f = 100 MHz				
$I_C = 15$ mA; $V_{CE} = 10$ V	f_T	typ.	90	MHz
Feedback capacitance at f = 1 MHz				
$I_E = 0$; $V_{CB} = 30$ V	C_{re}	<	3,5	pF
Output capacitance at f = 1 MHz				
$I_E = 0$; $V_{CB} = 30$ V	C_{oe}	<	4,5	pF

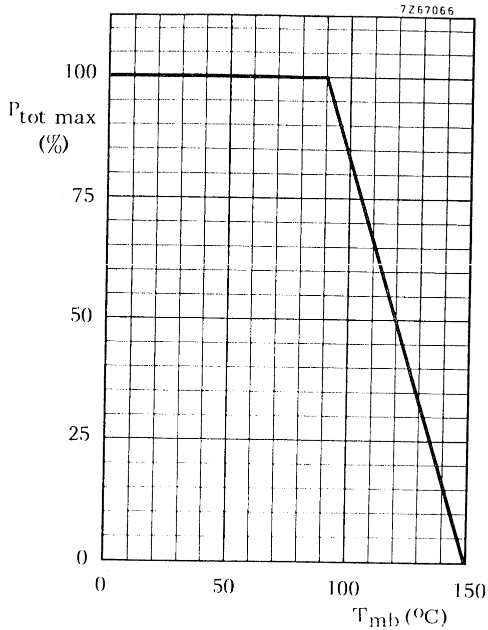


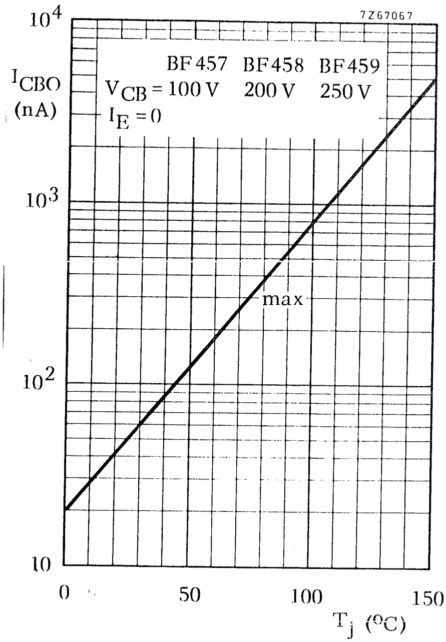
Safe Operating Area with the transistor forward biased




7Z67877.1
S.B. voltage multiplying factor at the $I_{C\,max}$ level
M_V
10^2
10
1
δ = 0,01
0,02
0,05
0,1
0,2
0,33
0,5
0,75
1,0
10
10^2
10^3
t_p (μs)
10^4


7Z67878.1
S.B. current multiplying factor at the $V_{CEO\,max}$ level
M_I
10^2
10
1
δ = 0,01
0,02
0,05
0,1
0,2
0,33
0,5
0,75
1,0
10
10^2
10^3
t_p (μs)
10^4


7Z67066
100
75
50
25
0
0
50
100
150
Ptot max (%)
Tmb (°C)


7Z67067
ICBO (nA)
BF457 BF458 BF459
VCB = 100 V 200 V 250 V
IE = 0
max
10
10^2
10^3
10^4
0
50
100
150
Tj (°C)

SILICON PLANAR EPITAXIAL TRANSISTORS

N-P-N transistors in plastic envelope intended for class-B video output stages in television receivers and for high-voltage i.f. output stages.
P-N-P complements are BF470 and BF472 respectively.

QUICK REFERENCE DATA

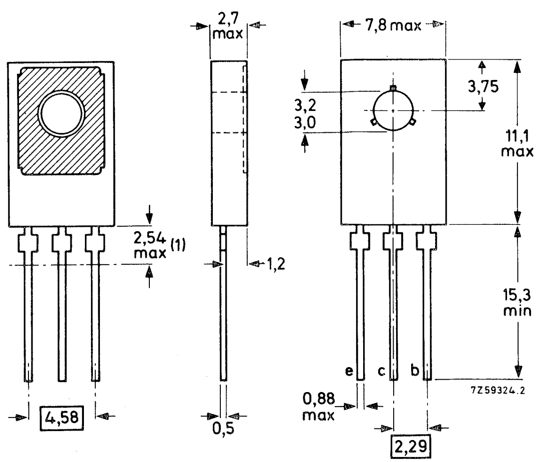
			BF469	BF471	
Collector-base voltage (open emitter)	V_{CBO}	max.	250	300	V
Collector-emitter voltage					
open base	V_{CEO}	max.	250	–	V
R_{BE} = 2,7 kΩ	V_{CER}	max.	–	300	V
Collector current (peak value)	I_{CM}	max.	100		mA
Total power dissipation up to $T_{mb} \leq 114$ °C	P_{tot}	max.	1,8		W
Junction temperature	T_j	max.	150		°C
D.C. current gain					
I_C = 25 mA; V_{CE} = 20 V	h_{FE}	>	50		
Transition frequency					
I_C = 10 mA; V_{CE} = 10 V	f_T	>	60		MHz
Feedback capacitance at f = 0,5 MHz					
I_E = 0; V_{CB} = 30 V	C_{re}	<	1,8		pF

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-126 (SOT-32).

Collector connected to mounting base



See also chapters Mounting instructions and Accessories.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BF469	BF471	
Collector-base voltage (open emitter)	V_{CBO}	max.	250	300	V
Collector-emitter voltage					
R_{BE} = 2,7 kΩ	V_{CER}	max.	–	300	V
open base	V_{CEO}	max.	250	–	V
Emitter-base voltage (open collector)	V_{EBO}	max.	5		V
Collector current (d.c.)	I_C	max.	50		mA
Collector current (peak value)	I_{CM}	max.	100		mA
Total power dissipation up to T_{mb} = 114 °C *	P_{tot}	max.	1,8		W
Storage temperature	T_{stg}		–65 to + 150		°C
Junction temperature	T_j	max.	150		°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	20	K/W
From junction to ambient in free air *	$R_{th\ j\text{-}a}$	=	100	K/W

* Transistor mounted on a printed-circuit board, maximum lead length 4 mm, mounting pad for collector lead minimum 10 mm x 10 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current				
I_E = 0; V_{CB} = 200 V	I_{CBO}	<	10	nA
R_{BE} = 2,7 kΩ; V_{CE} = 200 V; T_j = 150 °C	I_{CER}	<	10	μA
Emitter cut-off current				
I_C = 0; V_{EB} = 5 V	I_{EBO}	<	10	μA
D.C. current gain				
I_C = 25 mA; V_{CE} = 20 V	h_{FE}	>	50	
High-frequency knee voltage at T_j = 150 °C*				
I_C = 25 mA	V_{CEK}	typ.	20	V
Transistion frequency				
I_C = 10 mA; V_{CE} = 10 V	f_T	>	60	MHz
Feedback capacitance at f = 0,5 MHz				
I_E = 0; V_{CB} = 30 V	C_{re}	<	1,8	pF

* The high-frequency knee voltage of a transistor is that value of the collector-emitter voltage at which the small-signal gain, measured in a practical circuit, has dropped to 80% of the gain at V_{CE} = 50 V.
A further reduction of the collector-emitter voltage results in a rapid increase of the distortion of the signal.

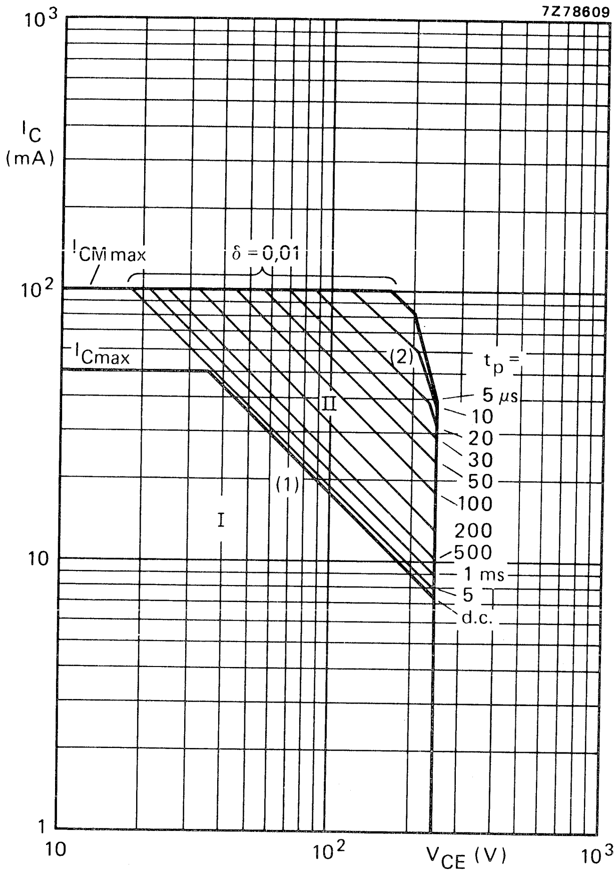


Fig. 2 Safe Operating ARea at T_{mb} = 114 °C.

I Region of permissible d.c. operation.

II Permissible extension for repetitive pulse operation.

(1) $P_{tot\,max}$ and $P_{peak\,max}$ lines.

(2) Second breakdown limits (independent of temperature).

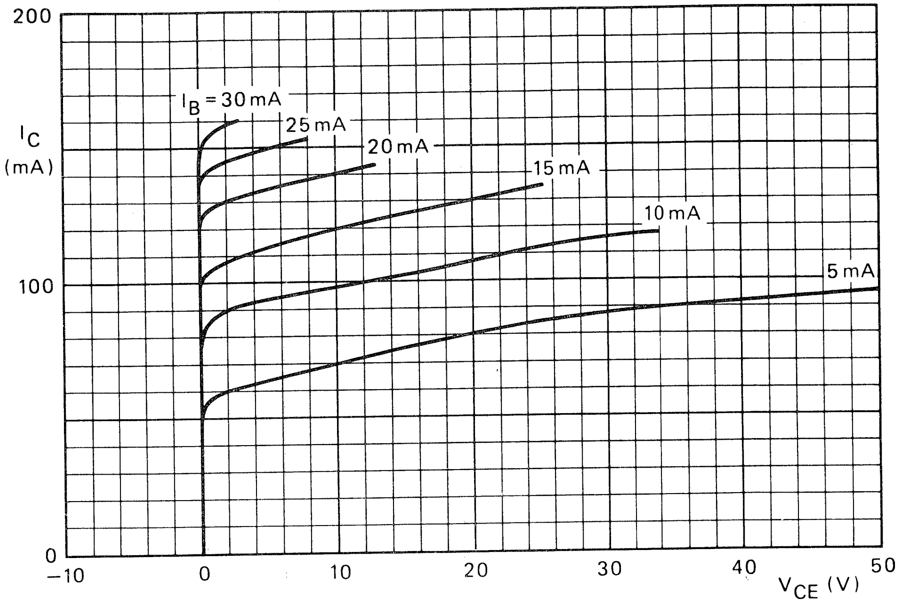


Fig. 3 T_j = 25 °C.

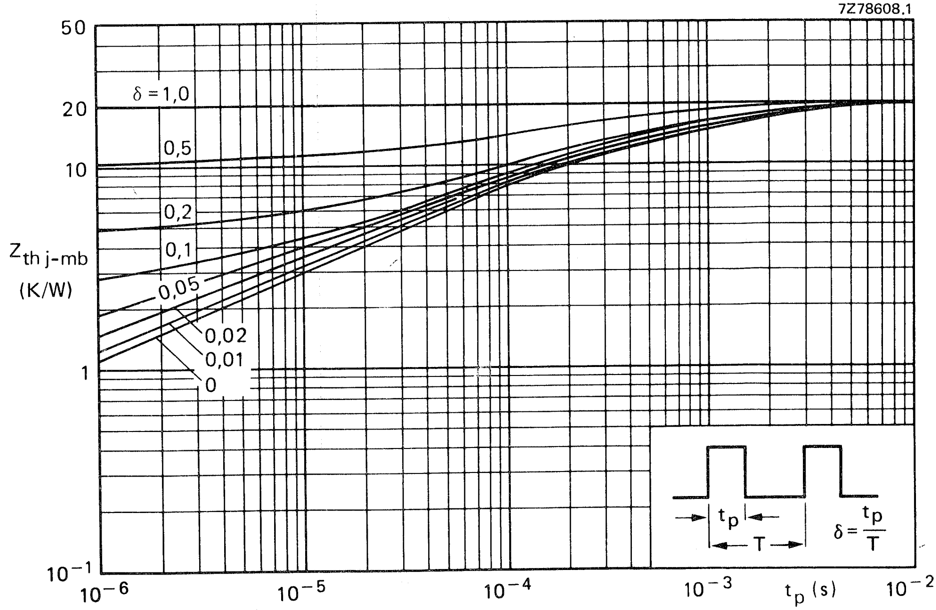


Fig. 4.

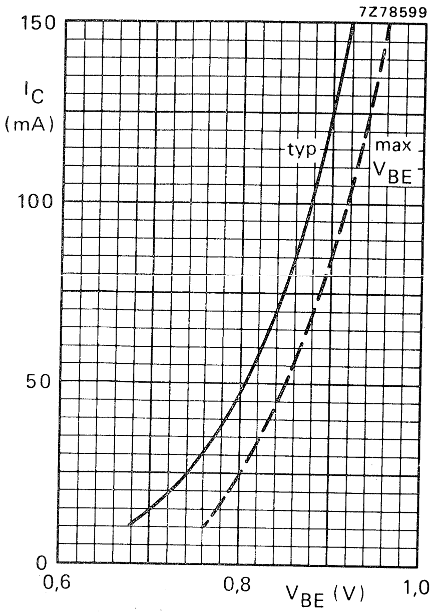


Fig. 5 V_{CE} = 20 V; T_j = 25 °C.

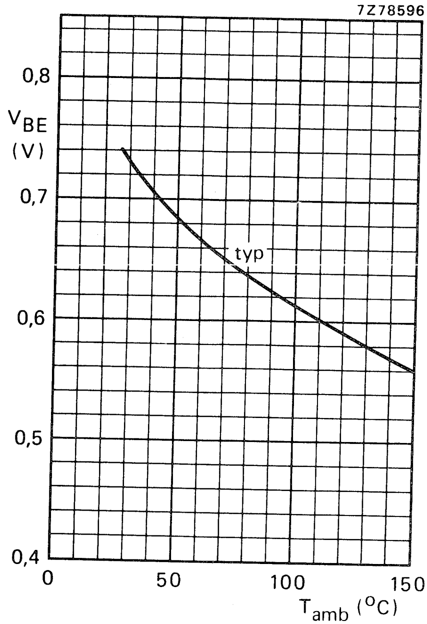


Fig. 6 I_C = 25 mA; V_{CE} = 20 V.

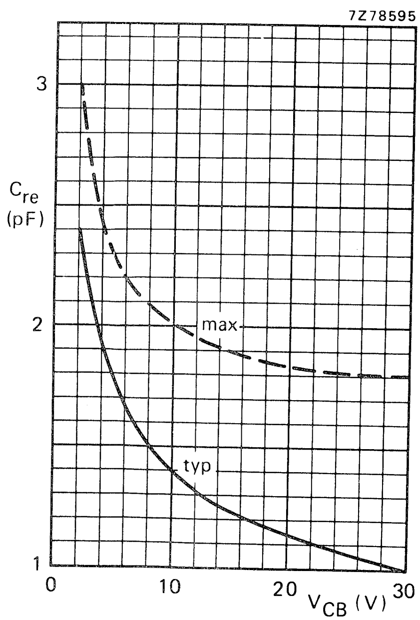


Fig. 7 I_E = 0; f = 1 MHz; T_j = 25 °C.

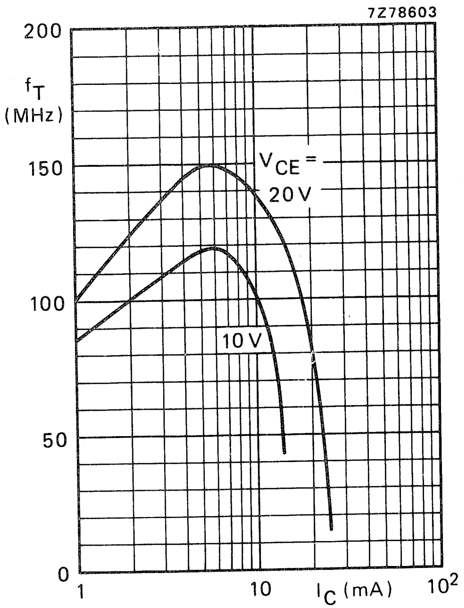


Fig. 8 f_M = 35 MHz; T_{amb} = 25 °C.

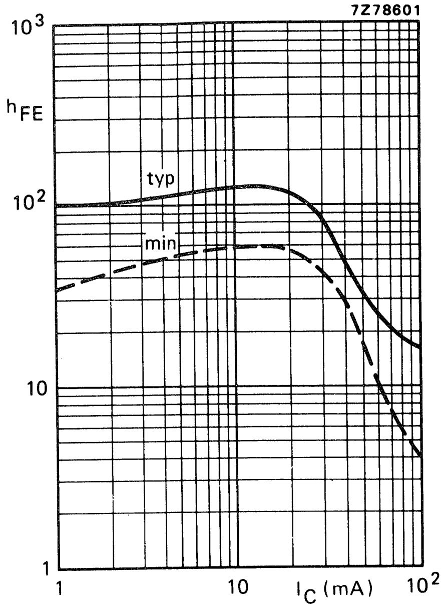


Fig. 9 V_{CE} = 20 V; T_{amb} = 25 °C.

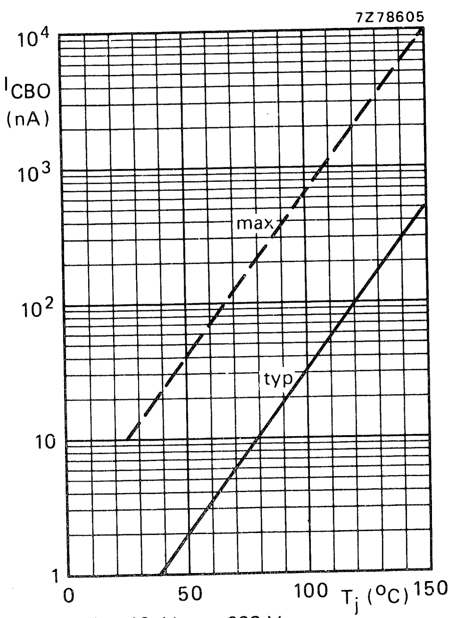


Fig. 10 V_{CB} = 200 V.

SILICON PLANAR EPITAXIAL TRANSISTORS

P-N-P transistors in a plastic envelope intended for class-B video output stages in television receivers and for high-voltage i.f. output stages.
N-P-N complements are BF469 and BF471 respectively.

QUICK REFERENCE DATA

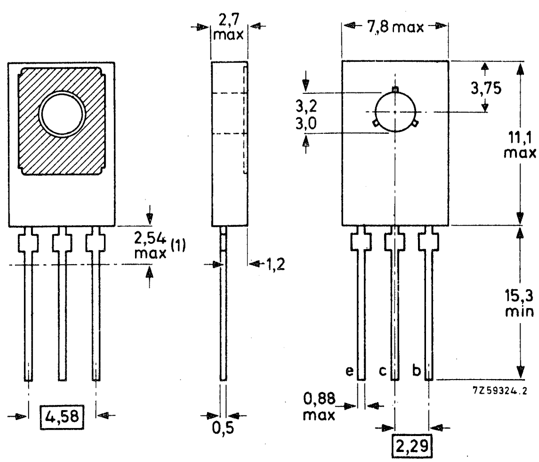
			BF470	BF472	
Collector-base voltage (open emitter)	$-V_{CBO}$	max.	250	300	V
Collector-emitter voltage					
open base	$-V_{CEO}$	max.	250	–	V
R_{BE} = 2,7 kΩ	$-V_{CER}$	max.	–	300	V
Collector current (peak value)	$-I_{CM}$	max.	100		mA
Total power dissipation up to T_{mb} = 114 °C	P_{tot}	max.	1,8		W
Junction temperature	T_j	max.	150		°C
D.C. current gain					
$-I_C$ = 25 mA; $-V_{CE}$ = 20 V	h_{FE}	>	50		
Transition frequency					
$-I_C$ = 10 mA; $-V_{CE}$ = 10 V	f_T	>	60		MHz
Feedback capacitance at f = 0,5 MHz					
I_E = 0; $-V_{CB}$ = 30 V	C_{re}	<	1,8		pF

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-126 (SOT-32).

Collector connected to mounting base.



See also chapters Accessories and Mounting Instructions.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BF470	BF472	
Collector-base voltage (open emitter)	$-V_{CBO}$	max.	250	300	V
Collector-emitter voltage					
R_{BE} = 2,7 kΩ	$-V_{CER}$	max.	–	300	V
open base	$-V_{CEO}$	max.	250	–	V
Emitter-base voltage (open collector)	$-V_{EBO}$	max.	5		V
Collector current (d.c.)	$-I_C$	max.	50		mA
Collector current (peak value)	$-I_{CM}$	max.	100		mA
Total power dissipation up to T_{mb} = 114 °C *	P_{tot}	max.	1,8		W
Storage temperature	T_{stg}		−65 to + 150		°C
Junction temperature	T_j	max.	150		°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	20	°C/W
From junction to ambient in free air *	$R_{th\ j\text{-}a}$	=	100	°C/W

* Transistor mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for collector lead minimum 10 mm x 10 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current				
$I_E = 0$; $-V_{CB} = 200$ V	$-I_{CBO}$	<	10	nA
$R_{BE} = 2{,}7$ kΩ; $-V_{CE} = 200$ V; $T_j = 150$ °C	$-I_{CER}$	<	10	μA
Emitter cut-off current				
$I_C = 0$; $-V_{EB} = 5$ V	$-I_{EBO}$	<	10	μA
D.C. current gain				
$-I_C = 25$ mA; $-V_{CE} = 20$ V	h_{FE}	>	50	
High-frequency knee voltage at $T_j = 150$ °C*				
$-I_C = 25$ mA	$-V_{CEK}$	typ.	20	V
Transition frequency				
$-I_C = 10$ mA; $-V_{CE} = 10$ V	f_T	>	60	MHz
Feedback capacitance at f = 0,5 MHz				
$I_E = 0$; $-V_{CB} = 30$ V	C_{re}	<	1,8	pF

* The high-frequency knee voltage of a transistor is that value of the collector-emitter voltage at which the small-signal gain, measured in a practical circuit, has dropped to 80% of the gain at $-V_{CE} = 50$ V. A further reduction of the collector-emitter voltage results in a rapid increase of the distortion of the signal.

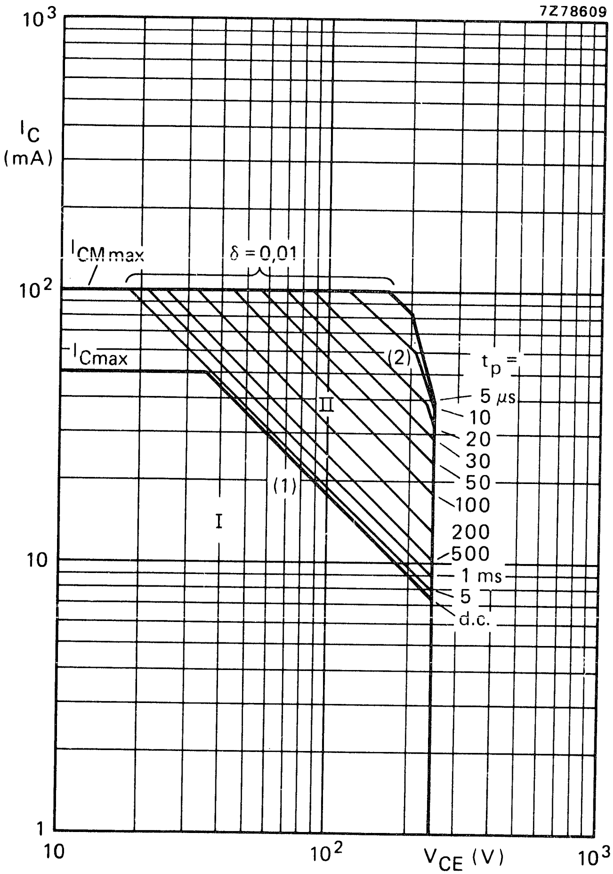


Fig. 2 Safe Operating ARea at T_{mb} = 114 °C.

I Region of permissible d.c. operation.

II Permissible extension for repetitive pulse operation.

(1) $P_{tot\,max}$ and $P_{tot\,peak\,max}$ lines.

(2) Second breakdown limits (independent of temperature).

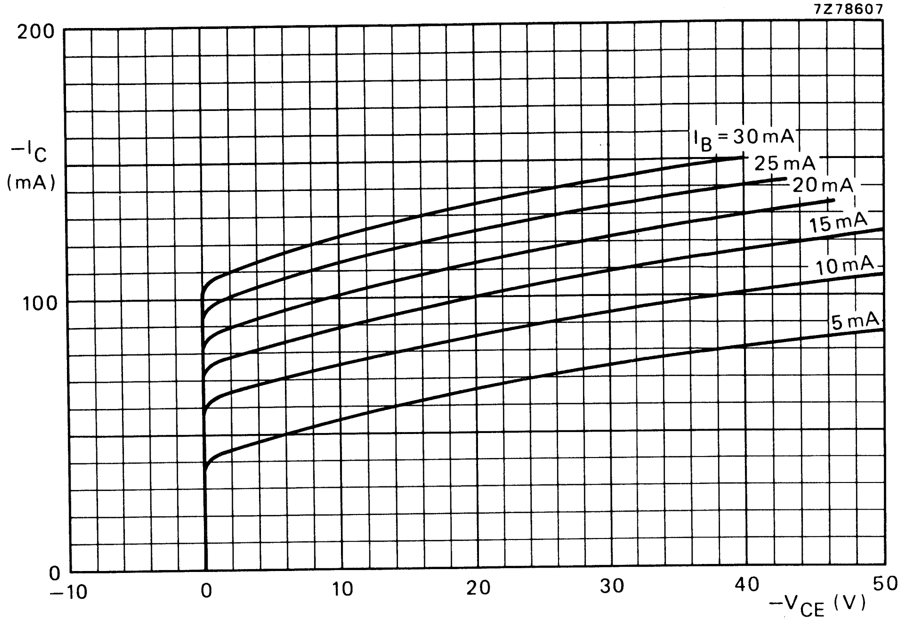


Fig. 3 T_j = 25 °C.

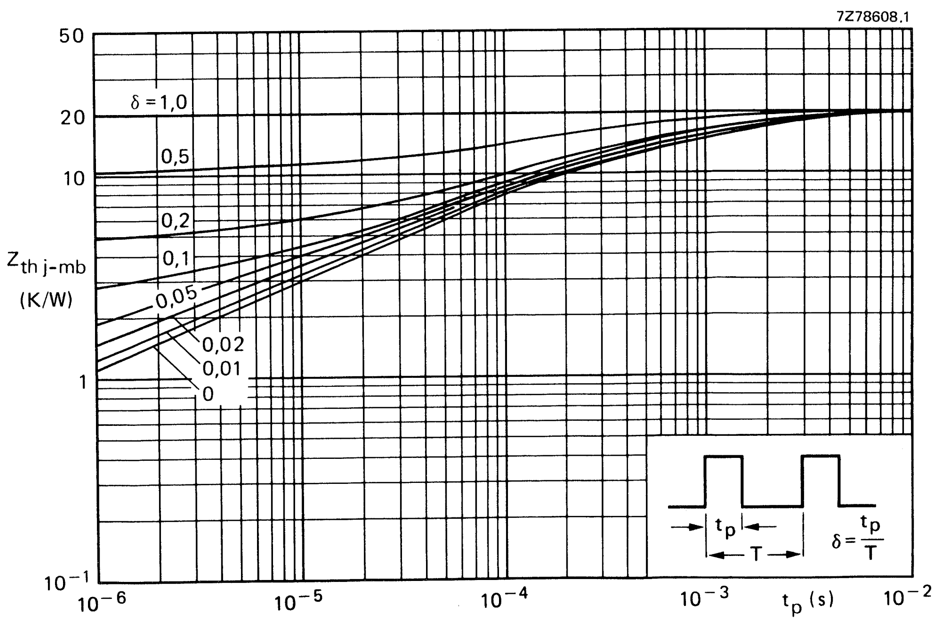


Fig. 4.

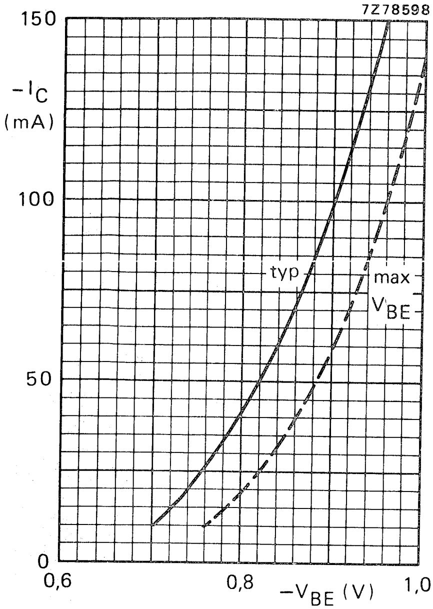


Fig. 5 $-V_{CE}$ = 20 V; T_j = 25 °C.

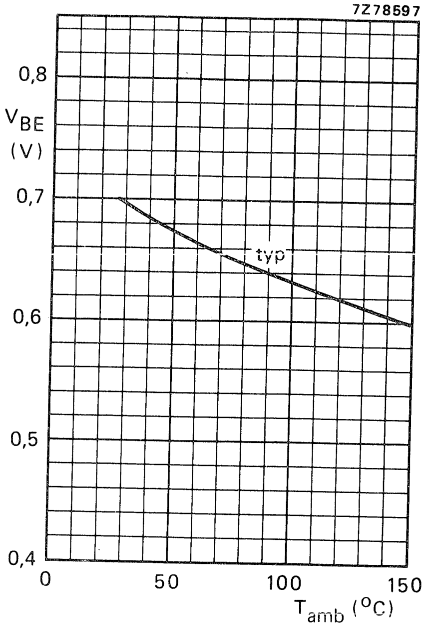


Fig. 6 $-V_{CE}$ = 20 V; $-I_C$ = 25 mA.

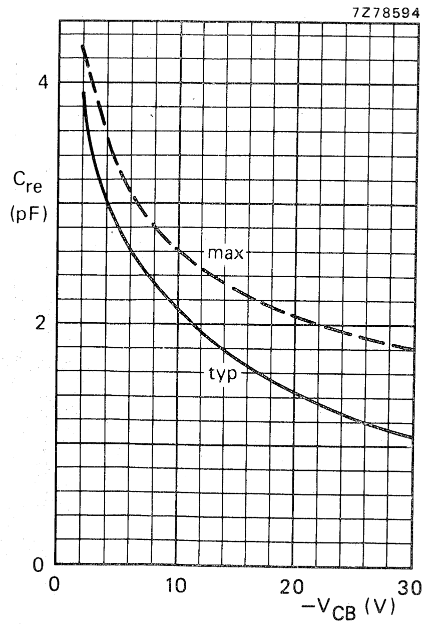


Fig. 7 I_E = 0; f = 1 MHz; T_j = 25 °C.

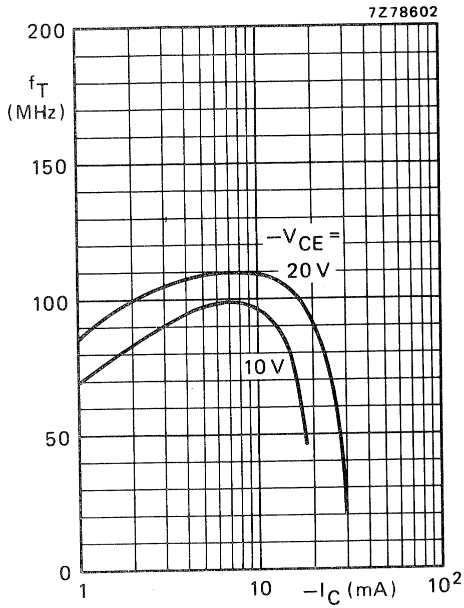


Fig. 8 f_M = 35 MHz; T_{amb} = 25 °C.

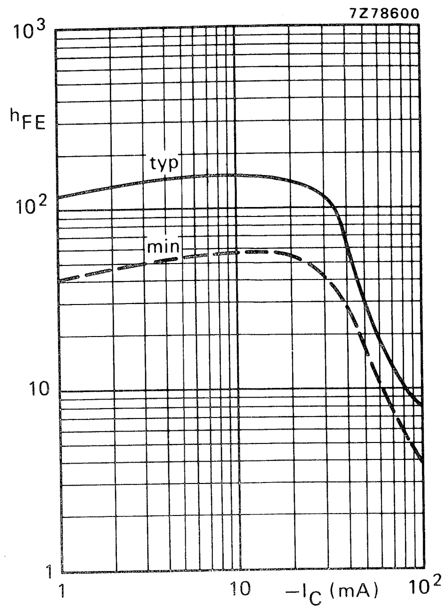


Fig. 9 $-V_{CE}$ = 20 V; T_{amb} = 25 °C.

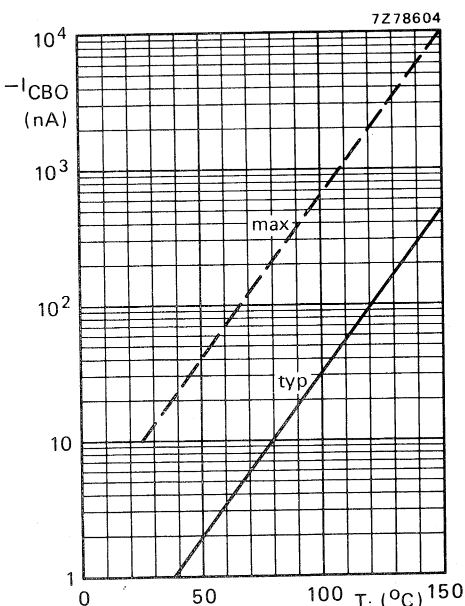


Fig. 10 $-V_{CB}$ = 200 V.

SILICON PLANAR TRANSISTOR

N-P-N transistor in TO-202 plastic envelope intended for use as a driver for line output transistors in colour television receivers.

QUICK REFERENCE DATA

Collector-base voltage (open emitter)	V_{CBO}	max.	300 V
Collector-emitter voltage (open base)	V_{CEO}	max.	250 V
Collector current (peak value)	I_{CM}	max.	300 mA
Total power dissipation up to T_{mb} = 75 °C	P_{tot}	max.	6 W
Junction temperature	T_j	max.	150 °C
D.C. current gain I_C = 20 mA, V_{CE} = 10 V	h_{FE}	typ.	45
Storage time	t_s	typ.	0,5 µs

MECHANICAL DATA

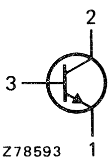
Dimensions in mm

Fig. 1 TO-202.

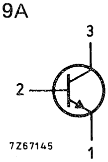
Collector connected to mounting base.

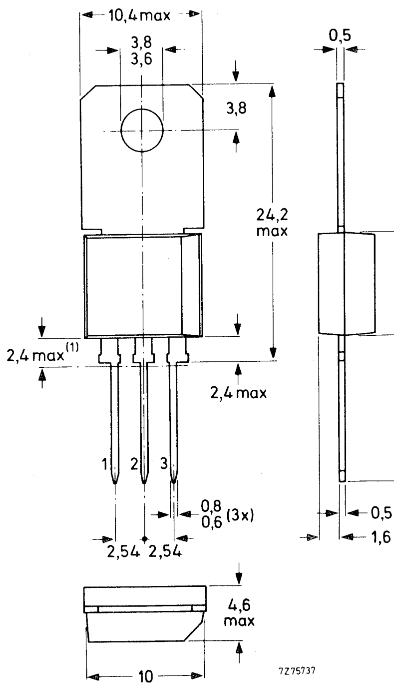
(1) Plastic flash allowed within this zone.

BF819



BF819A





BF819A is available on request. It has ebc pinning instead of ecb.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-base voltage (open emitter)	V_{CBO}	max.	300	V
Collector-emitter voltage (open base)	V_{CEO}	max.	250	V
Emitter-base voltage (open collector)	V_{EBO}	max.	5	V
Collector current (d.c.)	I_C	max.	100	mA
Collector current (peak value)*	I_{CM}	max.	300	mA
Base current (d.c.)	I_B	max.	50	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	1,2	W
Total power dissipation up to T_{mb} = 75 °C	P_{tot}	max.	6	W
Storage temperature	T_{stg}	−65 to +150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	62,5	K/W
From junction to mounting base	$R_{th\ j\text{-}mb}$	=	12,5	K/W

* Precautions should be taken during switch-on of the BF819 where an overshoot of current is likely to occur. The amplitude of the overshoot depends on the relative magnitude of stray external capacities to the transistor collector capacity. It is desirable to keep the stray capacities to a minimum by short lead lengths etc. so as to minimise the area of the switching path.

CHARACTERISTICS

T_j = 25 °C

Collector cut-off current I_E = 0; V_{CB} = 250 V	I_{CBO}	<	50 nA
Emitter cut-off current I_C = 0; V_{EB} = 3 V	I_{EBO}	<	50 nA
D.C. current gain I_C = 20 mA; V_{CE} = 10 V	h_{FE}	typ.	45
Collector-emitter saturation voltage I_C = 200 mA; I_B = 20 mA*	$V_{CE\,sat}$	<	11 V
Collector output capacitance at f = 1 MHz I_E = 0; V_{CB} = 30 V	C_{ob}	<	4,5 pF
Storage time (in the typical circuit below)	t_s	typ.	0,5 μs

* The BF819 is controlled to V_{CEsat} max. 11,0 V and is thermally stable under all operating conditions where $T_{j\,max}$ of 150 °C is not exceeded. For the typical circuit shown below, a heatsink is not required for operation with T_{amb} ≤ 75 °C.

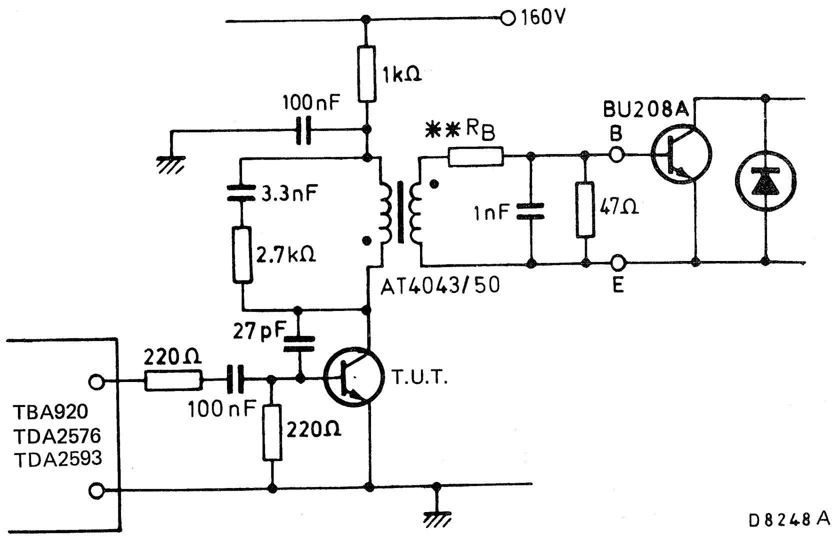


Fig. 2 Typical circuit.

** R_B is chosen so that the end-of-scan base current for the BU208A is 1,4 A under nominal conditions. Typical value of R_B is 0,5 Ω plus 0,1 Ω lead resistance.

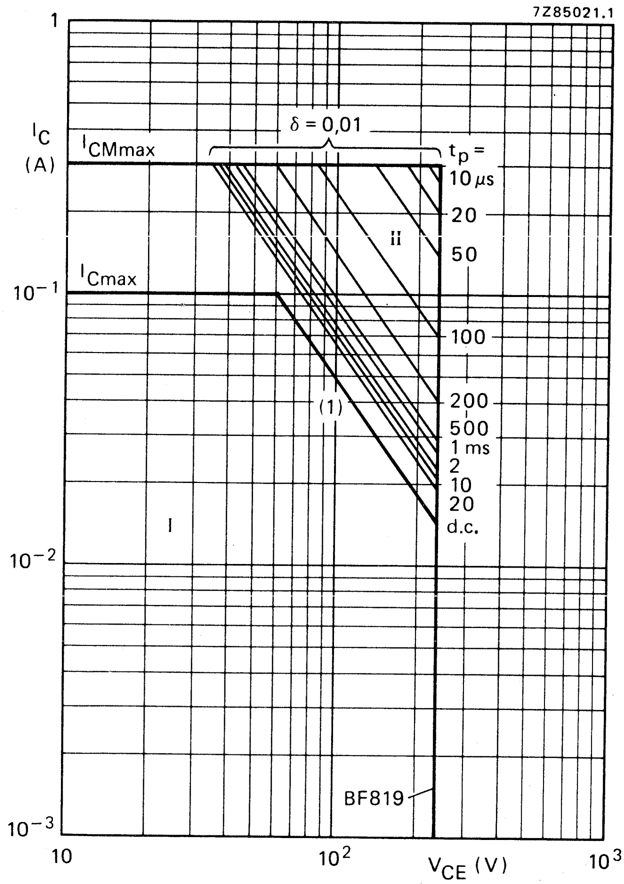


Fig. 3 Safe Operating ARea; $T_{mb} = 25\ ^oC$.

I Region of permissible d.c. operation.

II Permissible extension for repetitive pulse operation.

(1) Second breakdown limits (independent of temperature).

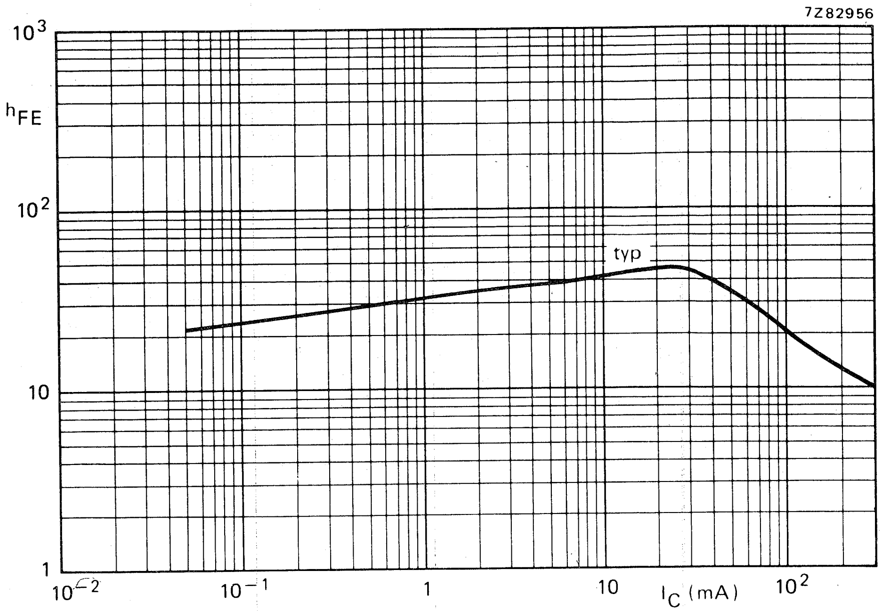


Fig. 4 D.C. current gain. V_{CB} = 10 V.

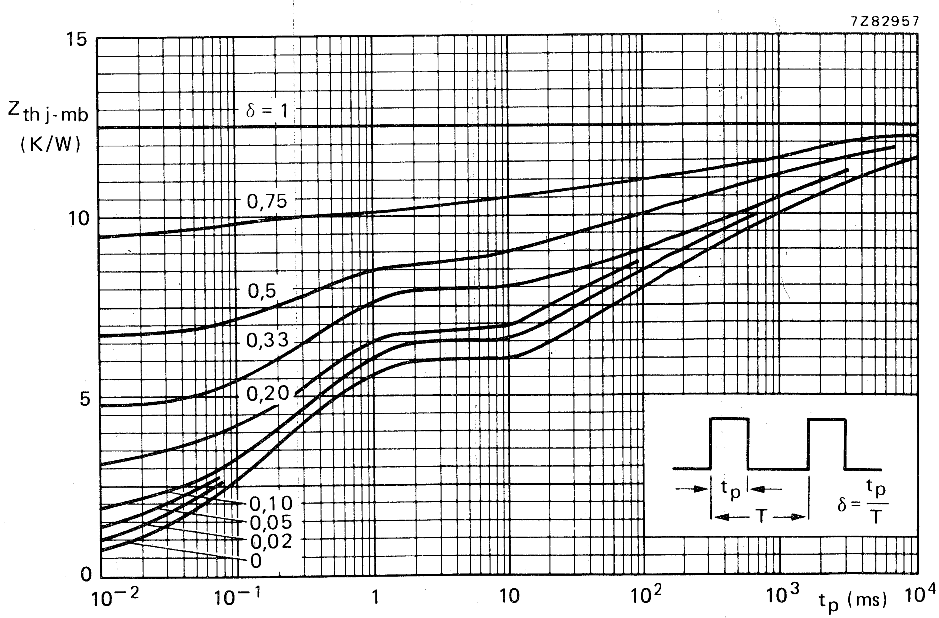


Fig. 5 Pulse power rating chart.

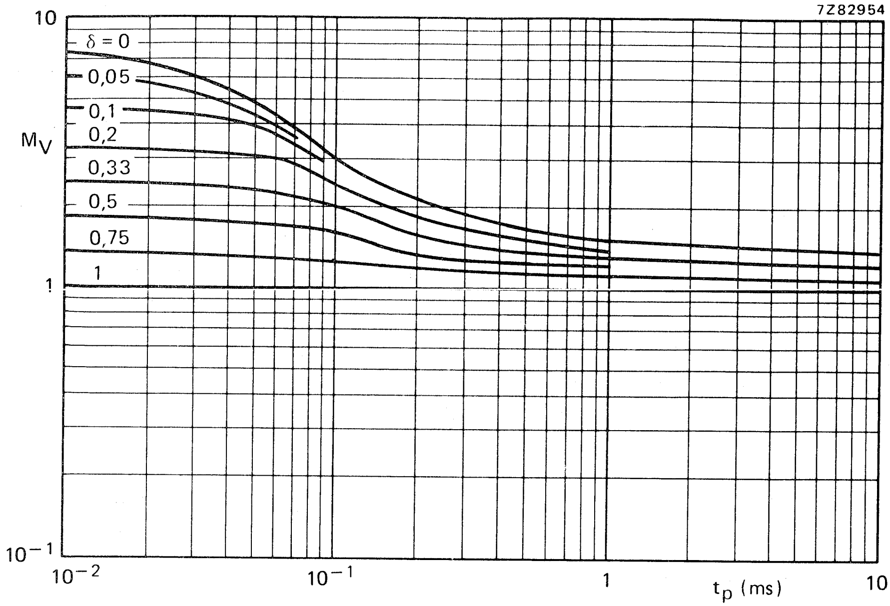


Fig. 6 S.B. voltage multiplying factor at the I_{Cmax} level.

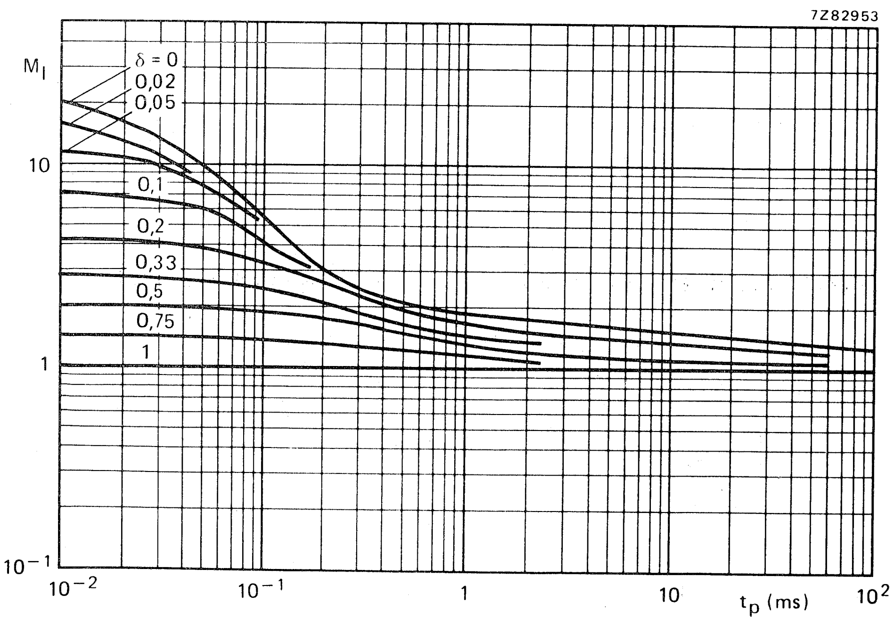


Fig. 7 S.B. current multiplying factor at the V_{CEOmax} level.

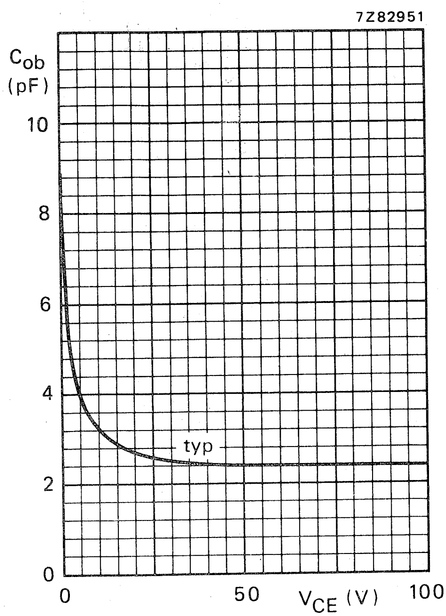


Fig. 8 Collector output capacitance
$f = 1$ MHz; $I_E = 0$.

SILICON PLANAR VIDEO OUTPUT TRANSISTORS

N-P-N transistors in TO-202 plastic envelopes intended for video output stages in black-and-white and in colour television receivers.

QUICK REFERENCE DATA

			BF857	BF858	BF859	
Collector-base voltage (open emitter)	V_{CBO}	max.	160	250	300	V
Collector-emitter voltage (open base)	V_{CEO}	max.	160	250	300	V
Collector current (peak value)	I_{CM}	max.		300		mA
Total power dissipation up to T_{mb} = 75 °C	P_{tot}	max.		6		W
Junction temperature	T_j	max.		150		°C
D.C. current gain I_C = 30 mA; V_{CE} = 10 V	h_{FE}	>		26		
Transition frequency at f = 35 MHz I_C = 15 mA; V_{CE} = 10 V	f_T	typ.		90		MHz
Feedback capacitance at f = 1 MHz I_E = 0; V_{CB} = 30 V	C_{re}	<		3		pF

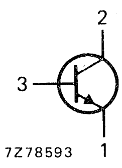
MECHANICAL DATA

Dimensions in mm

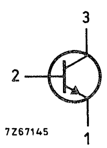
Fig. 1 TO-202.

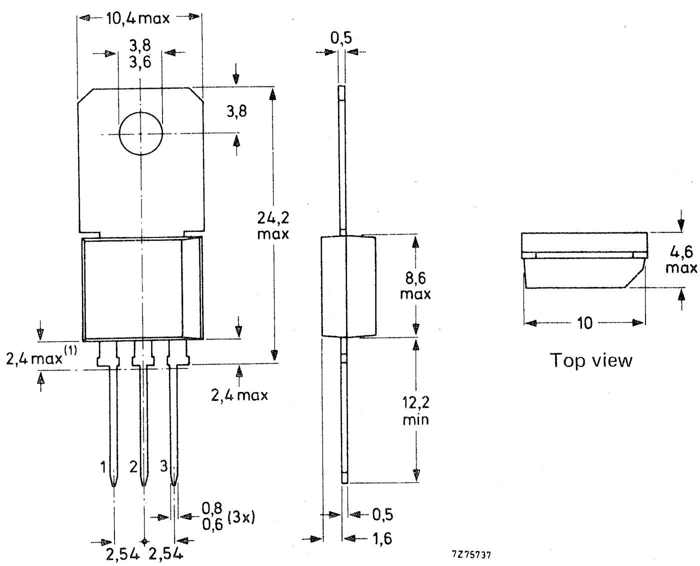
Collector connected to mounting base.

(1) Plastic flash allowed within this zone.



A-version





An A-version is available on request. It has ebc pinning instead of ecb.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BF857	BF858	BF859	
Collector-base voltage (open emitter)	V_{CBO}	max.	160	250	300	V
Collector-emitter voltage (open base)	V_{CEO}	max.	160	250	300	V
Emitter-base voltage (open collector)	V_{EBO}	max.	5	5	5	V
Collector current (d.c.)	I_C	max.		100		mA
Collector current (peak value)	I_{CM}	max.		300		mA
Base current (d.c.)	I_B	max.		50		mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.		2		W
Total power dissipation up to T_{mb} = 75 °C	P_{tot}	max.		6		W
Storage temperature	T_{stg}			–65 to + 150		°C
Junction temperature	T_j	max.		150		°C

THERMAL RESISTANCE

from junction to ambient in free air	$R_{th\ j\text{-}a}$	=	62,5	K/W
from junction to mounting base	$R_{th\ j\text{-}mb}$	=	12,5	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current				
I_E = 0; V_{CB} = 100 V for BF857	I_{CBO}	<	0,1	μA
I_E = 0; V_{CB} = 200 V for BF858	I_{CBO}	<	0,1	μA
I_E = 0; V_{CB} = 250 V for BF859	I_{CBO}	<	0,1	μA
Emitter cut-off current				
I_C = 0; V_{EB} = 5 V	I_{EBO}	<	100	μA
D.C. current gain				
I_C = 30 mA; V_{CE} = 10 V	h_{FE}	>	26	
Collector-emitter saturation voltage				
I_C = 30 mA; I_B = 6 mA	V_{CEsat}	<	1	V
Transition frequency at f = 35 MHz				
I_C = 15 mA; V_{CE} = 10 V	f_T	typ.	90	MHz
Feedback capacitance at f = 1 MHz				
I_E = 0; V_{CB} = 30 V	C_{re}	<	3	pF

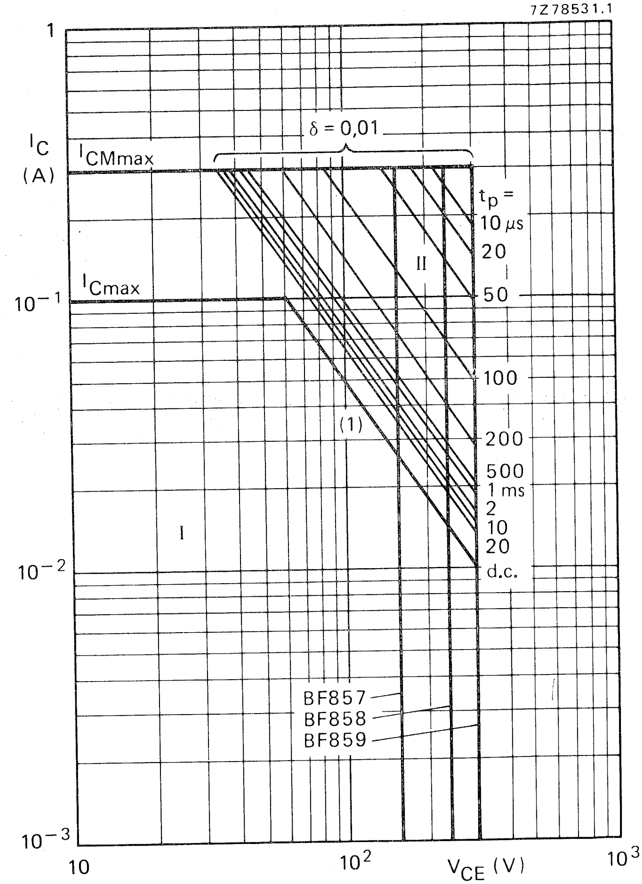


Fig. 2 Safe Operating ARea; T_{mb} = 75 °C.

I Region of permissible d.c. operation.

II Permissible extension for repetitive pulse operation.

(1) Second-breakdown limits (independent of temperature).

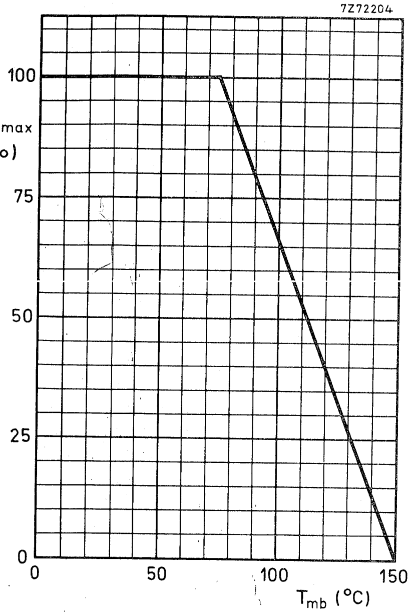


Fig. 3 Power derating curve.

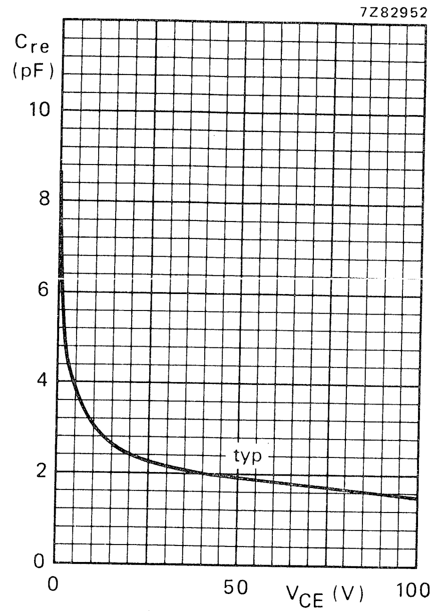


Fig. 4 Feedback capacitance f = 1 MHz.

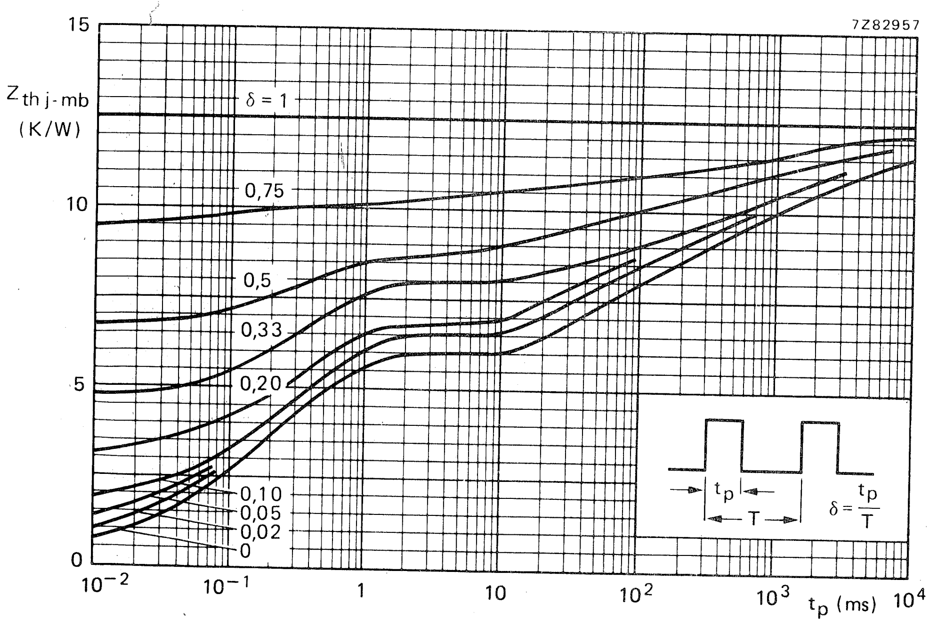


Fig. 5 Pulse power rating chart.

7Z82954

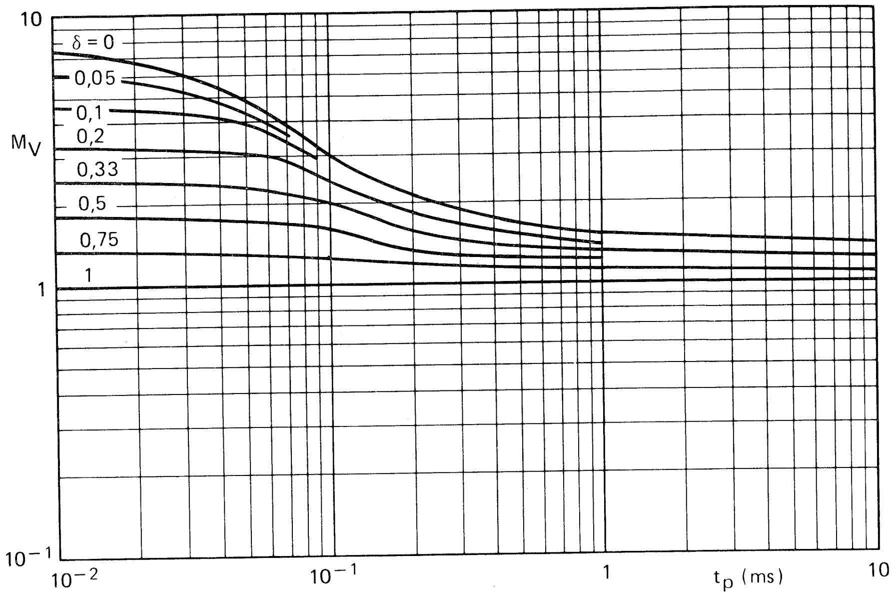


Fig. 6 S.B. voltage multiplying factor at the I_{Cmax} level.

7Z82953

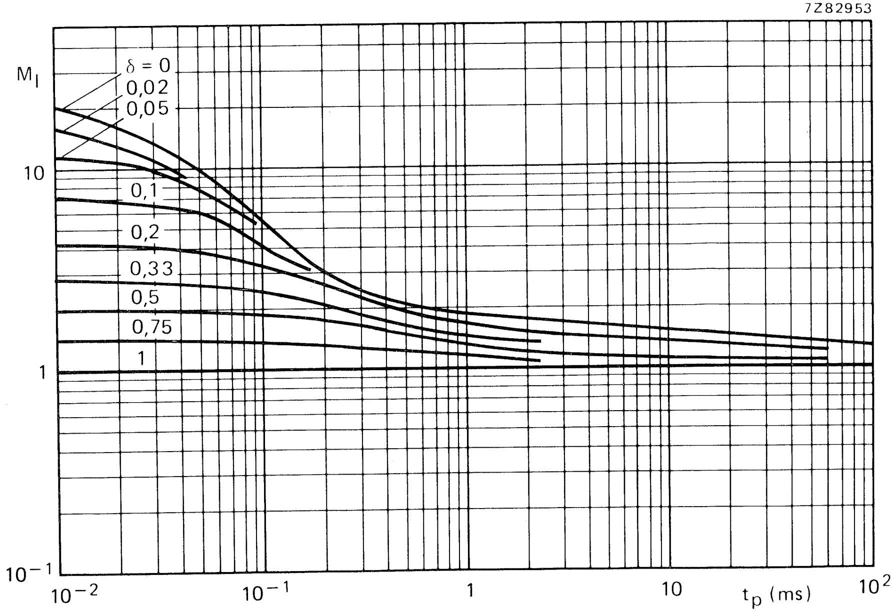


Fig. 7 S.B. current multiplying factor at the V_{CEmax} level.

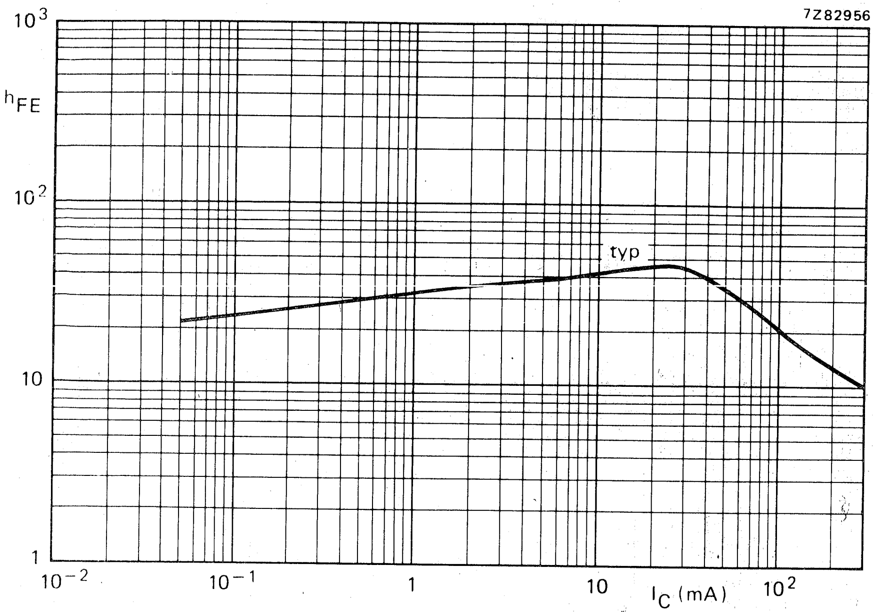


Fig. 8 D.C. current gain. V_{CE} = 10 V.

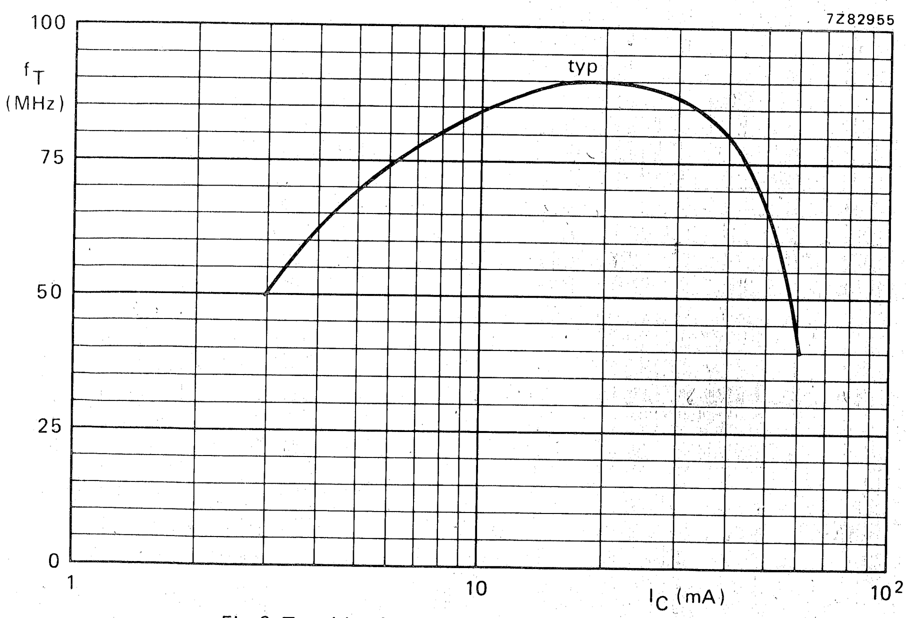


Fig. 9 Transition frequency. V_{CE} = 10 V; f = 35 MHz.

SILICON PLANAR VIDEO OUTPUT TRANSISTORS

N-P-N transistors in a TO-202 plastic envelope intended for class-B video output stages in colour television receivers. P-N-P complements are BF870 and BF872.

QUICK REFERENCE DATA

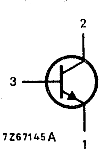
			BF869	BF871	
Collector-base voltage (open emitter)	V_{CBO}	max.	250	300	V
Collector-emitter voltage (open base)	V_{CEO}	max.	250	–	V
Collector-emitter voltage (R_{BE} = 2,7 kΩ)	V_{CER}	max.	–	300	V
Collector current (peak value)	I_{CM}	max.	100	100	mA
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	5	5	W
Junction temperature	T_j	max.	150	150	°C
D.C. current gain I_C = 25 mA; V_{CE} = 20 V; T_j = 25 °C	h_{FE}	>	50	50	
Transition frequency $-I_E$ = 10 mA; V_{CB} = 10 V	f_T	>	60	60	MHz
Feedback capacitance at f = 1 MHz I_E = 0; V_{CB} = 30 V	C_{re}	<	2	2	pF

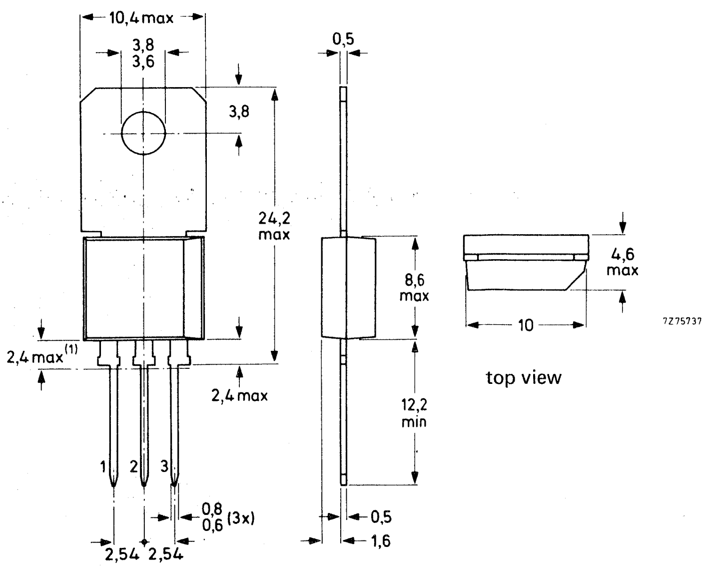
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-202.

Collector connected to mounting base.





(1) Plastic flash allowed within this zone.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BF869	BF871	
Collector-base voltage (open emitter)	V_{CBO}	max.	250	300	V
Collector-emitter voltage (open base)	V_{CEO}	max.	250	–	V
Collector-emitter voltage (R_{BE} = 2,7 kΩ)	V_{CER}	max.	–	300	V
Emitter-base voltage (open collector)	V_{EBO}	max.	5		V
Collector current (d.c.)	I_C	max.	50		mA
Collector current (peak value)	I_{CM}	max.	100		mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1,6		W
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	5		W
Storage temperature	T_{stg}		−65 to +150		°C
Junction temperature	T_j	max.	150		°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	78	K/W
From junction to mounting base	$R_{th\ j\text{-}mb}$	=	25	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			BF869	BF871	
Collector cut-off current					
I_E = 0; V_{CB} = 200 V	I_{CBO}	<	10	10	nA
R_{BE} = 2,7 kΩ; V_{CE} = 300 V	I_{CER}	<	–	1	μA
R_{BE} = 2,7 kΩ; V_{CE} = 200 V; T_j = 150 °C	I_{CER}	<	10		μA
Emitter cut-off current					
I_C = 0; V_{EB} = 5 V	I_{EBO}	<	10		μA
D.C. current gain					
I_C = 25 mA; V_{CE} = 20 V	h_{FE}	>	50		
Base-emitter voltage					
I_C = 25 mA; V_{CE} = 20 V	V_{BE}	typ.	0,75		V
High frequency knee voltage					
I_C = 25 mA; T_j = 150 °C	V_{CEK}	typ.	20		V
Transition frequency					
$-I_E$ = 10 mA; V_{CB} = 10 V	f_T	>	60		MHz
Feedback capacitance at f = 1 MHz					
I_E = 0; V_{CB} = 30 V	C_{re}	<	2		pF

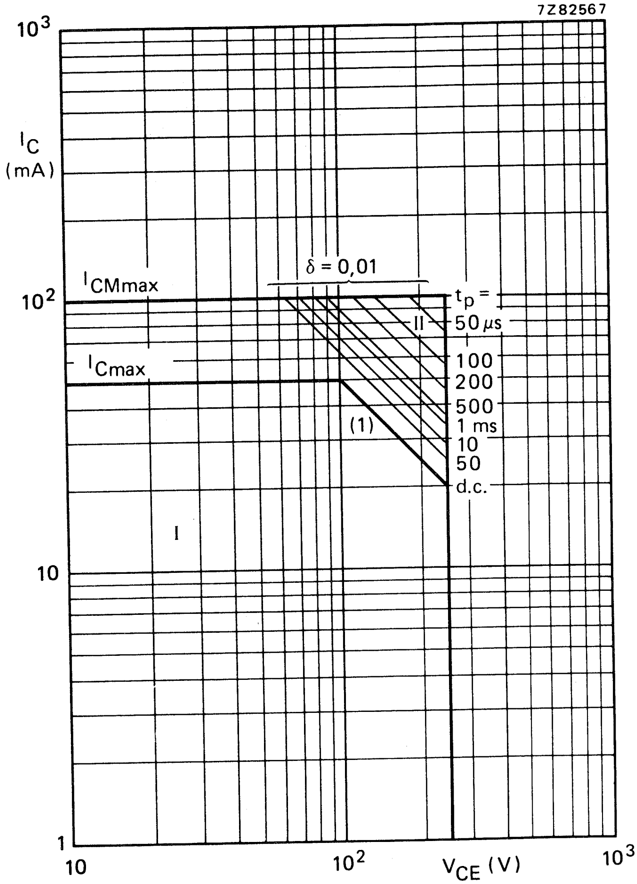


Fig. 2 Safe Operating ARea at T_{mb} = 25 °C.

I Region of permissible d.c. operation.
II Permissible extension for repetitive pulse operation.
(1) $P_{tot\ max}$ and $P_{tot\ peak\ max}$ lines.

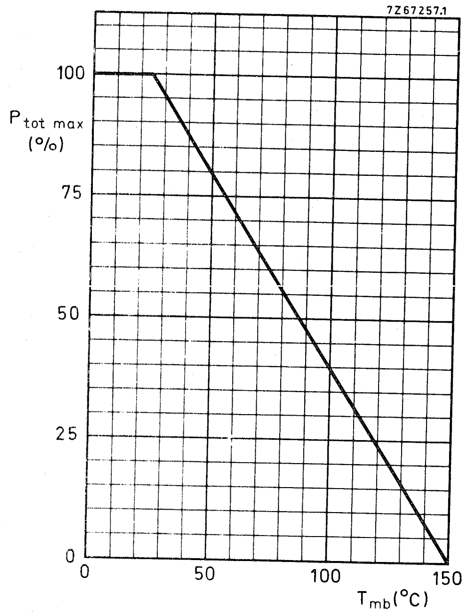


Fig. 3 Power derating curve.

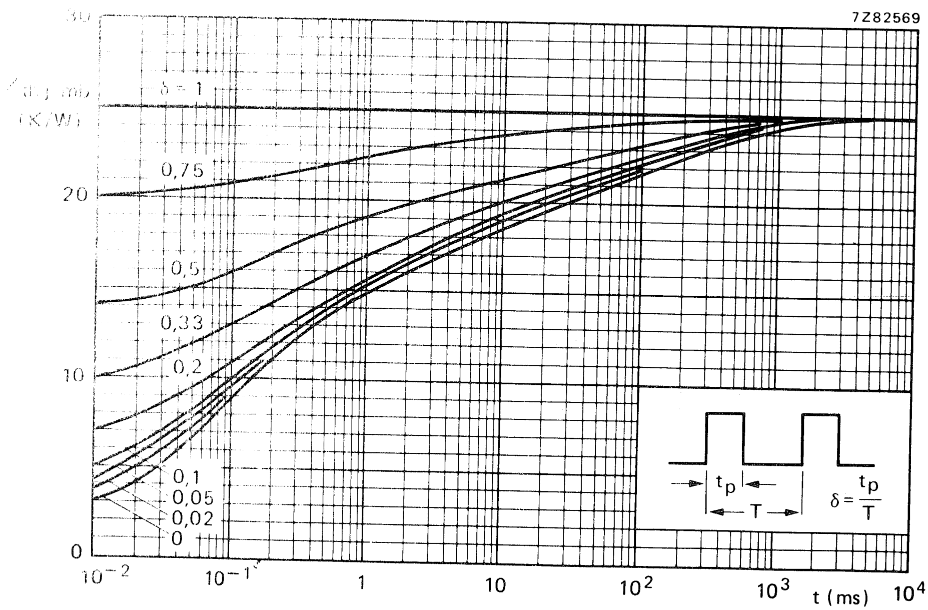


Fig. 4 Pulse power rating chart.

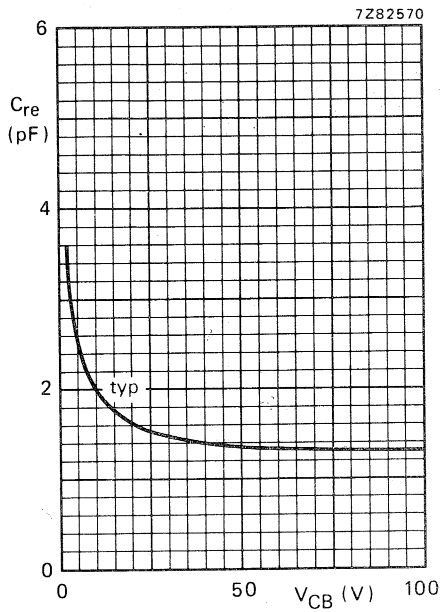


Fig. 5 $I_E = 0$; f = 1 MHz; $T_j = 25\ ^oC$.

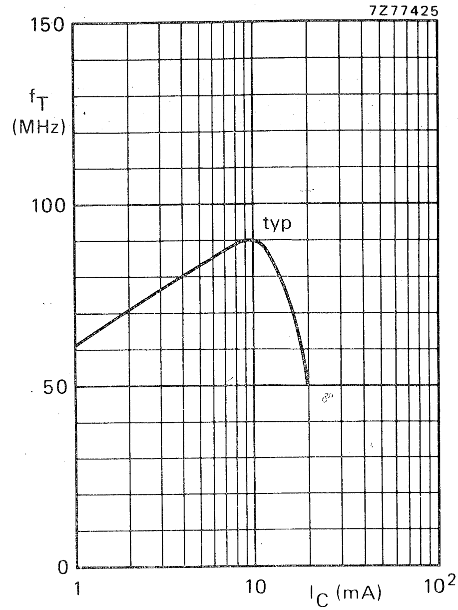


Fig. 6 $V_{CE} = 10$ V; $T_j = 25\ ^oC$.

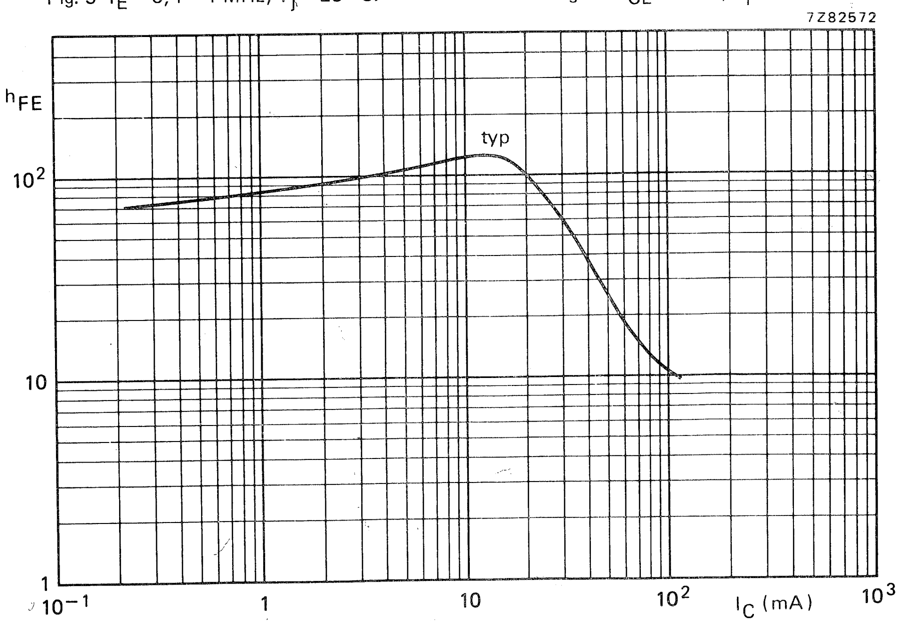


Fig. 7 D.C. current gain at $V_{CE} = 20$ V; $T_{amb} = 25\ ^oC$.

SILICON PLANAR VIDEO OUTPUT TRANSISTORS

P-N-P transistors in a TO-202 plastic envelope intended for class-B video output stages in colour television receivers. N-P-N complements are BF869 and BF871.

QUICK REFERENCE DATA

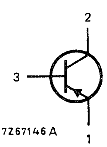
			BF870	BF872	
Collector-base voltage (open emitter)	$-V_{CBO}$	max.	250	300	V
Collector-emitter voltage (open base)	$-V_{CEO}$	max.	250	–	V
Collector-emitter voltage (R_{BE} = 2,7 kΩ)	$-V_{CER}$	max.	–	300	V
Collector current (peak value)	$-I_{CM}$	max.	100		mA
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	5		W
Junction temperature	T_j	max.	150		°C
D.C. current gain $-I_C$ = 25 mA; $-V_{CE}$ = 20 V; T_j = 25 °C	h_{FE}	>	50		
Transition frequency I_E = 10 mA; $-V_{CB}$ = 10 V	f_T	>	60		MHz
Feedback capacitance at f = 1 MHz I_E = 0; $-V_{CB}$ = 30 V	C_{re}	<	2,2		pF

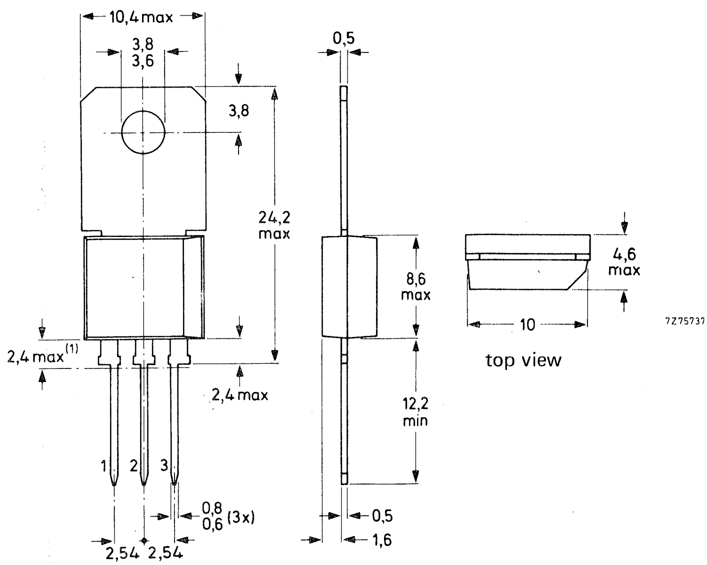
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-202.

Collector connected to mounting base.





(1) Plastic flash allowed within this zone.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BF870	BF872	
Collector-base voltage (open emitter)	$-V_{CBO}$	max.	250	300	V
Collector-emitter voltage (open base)	$-V_{CEO}$	max.	250	–	V
Collector-emitter voltage (R_{BE} = 2,7 kΩ)	$-V_{CER}$	max.	–	300	V
Emitter-base voltage (open collector)	$-V_{EBO}$	max.	5		V
Collector current (d.c.)	$-I_C$	max.	50		mA
Collector current (peak value)	$-I_{CM}$	max.	100		mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1,6		W
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	5		W
Storage temperature	T_{stg}		–65 to +150		°C
Junction temperature	T_j	max.	150		°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	78	K/W
From junction to mounting base	$R_{th\ j\text{-}mb}$	=	25	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			BF870	BF872	
Collector cut-off current					
I_E = 0; $-V_{CB}$ = 200 V	$-I_{CBO}$	<	10	10	nA
R_{BE} = 2,7 kΩ; $-V_{CE}$ = 300 V	$-I_{CER}$	<	–	1	μA
R_{BE} = 2,7 kΩ; $-V_{CE}$ = 200 V; T_j = 150 °C	$-I_{CER}$	<	10		μA
Emitter cut-off current					
I_C = 0; $-V_{EB}$ = 5 V	$-I_{EBO}$	<	10		μA
D.C. current gain					
$-I_C$ = 25 mA; $-V_{CE}$ = 20 V	h_{FE}	>	50		
Base emitter voltage					
$-I_C$ = 25 mA; $-V_{CE}$ = 20 V	$-V_{BE}$	typ.	0,75		V
High-frequency knee voltage					
$-I_C$ = 25 mA; T_j = 150 °C	$-V_{CEK}$	typ.	20		V
Transition frequency					
I_E = 10 mA; $-V_{CB}$ = 10 V	f_T	>	60		MHz
Feedback capacitance at f = 1 MHz					
I_E = 0; $-V_{CB}$ = 30 V	C_{re}	<	2,2		pF

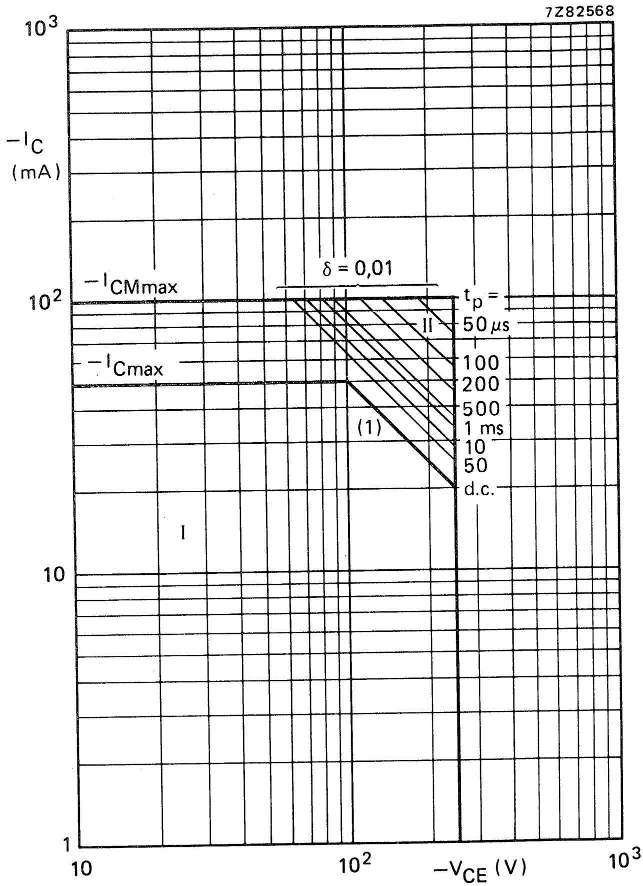


Fig. 2 Safe Operating ARea; T_{mb} = 25 °C.

I Region of permissible d.c. operation.
II Permissible extension for repetitive pulse operation.
(1) $P_{tot\ max}$ and $P_{tot\ peak\ max}$ lines.

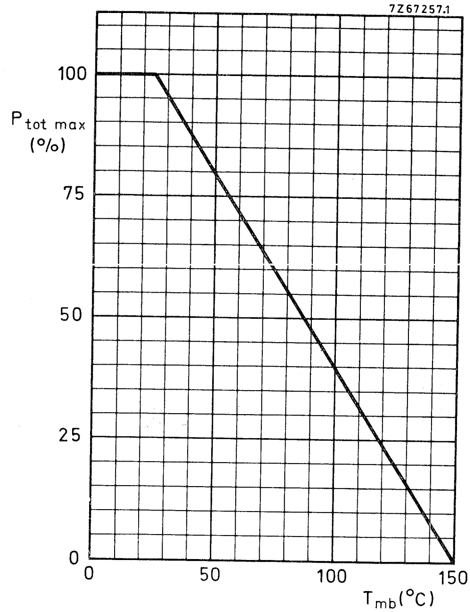


Fig. 3 Power derating curve.

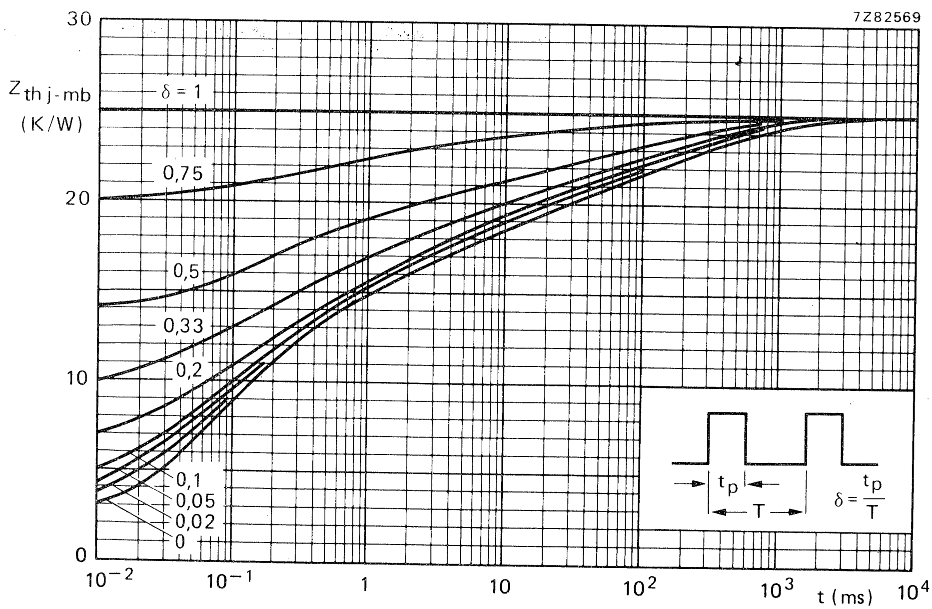


Fig. 4 Pulse power rating chart.

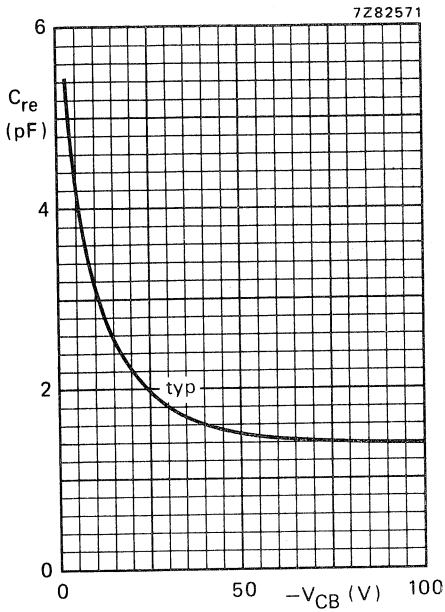


Fig. 5 $I_E = 0$; f = 1 MHz; T_{amb} = 25 °C.

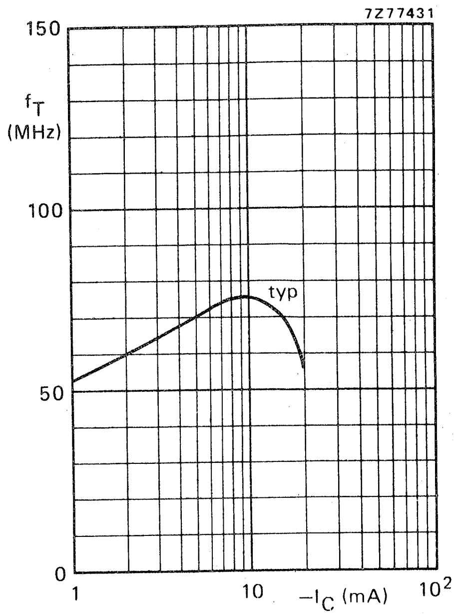


Fig. 6 $-V_{CE}$ = 10 V; T_j = 25 °C.

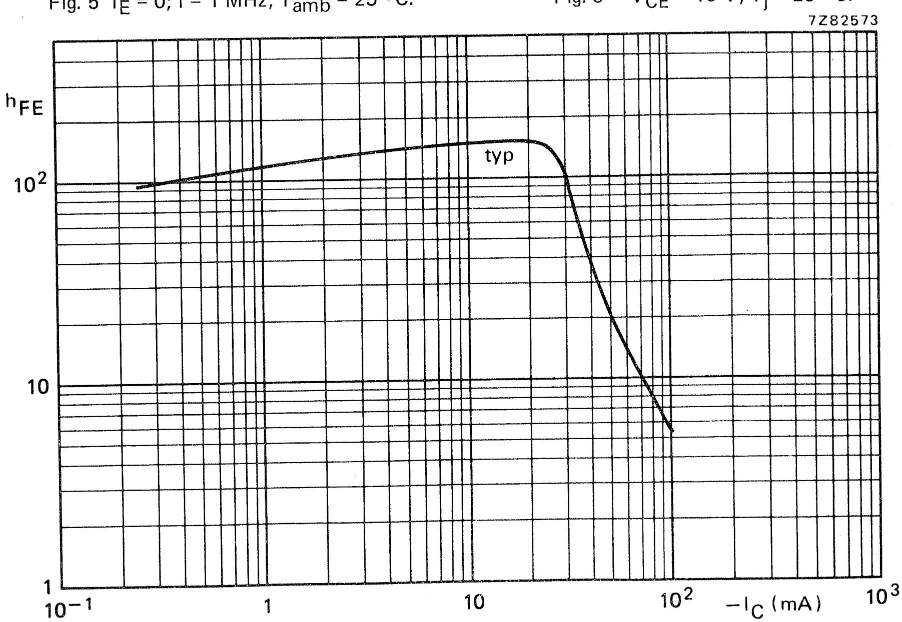


Fig. 7 D.C. current gain at $-V_{CE}$ = 20 V; T_{amb} = 25 °C.

Successor type is BU508A

SILICON DIFFUSED POWER TRANSISTOR

High-voltage, high-speed switching n-p-n transistor in a metal envelope intended for use in horizontal deflection circuits of colour television receivers.

QUICK REFERENCE DATA

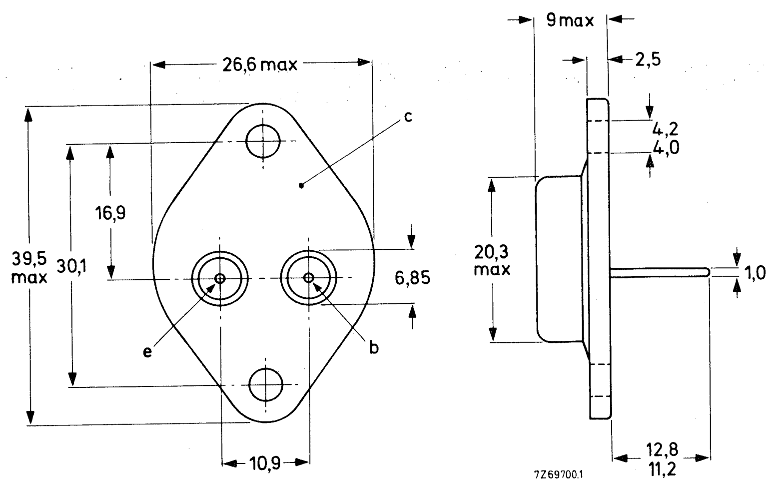
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	1500	V
Collector current (d.c.)	I_C	max.	5	A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	80	W
Collector-emitter saturation voltage I_C = 4,5 A; I_B = 2 A	V_{CEsat}	<	1	V
Fall time I_{CM} = 4,5 A; $I_{B(end)}$ = 1,4 A	t_f	typ.	0,7	µs

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Collector connected to case.



See also chapters Mounting Instructions and Accessories.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	1500 V
Collector-emitter voltage (open base)	V_{CEO}	max.	700 V
Collector current (d.c.)	I_C	max.	5 A
Collector current (peak value)	I_{CM}	max.	7,5 A
Collector current (non-repetitive peak)	I_{CSM}	max.	15 A
Base current (peak value)	I_{BM}	max.	4 A
Reverse base current (d.c. or average over any 20 ms period)	$-I_{B(AV)}$	max.	100 mA
Reverse base current (peak value) *	$-I_{BM}$	max.	4 A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	80 W
Storage temperature	T_{stg}	−65 to + 115 °C	
Junction temperature	T_j	max.	115 °C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	max.	1,12 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current $V_{BE} = 0$; $V_{CE} = V_{CESMmax}$	I_{CES}	<	1,0 mA
D.C. current gain I_C = 4,5 A; V_{CE} = 5 V	h_{FE}	>	2,5
Emitter-base voltage $I_C = 0$; I_E = 10 mA	$+V_{EBO}$	>	5 V
$I_C = 0$; I_E = 100 mA	$+V_{EBO}$	typ.	7 V
Saturation voltage I_C = 4,5 A; I_B = 2 A	V_{CEsat}	<	1 V
I_C = 4,5 A; I_B = 2 A	V_{BEsat}	<	1,5 V
Collector-emitter sustaining voltage $I_B = 0$; I_C = 100 mA; L = 25 mH	$V_{CEOsust}$	>	700 V
Transition frequency at f = 5 MHz I_C = 0,1 A; V_{CE} = 5 V	f_T	typ.	7 MHz
Collector capacitance at f = 1 MHz $I_E = I_e = 0$; V_{CB} = 10 V	C_c	typ.	125 pF
Switching times (in line deflection circuit) L_B = 6 μH; $-V_{IM}$ = 4 V; I_{CM} = 4,5 A; $I_{B(end)}$ = 1,4 A ($-dI_B/dt$ = 0,6 A/μs)	t_f	typ.	0,7 μs
	t_s	typ.	6,5 μs

* Turn-off current.

Successor type is BU508

SILICON DIFFUSED POWER TRANSISTOR

High-voltage, high-speed switching n-p-n transistor in a metal envelope especially intended for use in supply and horizontal deflection systems of colour television receivers.

QUICK REFERENCE DATA

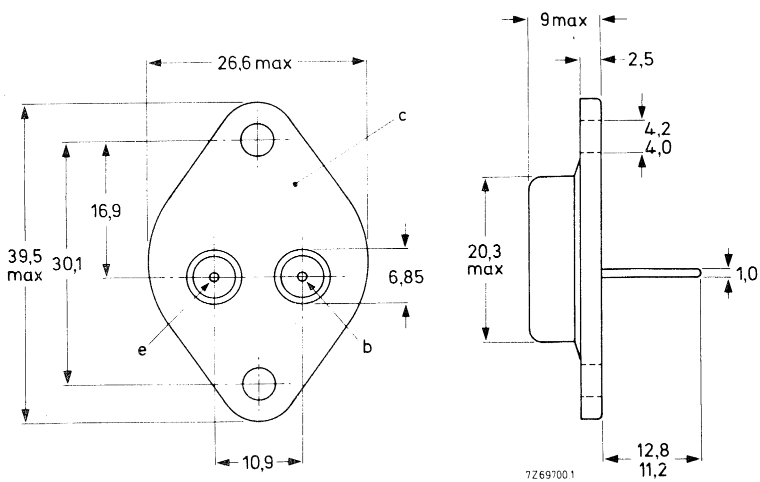
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	1500	V
Collector current (d.c.)	I_C	max.	5	A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	80	W
Collector-emitter saturation voltage I_C = 4,0 A; I_B = 2 A	V_{CEsat}	<	1	V
Fall time I_{CM} = 4,0 A; $I_{B(end)}$ = 1,4 A	t_f	typ.	0,7	μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Collector connected to case.



See also chapters Mounting instructions and Accessories.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	1500 V
Collector-emitter voltage ($R_{BE} \leq 100\ \Omega$, peak value)	V_{CERM}	max.	1500 V
Collector-emitter voltage (open base)	V_{CEO}	max.	700 V
Collector current (d.c.)	I_C	max.	5 A
Collector current (peak value)	I_{CM}	max.	7,5 A
Collector current (non-repetitive peak)	I_{CSM}	max.	15 A
Base current (peak value)	I_{BM}	max.	4 A
Reverse base current (d.c. or average over any 20 ms period)	$-I_{B(AV)}$	max.	100 mA
Reverse base current (peak value) *	$-I_{BM}$	max.	4 A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	80 W
Storage temperature	T_{stg}	−65 to + 115 °C	
Junction temperature	T_j	max.	115 °C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	max.	1,12 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current V_{BE} = 0; V_{CE} = $V_{CESMmax}$	I_{CES}	<	1,0 mA
D.C. current gain I_C = 4,0 A; V_{CE} = 5 V	h_{FE}	>	2,5
Emitter-base voltage I_C = 0; I_E = 10 mA	$+V_{EBO}$	>	5 V
I_C = 0; I_E = 100 mA	$+V_{EBO}$	typ.	7 V
Saturation voltage I_C = 4,0 A; I_B = 2 A	V_{CEsat}	<	1 V
I_C = 4,0 A; I_B = 2 A	V_{BEsat}	<	1,5 V

* Turn-off current.

SILICON DIFFUSED POWER TRANSISTORS

High-voltage, high-speed switching n-p-n power transistors in TO-3 envelopes, intended for use in the switched-mode power supply of 90° and 110° colour television receivers.

QUICK REFERENCE DATA

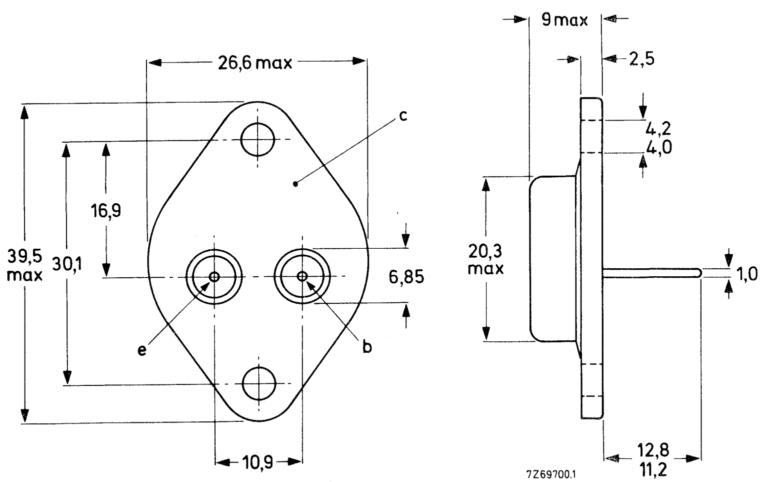
			BU326	BU326A	
Collector-emitter voltage (V_{BE} = 0; peak value)	V_{CESM}	max.	800	900	V
Collector-emitter voltage (open base)	V_{CEO}	max.	375	400	V
Collector current (d.c.)	I_C	max.	6		A
Collector current (peak value; t_p < 2 ms)	I_{CM}	max.	8		A
Total power dissipation up to T_{mb} = 50 °C	P_{tot}	max.	60		W
Collector-emitter saturation voltage I_C = 2,5 A; I_B = 0,5 A	V_{CEsat}	<	1,5		V
Fall time I_{Con} = 2,5 A; I_{Bon} = 0,5 A; $-I_{Boff}$ = 1 A	t_f	typ.	0,3		μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Collector connected to case.



See also chapters Mounting instructions and Accessories.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BU326	BU326A	
Collector-emitter voltage (V_{BE} = 0; peak value)	V_{CESM}	max.	800	900	V
Collector-emitter voltage (open base)	V_{CEO}	max.	375	400	V
Collector current (d.c.)	I_C	max.	6		A
Collector current (peak value; $t_p < 2$ ms)	I_{CM}	max.	8		A
Base current (d.c.)	I_B	max.	2		A
Base current (peak value)	I_{BM}	max.	3		A
Reverse base current (d.c. or average over any 20 ms period)	$-I_{B(AV)}$	max.	0,1		A
Reverse base current (peak value; turn-off current)	$-I_{BM}$	max.	3		A
Total power dissipation up to T_{mb} = 50 °C	P_{tot}	max.	60		W
Storage temperature	T_{stg}		−65 to + 150		°C
Junction temperature	T_j	max.	150		°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j-mb}$	=	1,65	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current *				
$V_{BE} = 0$; $V_{CEM} = V_{CESMmax}$	I_{CES}	<	1	mA
$V_{BE} = 0$; $V_{CEM} = V_{CESMmax}$; T_j = 125 °C	I_{CES}	<	2	mA
Emitter cut-off current				
$I_C = 0$; V_{EB} = 10 V	I_{EBO}	<	10	mA
Saturation voltages				
I_C = 2,5 A; I_B = 0,5	V_{CEsat}	<	1,5	V
	V_{BEsat}	<	1,4	V
I_C = 4 A; I_B = 1,25 A	V_{CEsat}	<	3	V
	V_{BEsat}	<	1,6	V
Collector-emitter sustaining voltage (see Figs 2 and 3)				
$I_{Boff} = 0$; I_C = 0,1 A; L = 25 mH BU326	$V_{CEOsust}$	>	375	V
BU326A	$V_{CEOsust}$	>	400	V
D.C. current gain				
I_C = 0,6 A; V_{CE} = 5 V	h_{FE}	typ.	30	
Transition frequency at f = 1 MHz				
I_C = 0,2 A; V_{CE} = 10 V	f_T	typ.	6	MHz

* Measured with a half sine-wave voltage (curve tracer).

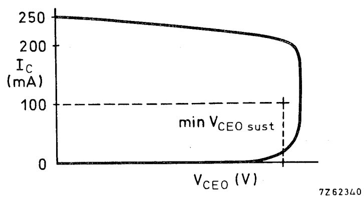


Fig. 2 Oscilloscope display for $V_{CEOsust}$.

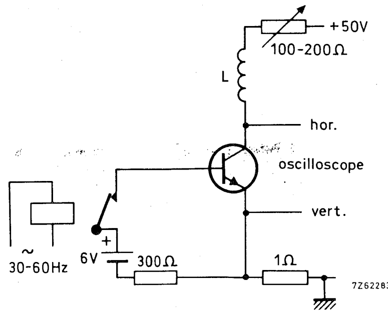


Fig. 3 Test circuit for $V_{CEOsust}$.

Switching times (see Figs 4 and 5)
I_{Con} = 2,5 A; V_{CC} = 250 V;
I_{Bon} = 0,5 A; $-I_{Boff}$ = 1 A

Turn-on time	t_{on}	typ.	0,3	μs
		<	0,5	μs
Turn-off time ($t_{off} = t_s + t_f$)				
Storage time	t_s	typ.	2	μs
		<	3,5	μs
Fall time	t_f	typ.	0,3	μs
Fall time at T_{mb} = 95 °C	t_f	<	1	μs

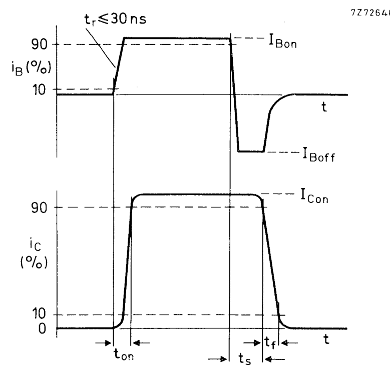
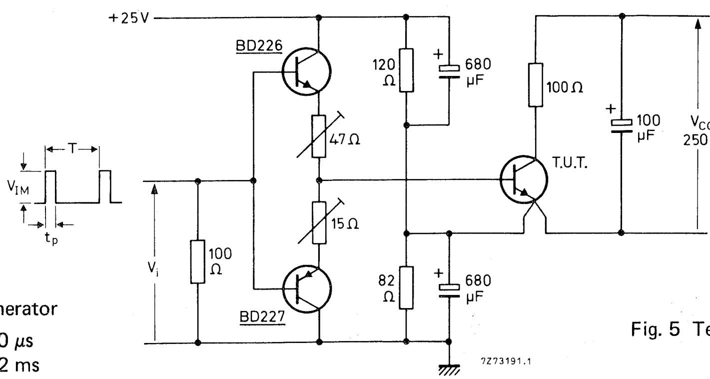


Fig. 4 Waveforms.



Pulse generator

t_p = 20 μs
T = 2 ms
V_{IM} = 15 V

Fig. 5 Test circuit.

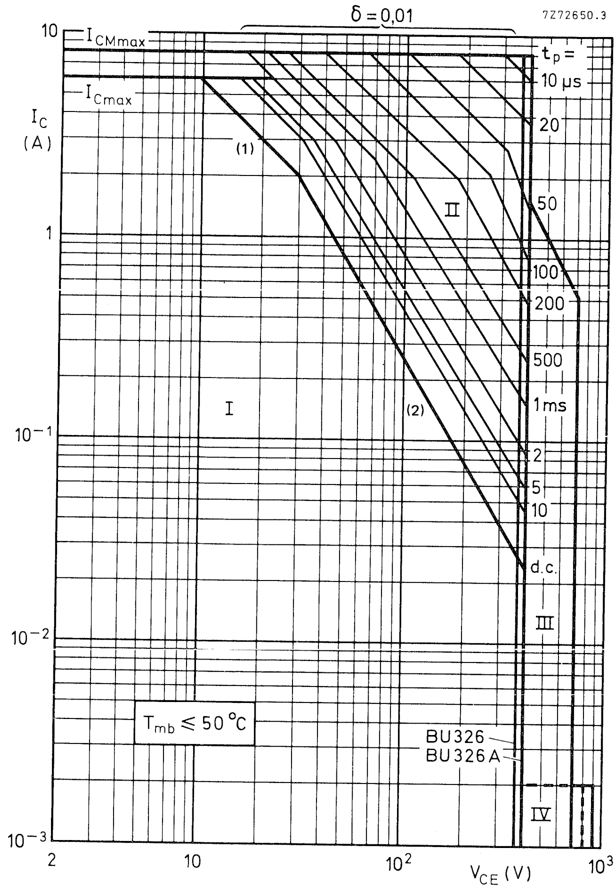


Fig. 6 Safe Operating ARea.

I Region of permissible d.c. operation

II Permissible extension for repetitive pulse operation

III Area of permissible operation during turn-on in single-transistor converters, provided $R_{BE} \leqslant 100\ \Omega$ and $t_p \leqslant 0{,}6\ \mu s$

IV Repetitive pulse operation in this region is permissible, provided $V_{BE} \leqslant 0$ and $t_p \leqslant 2$ ms

(1) $P_{tot\ max}$ and $P_{peak\ max}$ lines.

(2) Second-breakdown limits (independent of temperature).

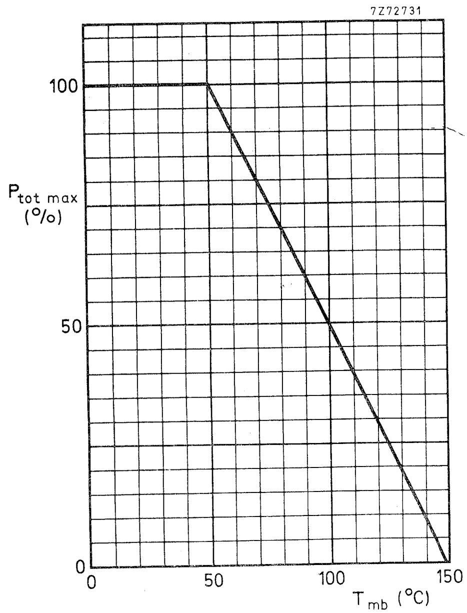


Fig. 7 Power derating curve.

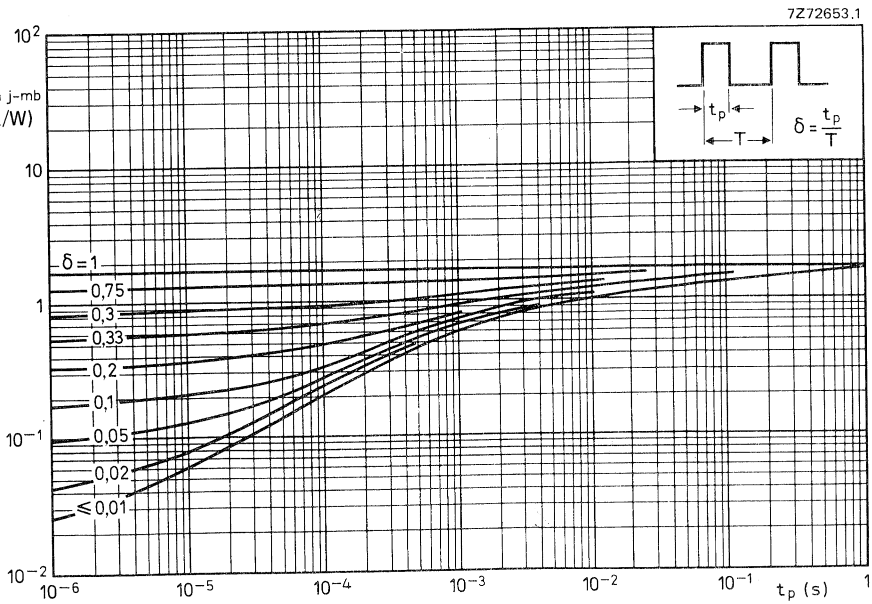


Fig. 8 Pulse power rating chart.

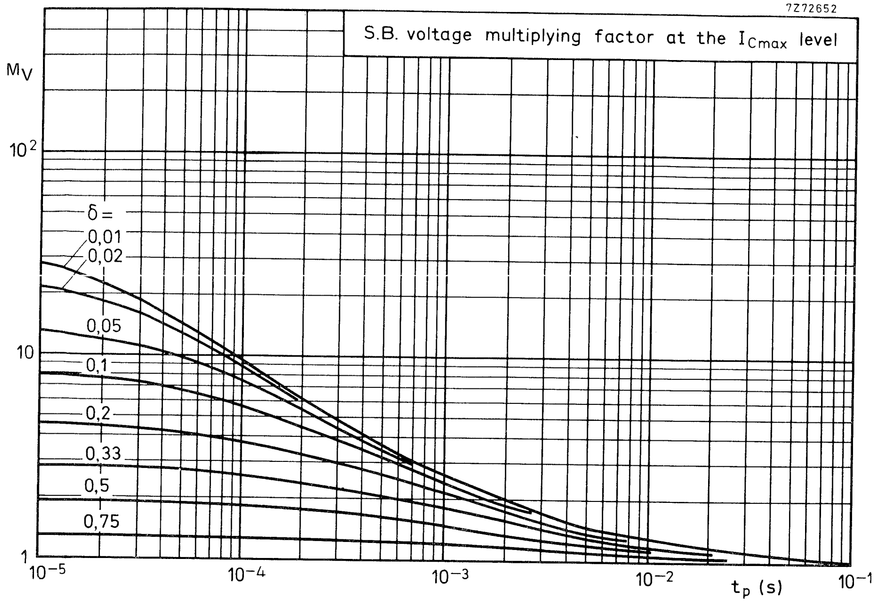


Fig. 9 S.B. voltage multiplying factor at the I_{Cmax} level.

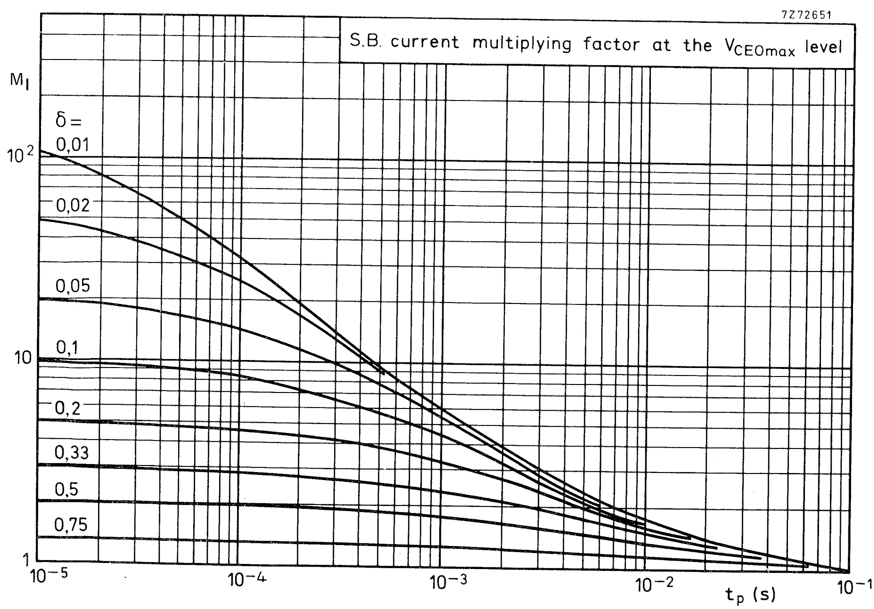


Fig. 10 S.B. current multiplying factor at the V_{CEOmax} level.

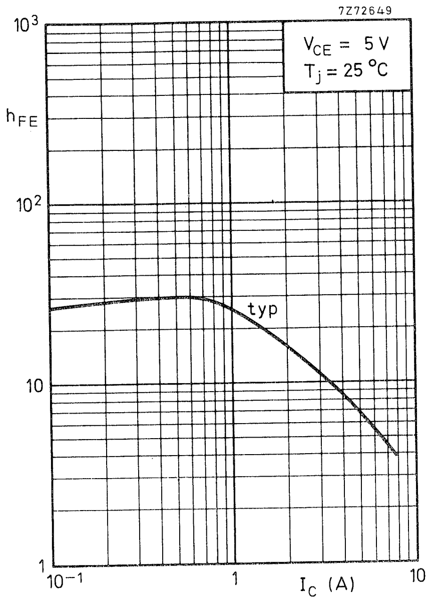


Fig. 11 D.C. current gain.

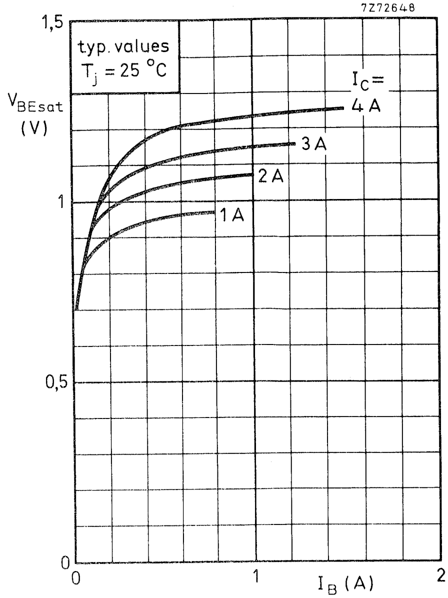


Fig. 12 Base-emitter saturation voltage.

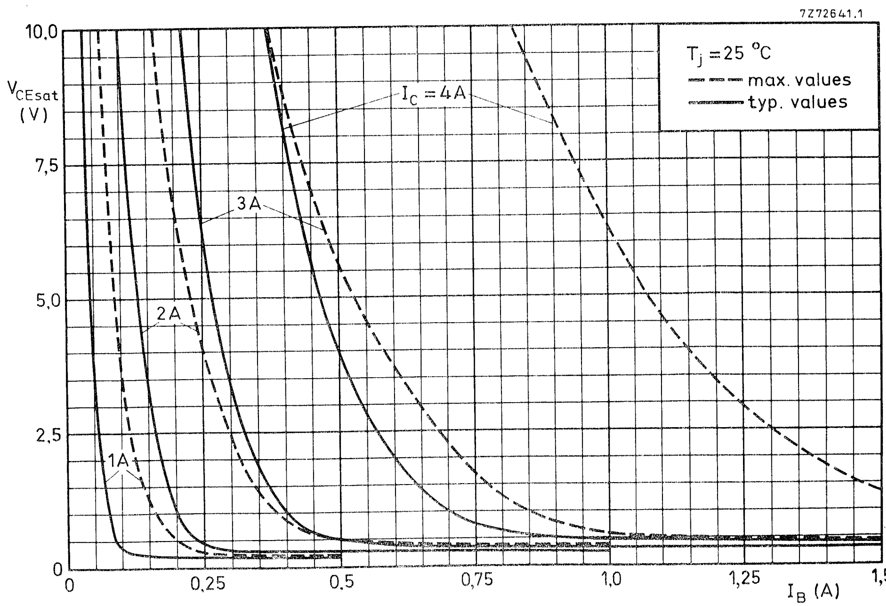


Fig. 13 Collector-emitter saturation voltage.

APPLICATION INFORMATION BU326A (detailed information on request)

Important factors in the design of SMPS circuits are the power losses and heatsink requirements of the supply output transistor and the base drive conditions during turn-off. In SMPS circuits for CTV receivers the duty factor of the collector current generally varies between 0,35 and 0,6.

The operating frequency lies between 15 kHz and 35 kHz and the shape of the collector current varies from rectangular in a forward converter to a sawtooth in a flyback circuit.

As the BU326A will mainly be used in flyback converters the information on optimum base drive and device dissipation given in the graphs on page 10 is concentrated on this application. In these figures I_{CM} represents the highest repetitive peak collector current that can occur in the given circuit, e.g. during overload.

The total power dissipation for a limit-case transistor is given in Fig. 18 which applies for a mounting base temperature of 100 °C. The required thermal resistance for the heatsink can be calculated from

$$R_{th\ mb\text{-}a\ max}{}^{*} = \frac{T_{mb\ max} - T_{amb\ max}}{P_{tot}}$$

* Including additional thermal resistances resulting from mounting hardware.

To ensure thermal stability the thermal resistance of the heatsink used must not exceed the values plotted in Fig. 19.

A practical SMPS output circuit for an output power in the order of 180 W is given in Fig. 15.

At a collector current of 2,5 A and a base current of 0,25 A in this circuit the following turn-off times can be expected.

			T_{mb} = 25 °C	= 100 °C	
Storage time	t_s	typ.	1,4	< 2,0	μs
Fall time	t_f	typ.	0,15	< 0,5	μs

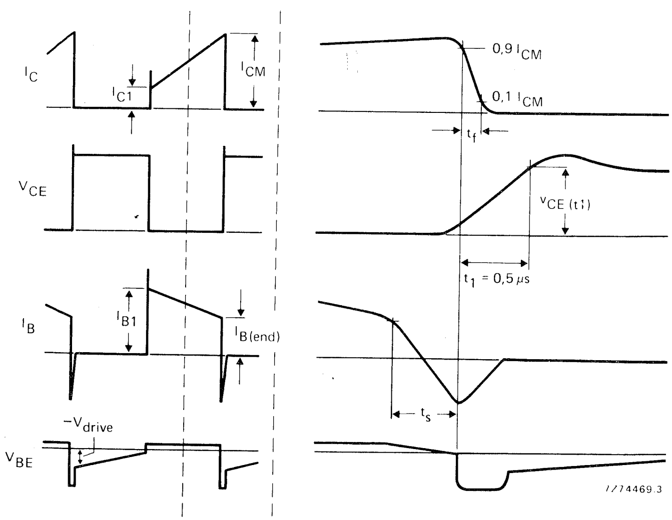


Fig. 14 Relevant waveforms of switching transistor.

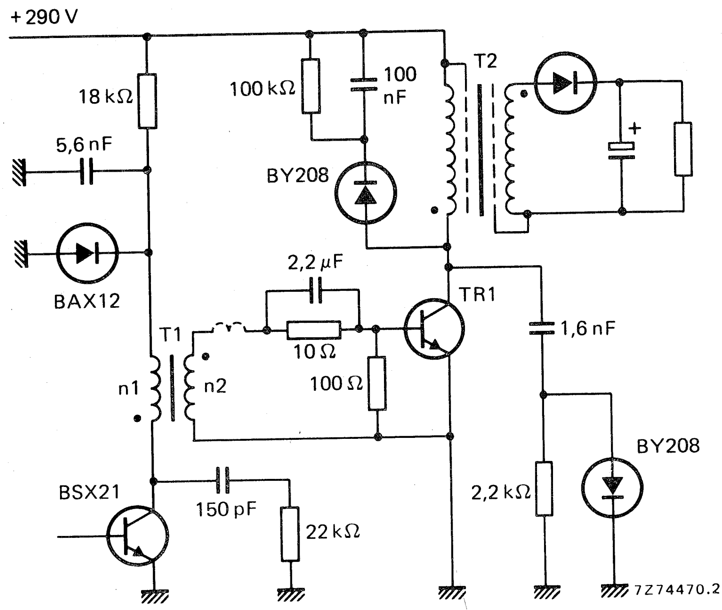


Fig. 15 Practical SMPS output circuit.

TR1 = BU326A
T1 (driver transformer): Core U20; n1 = 400 turns; n2 = 25 turns
total inductance in base circuit ≈ 4,5 μH
T2 (output transformer): L_p = 6 mH
$v_{CE(t1)}$ < 500 V (see Fig. 14)

Next page:

Fig. 16 Recommended nominal "end" value of the base current versus maximum peak collector current.

Fig. 17 Minimum required base inductance and recommended negative drive voltage versus maximum peak collector current.

Fig. 18 Maximum total power dissipation of a limit-case transistor if the base current is chosen in accordance with Fig. 16.

Fig. 19 Maximum permissible thermal resistance of the heatsink versus maximum peak collector current to ensure thermal stability.

Note: For all curves the duty factor δ = 0,5, as shown in Fig. 14.

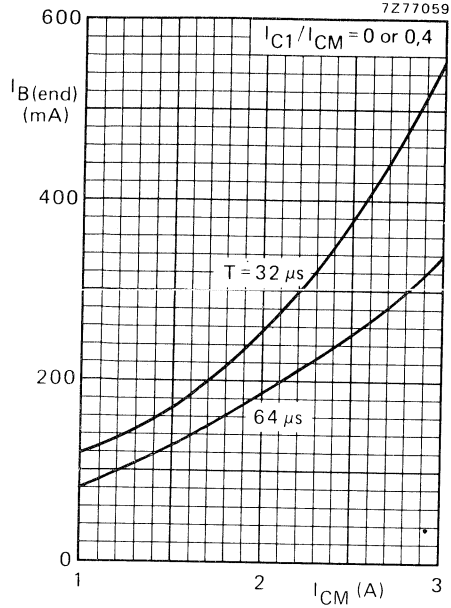


Fig. 16.

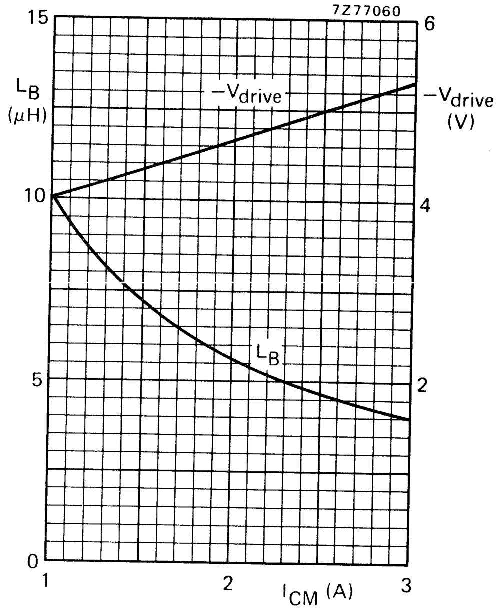


Fig. 17.

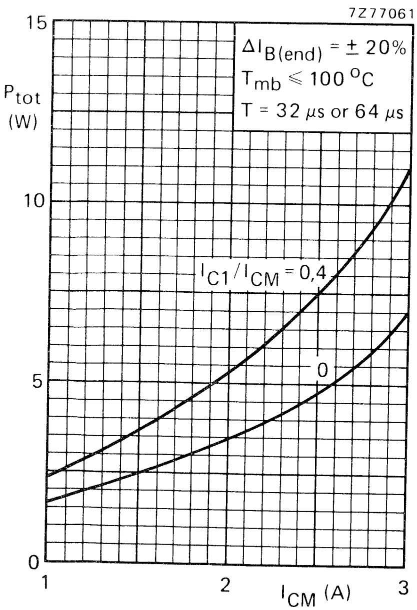


Fig. 18.

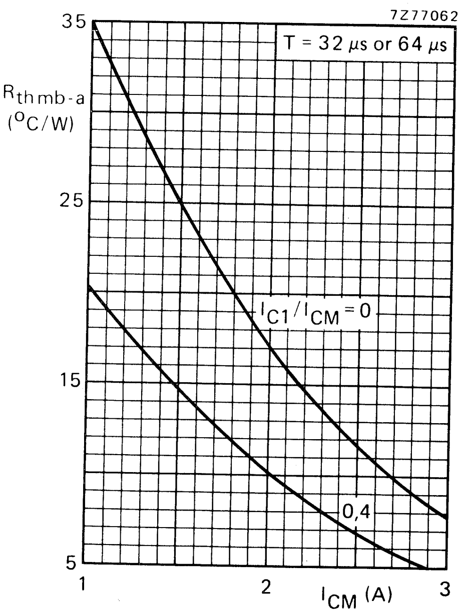


Fig. 19.

SILICON DIFFUSED POWER TRANSISTORS

High voltage, high speed switching n-p-n power transistor in plastic SOT-93 envelope, intended for use in the switched-mode power supply of 90° and 110° colour television receivers.

QUICK REFERENCE DATA

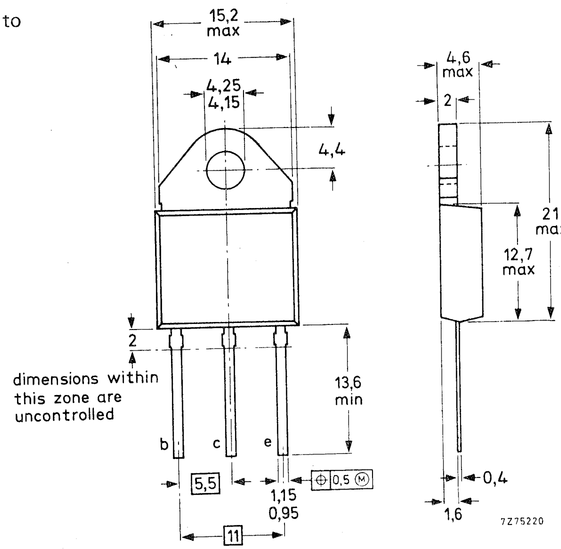
			BU426	426A	433	
Collector-emitter voltage (V_{BE} = 0; peak value)	V_{CESM}	max.	800	900	800	V
Collector-emitter voltage (open base)	V_{CEO}	max.	375	400	375	V
Collector current (d.c.)	I_C	max.		6		A
Collector current (peak value) t_p = 2 ms	I_{CM}	max.		10		A
Total power dissipation up to T_{mb} = 73 °C	P_{tot}	max.		70		W
Collector-emitter saturation voltage I_C = 2,5 A; I_B = 0,5 A	V_{CEsat}	<		1,5		V
Fall time I_{Con} = 2,5 A; I_{Bon} = 0,5 A; $-I_{Boff}$ = 1 A	t_f	typ.	0,3	0,3	0,45	μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-93.

Collector connected to mounting base



See also chapters Mounting instructions and Accessories.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BU426	426A	433	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	800	900	800	V
Collector-emitter voltage (open base)	V_{CEO}	max.	375	400	375	V
Collector current (d.c.)	I_C	max.		6		A
Collector current (peak value) $t_p < 2$ ms	I_{CM}	max.		10		A
Base current (d.c.)	I_B	max.		2		A
Base current (peak value)	I_{BM}	max.		3		A
Reverse base current (d.c. or average over any 20 ms period)	$-I_{B(AV)}$	max.		100		mA
Reverse base current (peak value)*	$-I_{BM}$	max.		3		A
Total power dissipation up to T_{mb} = 73 °C	P_{tot}	max.		70		W
Storage temperature	T_{stg}			−65 to + 150		°C
Junction temperature	T_j	max.		150		°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1,1	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current **				
V_{CEM} = 900 V; V_{BE} = 0	I_{CES}	<	1	mA
V_{CEM} = 900 V; V_{BE} = 0; T_j = 125 °C	I_{CES}	<	2	mA
D.C. current gain				
I_C = 0,6 A; V_{CE} = 5 V; BU426; BU426A	h_{FE}	typ. <	30 60	
I_C = 0,6 A; V_{CE} = 5 V; BU433	h_{FE}	typ.	40	
Transition frequency at f = 1 MHz				
I_C = 0,2 A; V_{CE} = 10 V	f_T	typ.	6	MHz

* Turn-off current.
** Measured with a half sine-wave voltage (curve tracer).

CHARACTERISTICS (continued)

T_j = 25 °C unless otherwise specified

Emitter cut-off current			
I_C = 0; V_{EB} = 10 V	I_{EBO}	<	10 mA
Saturation voltages			
I_C = 2,5 A; I_B = 0,5 A	V_{CEsat}	<	1,5 V
	V_{BEsat}	<	1,4 V
I_C = 4 A; I_B = 1,25 A	V_{CEsat}	<	3 V
	V_{BEsat}	<	1,6 V
Collector-emitter sustaining voltage			
I_C = 100 mA; I_{Boff} = 0; L = 25 mH; BU426; BU433	$V_{CEOsust}$	>	375 V
I_C = 100 mA; I_{Boff} = 0; L = 25 mH; BU426A	$V_{CEOsust}$	>	400 V

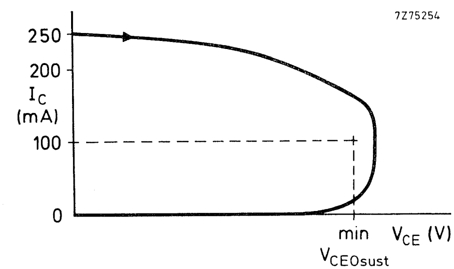


Fig. 2 Oscilloscope display for $V_{CEOsust}$.

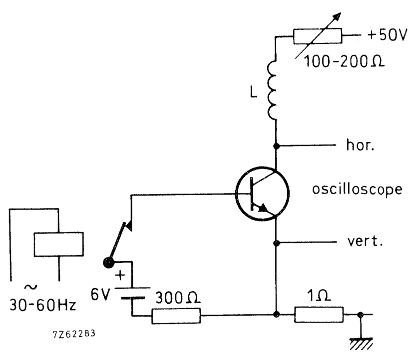


Fig. 3 Test circuit for $V_{CEOsust}$.

CHARACTERISTICS (continued)

Switching times (between 10% and 90% levels)

I_{Con} = 2,5 A; V_{CC} = 250 V

I_{Bon} = 0,5 A; $-I_{Boff}$ = 1 A

Turn-on time		t_{on}	typ.	0,5	μs
			<	0,6	μs
Turn-off time ($t_{off} = t_s + t_f$): Storage time		t_s	typ.	2	μs
			<	3,5	μs
Fall time	BU426; 426A	t_f	typ.	0,3	μs
	BU433	t_f	typ.	0,45	μs
			<	0,7	μs
Fall time, T_{mb} = 95 °C	BU433	t_f	typ.	0,7	μs
			<	1,0	μs
	BU426; 426A	t_f	<	0,75	μs

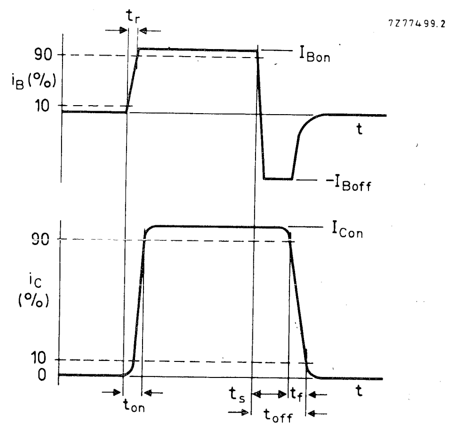


Fig. 4 Waveforms.

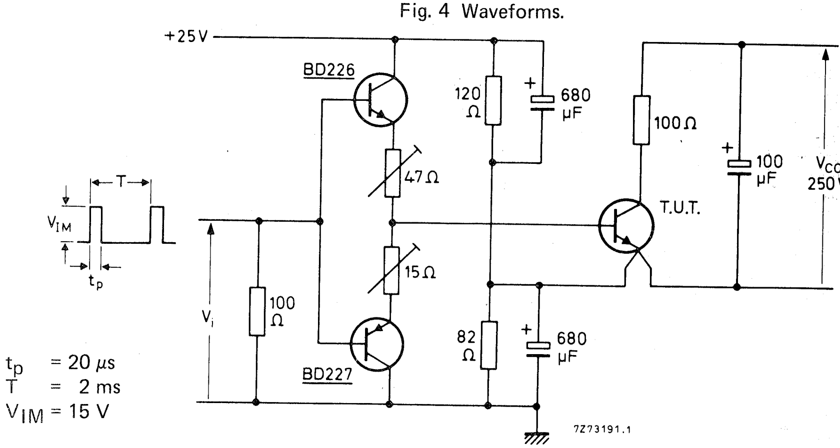


Fig. 5 Test circuit.

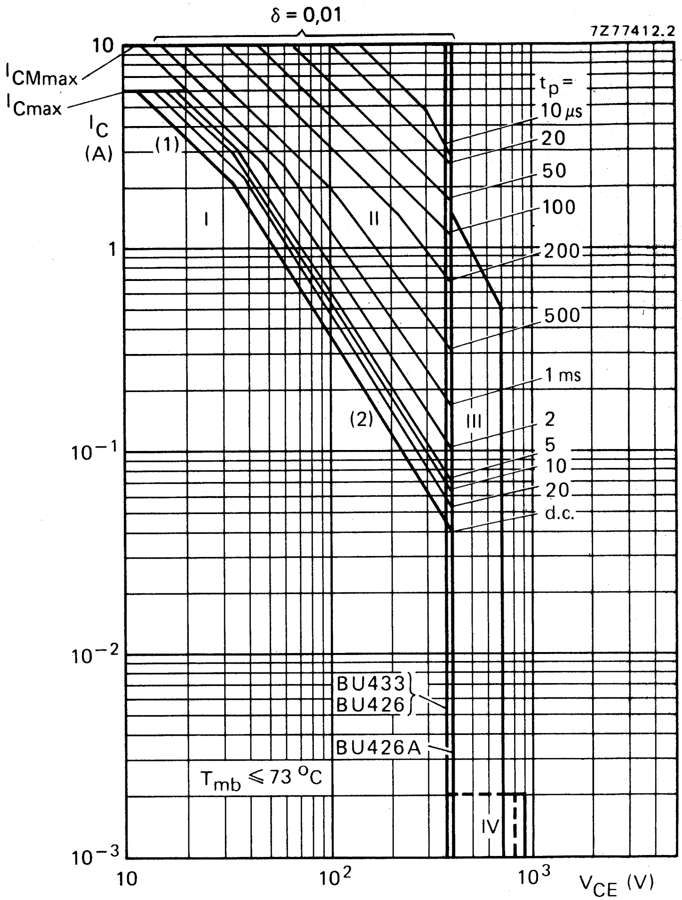


Fig. 6 Safe Operating ARea.

I Region of permissible d.c. operation.

II Permissible extension for repetitive pulse operation.

III Area of permissible operation during turn-on in single-transistor converters, provided $R_{BE} \leqslant 100\ \Omega$ and $t_p \leqslant 0{,}6\ \mu s$.

IV Repetitive pulse operation in this region is permissible, provided $V_{BE} \leqslant 0$ and $t_p \leqslant 2$ ms.

(1) $P_{tot\ max}$ and $P_{peak\ max}$ lines.

(2) Second-breakdown limits (independent of temperature).

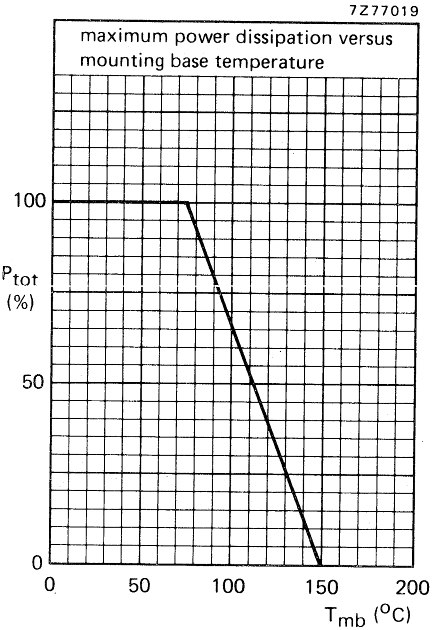


Fig. 7 Power derating curve.

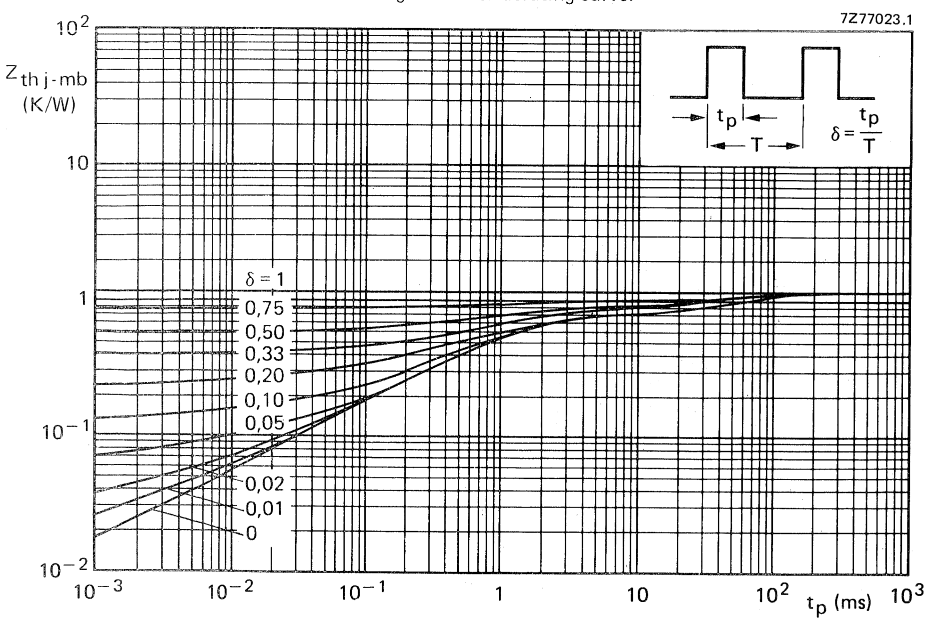


Fig. 8 Pulse power rating chart.

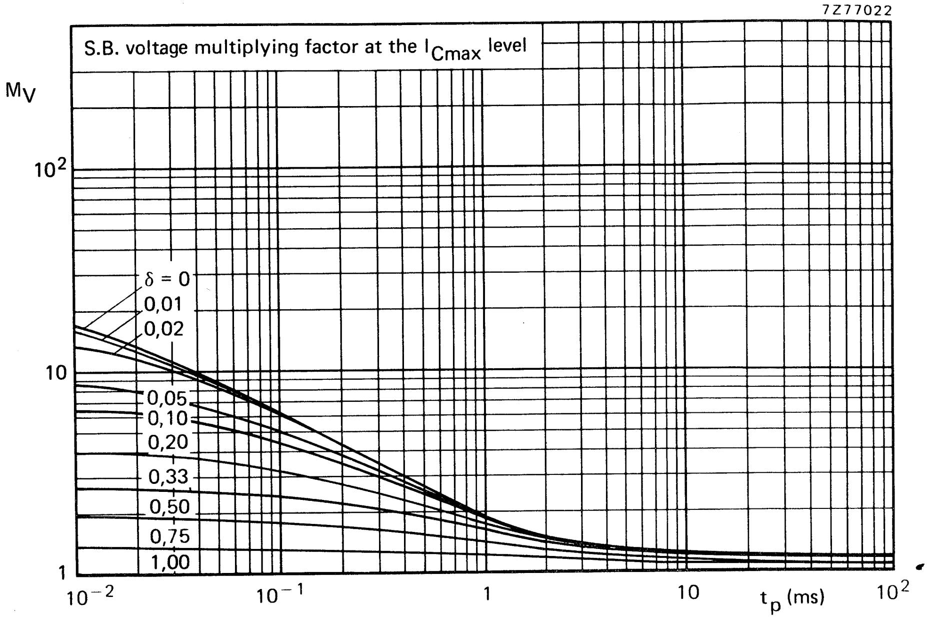


Fig. 9 S.B. voltage multiplying factor at the I_{Cmax} level.

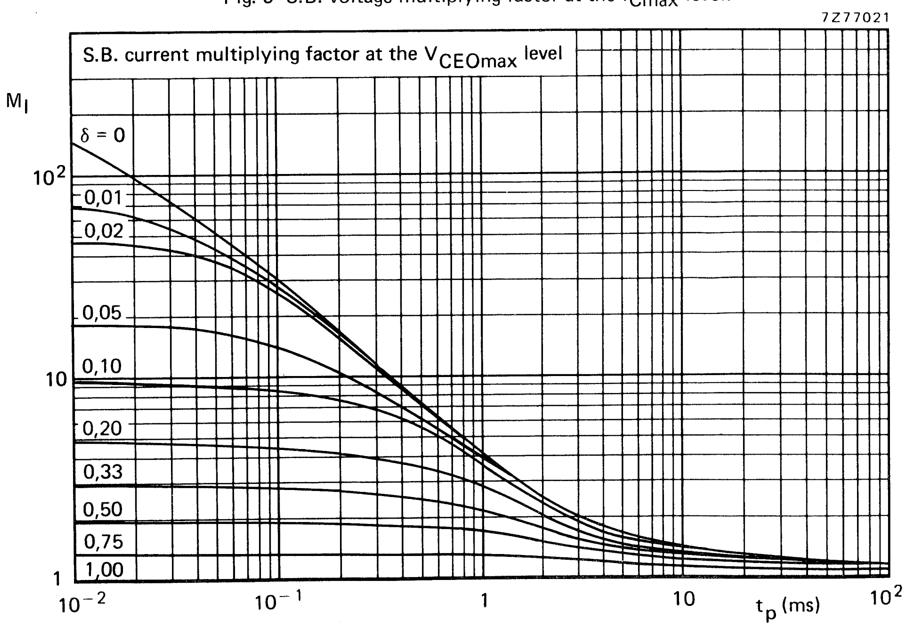


Fig. 10 S.B. current multiplying factor at the V_{CEOmax} level.

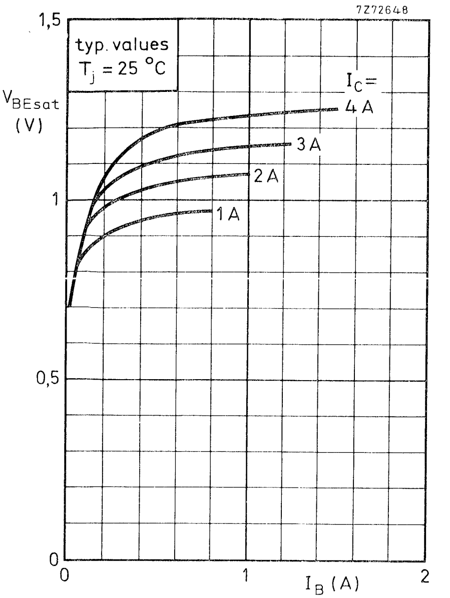


Fig. 11 Typical values. Base-emitter saturation voltage for BU426 and BU426A.

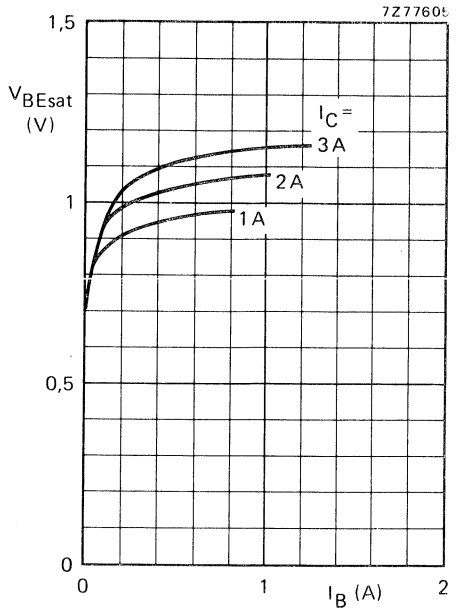


Fig. 11A. Typical values. Base-emitter saturation voltage for BU433; T_j = 25 °C.

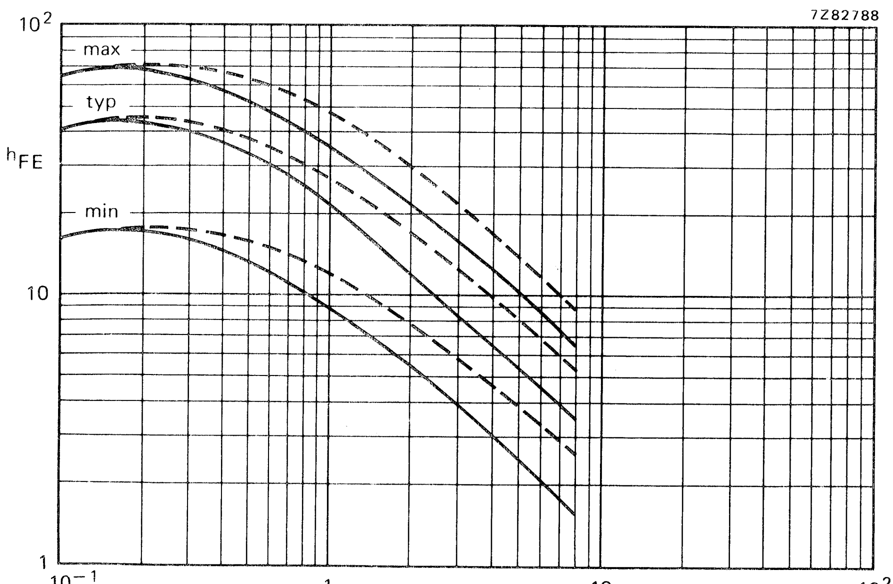


Fig. 12 D.C. current gain BU426 and BU426A. T_j = 25 °C. – – – – at V_{CE} = 5 V; ——— at V_{CE} = 1 V.

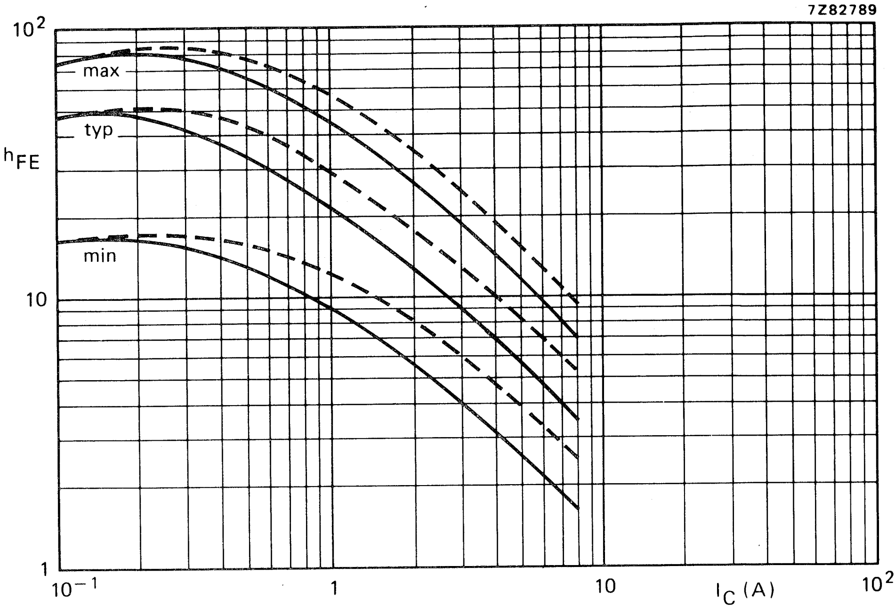


Fig. 13 D.C. current gain BU433; T_j = 25 °C; – – – – at V_{CE} = 5 V; ——— at V_{CE} = 1 V.

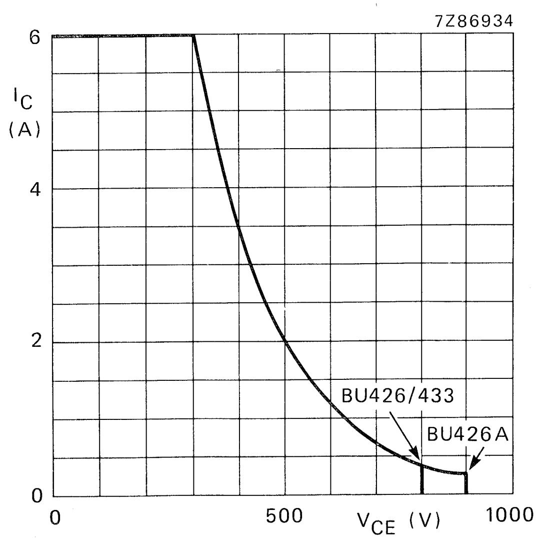


Fig. 14 Reverse bias SOAR.
$-V_{drive}$ = 2 to 6 V; L_B = 0 to 4,7 μH; T_{mb} = 100 °C.

APPLICATION INFORMATION (detailed information on request)

Important factors in the design of SMPS circuits are the power losses and heatsink requirements of the supply output transistor and the base drive conditions during turn-off. In SMPS circuits for CTV receivers the duty factor of the collector current generally varies between 0,35 and 0,6.

The operating frequency lies between 15 kHz and 35 kHz and the shape of the collector current varies from rectangular in a forward converter to a sawtooth in a flyback circuit.

All these variables influence the collector dissipation, so that a simple presentation of the design information is only possible if the information is restricted to the main application area of the relevant transistor type. Therefore, as the BU426 or BU426A will mainly be used in flyback converters and the BU433 in forward SMPS, the information of Figs 17 up to 22 is based on these applications:

The total power dissipation for a limit-case transistor BU426 or BU433 is given in Figs 19 and 22, which apply for a mounting base temperature of 100 °C. The required thermal resistance for the heatsink can be calculated from:

$$R_{th\ mb\text{-}a\ max}{}^{*} = \frac{T_{mb\ max} - T_{amb\ max}}{P_{tot}}$$

* Including additional thermal resistances resulting from mounting hardware.

To ensure thermal stability minimum value of T_{amb} in this equation is 40 °C. As indicated, the BU433 will mainly be used in (non-isolated) forward converters, where the turn-off losses are limited by the maximum collector emitter voltage ($\approx$ 300-350 V). The rate-of-rise of the voltage during turn-off must be below 1000 V/μs. Application of this transistor in low-power flyback converters is also possible, provided that the rate-of-rise is limited to 500 V/μs. For the BU426(A) a rate-of-rise of 1000 V/μs is permissible. Practical SMPS output circuits for an output power in the order of 180 W are given in Figs 17 and 20. At a collector current of 2,5 A and a base current of 0,25 A in these circuits the following turn-off times can be expected.

		T_{mb} = 25 °C	T_{mb} = 100 °C
BU426 (426A)	Storage time t_s	typ. 1,4	< 2,0 μs
	Fall time t_f	0,15	< 0,5 μs
BU433	Storage time t_s	typ. 1,4	< 2,0 μs
	Fall time t_f	0,18	< 0,6 μs

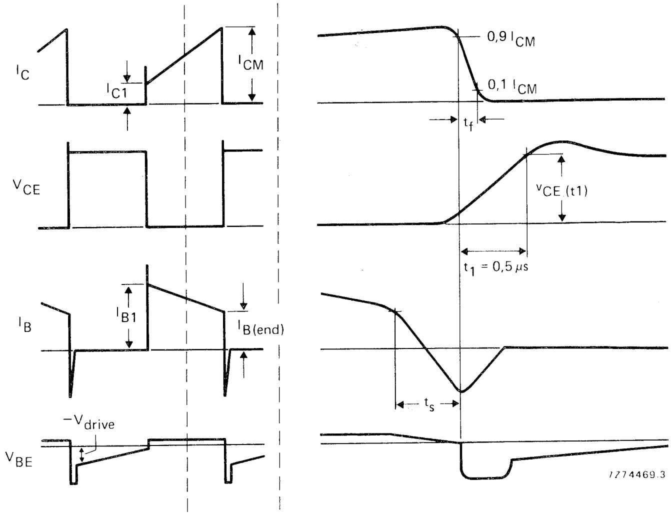


Fig. 15 Relevant waveforms of switching transistor.

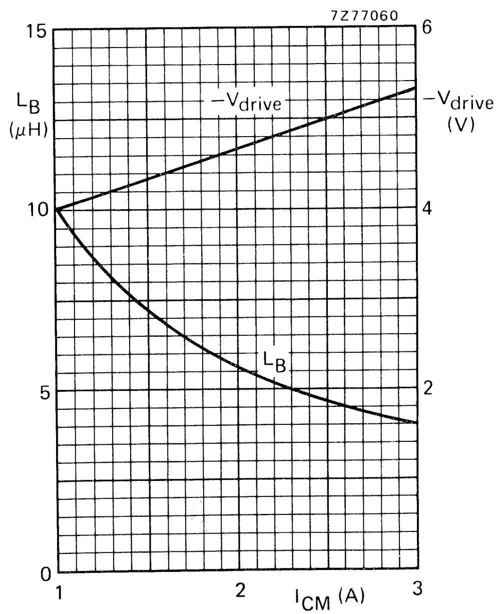


Fig. 16 Minimum required base inductance and recommended negative drive voltage versus maximum peak collector current.

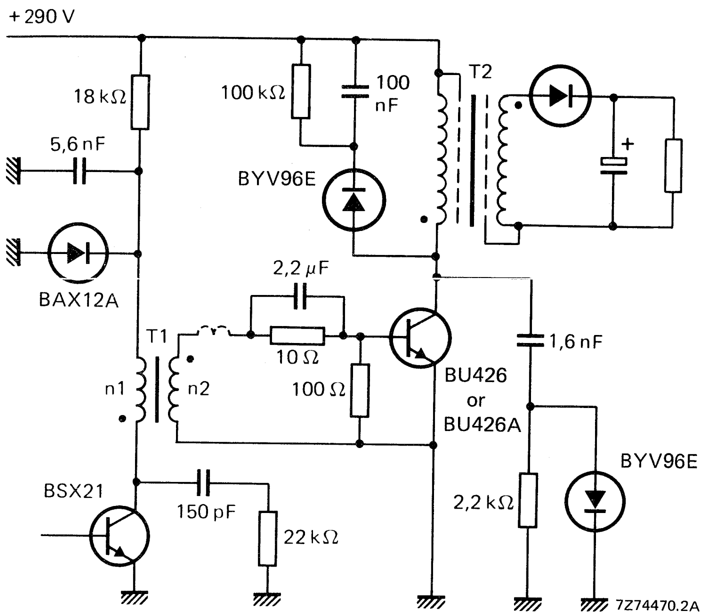


Fig. 17 Practical output circuit of a flyback SMPS of BU426 or BU426A.

T1 (driver transformer)
core U20; n1 = 400 turns
n2 = 25 turns

$L_{Btot} \approx 4,5\ \mu H$

T2 (output transformer)
$L_p = 6$ mH
$V_{CE(t1)} < 500$ V (see Fig. 15)

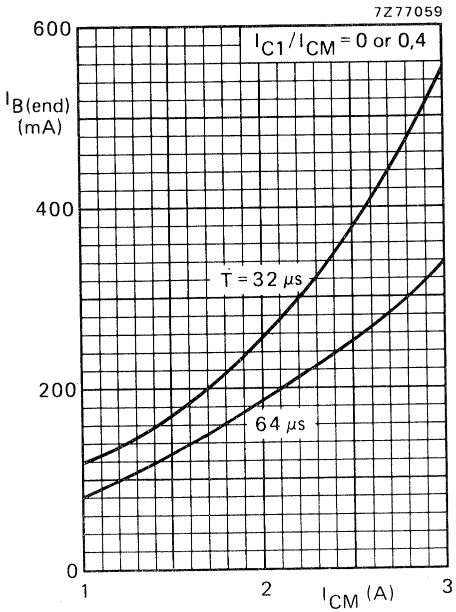


Fig. 18 Recommended nominal "end" value of the base current versus maximum peak collector current.

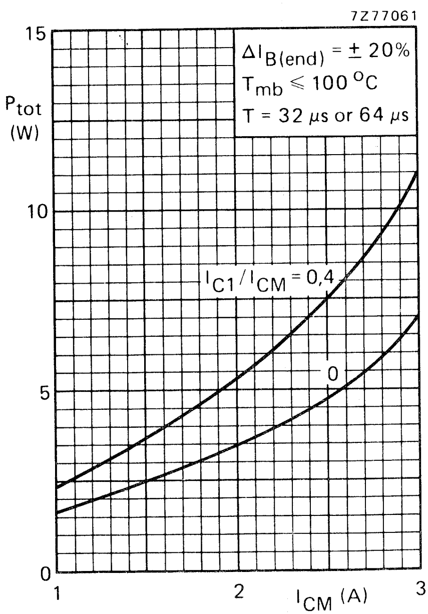


Fig. 19 Maximum total power dissipation of a limit-case transistor of the base current is chosen in accordance with Fig. 18.

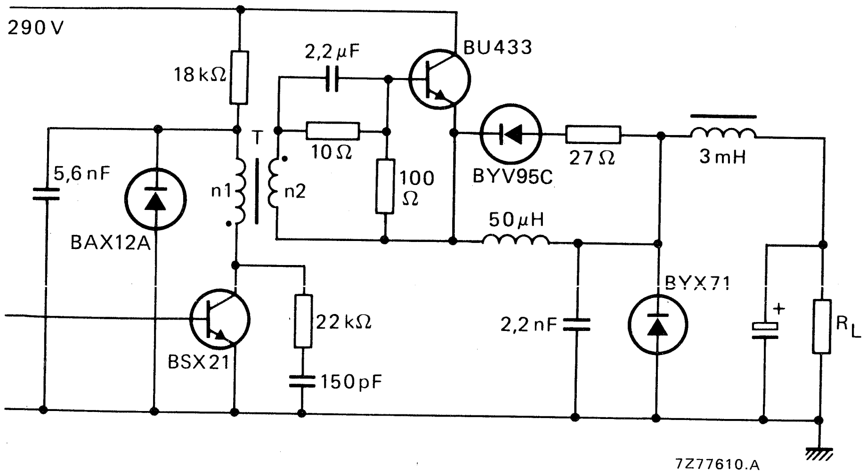


Fig. 20 Practical output circuit of a forward SMPS with BU433.
T (driver transformer): Core U20
n1 = 400 turns; n2 = 25 turns
$L_{Btot} \approx 4{,}5\ \mu H$

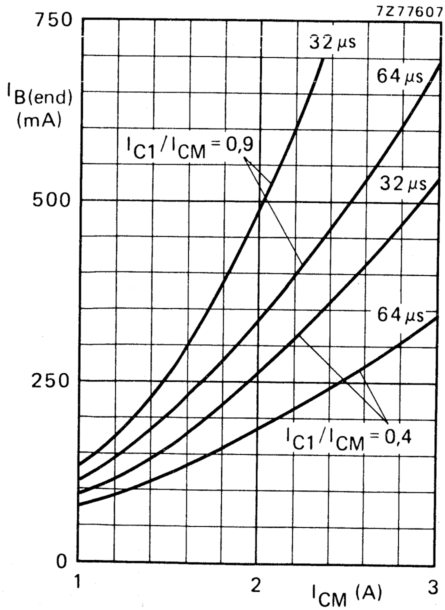


Fig. 21 Recommended nominal "end" value of the base current versus maximum peak collector current.

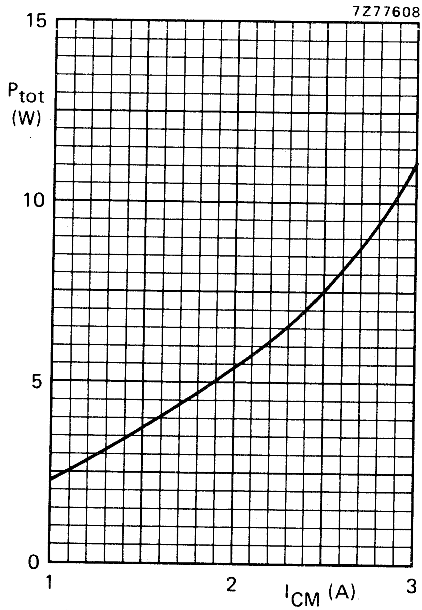


Fig. 22 Maximum total power dissipation of a limit-case transistor if the base current is chosen in accordance with Fig. 21.

SILICON POWER TRANSISTOR

High-voltage, high-speed switching, glass passivated n-p-n power transistor in a TO-220 envelope, intended for use in horizontal deflection circuits of television receivers.

QUICK REFERENCE DATA

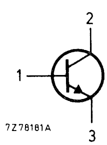
Collector-emitter voltage (V_{BE} = 0; peak value)	V_{CESM}	max.	1500 V
Collector-emitter voltage (open base)	V_{CEO}	max.	700 V
Collector current (d.c.)	I_C	max.	2,5 A
Collector current (peak value, t_p = 2 ms)	I_{CM}	max.	4 A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	75 W
Collector-emitter saturation voltage I_C = 2 A; I_B = 0,9 A	V_{CEsat}	<	5 V
Fall time I_{Con} = 2 A; I_{Bon} = 0,9 A	t_f	typ.	0,7 μs

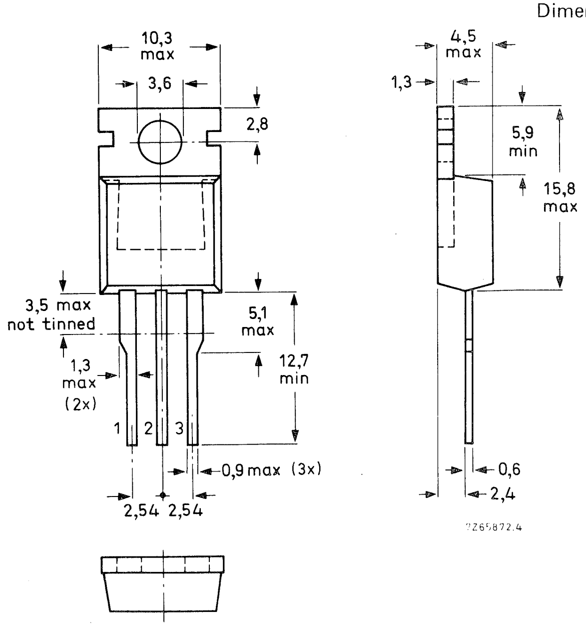
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220.

Collector connected to mounting base





See also chapters Mounting instructions and Accessories.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage (peak value; $V_{BE} = 0$)	V_{CESM}	max.	1500	V
Collector-emitter voltage (open base)	V_{CEO}	max.	700	V
Collector current (d.c.)	I_C	max.	2,5	A
Collector current (peak value); $t_p < 2$ ms	I_{CM}	max.	4	A
Base current (d.c.)	I_B	max.	2	A
Base current (peak value); $t_p < 2$ ms	I_{BM}	max.	4	A
Total power dissipation up to $T_{mb} = 25\ ^oC$	P_{tot}	max.	75	W
Storage temperature	T_{stg}	−65 to	+150	^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1,67	K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Collector cut off current*				
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$	I_{CES}	<	0,15	mA
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$; $T_j = 125\ ^oC$	I_{CES}	<	1	mA
Emitter cut-off current				
$I_C = 0$; $V_{EB} = 5$ V	I_{EBO}	<	1	mA
Saturation voltages				
$I_C = 2$ A; $I_B = 0{,}9$ A	V_{CEsat}	<	5	V
	V_{BEsat}	<	1,3	V
Collector-emitter sustaining voltage				
$I_C = 100$ mA; $I_B = 0$; $L = 50$ mH	$V_{CEOsust}$	>	700	V
D.C. current gain				
$I_C = 2$ A; $V_{CE} = 5$ V	h_{FE}	>	2,22	

* Measured with a half sine-wave voltage (curve tracer).

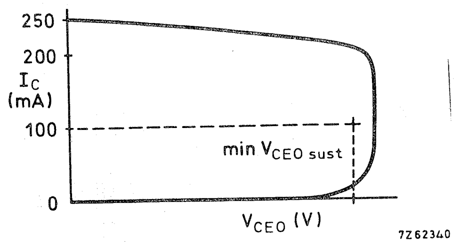


Fig. 2 Oscilloscope display for sustaining voltage.

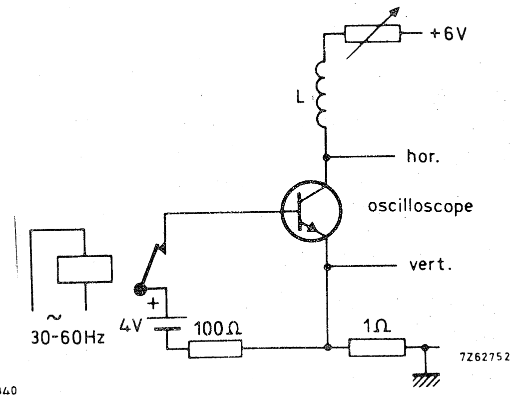


Fig. 3 Test circuit for $V_{CEOsust}$.

DEVELOPMENT SAMPLE DATA

Second-breakdown current V_{CE} = 120 V; T = 200 μs	I_{SB}	>	2 A
Transition frequency at f = 5 MHz I_C = 0,1 A; V_{CE} = 5 V	f_T	typ.	7 MHz
Collector capacitance at f = 1 MHz I_E = I_e = 0; V_{CB} = 10 V	C_c	typ.	65 pF
Switching times in horizontal deflection circuit $-V_{IM}$ = 4 V; L_B = 25 μH; I_{CM} = 2 A; $I_{B(end)}$ = 0,9 A			
fall time	t_f	typ.	0,7 μs
storage time	t_s	typ.	10 μs

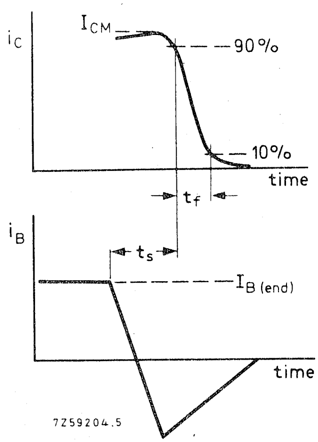


Fig. 4 Switching times waveforms.

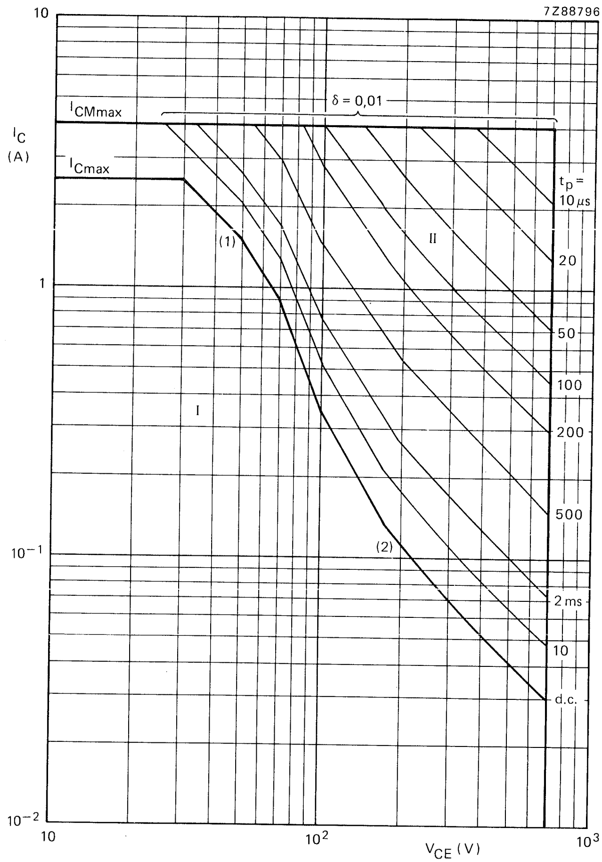


Fig. 5 Safe Operating ARea at $T_{mb} \leqslant 25\ ^{o}C$.

I Region of permissible d.c. operation.

II Permissible extension for repetitive pulse operation.

(1) $P_{tot\ max}$ and $P_{tot\ peak\ max}$ lines.

(2) Second-breakdown limits (independent of temperature).

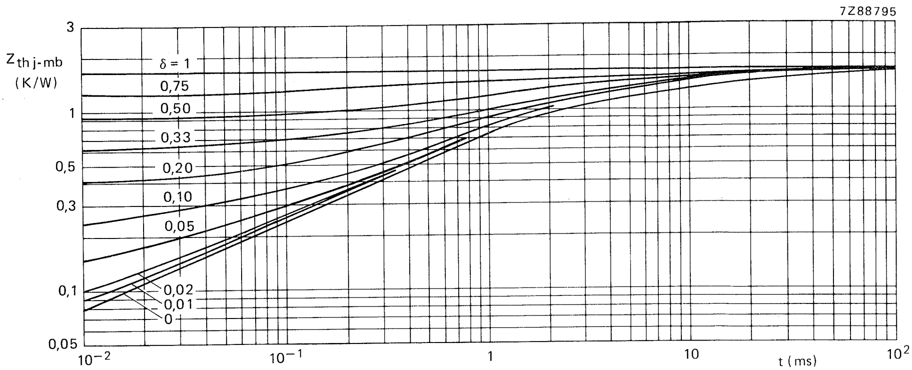


Fig. 6 Pulse power rating chart.

DEVELOPMENT SAMPLE DATA

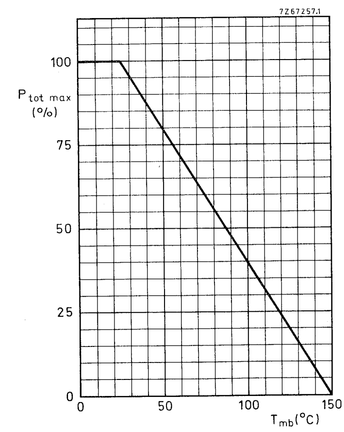


Fig. 7 Power derating curve.

SILICON DIFFUSED POWER TRANSISTOR

High-voltage, high-speed switching n-p-n transistor in a plastic envelope intended for use in horizontal deflection circuits of colour television receivers.

QUICK REFERENCE DATA

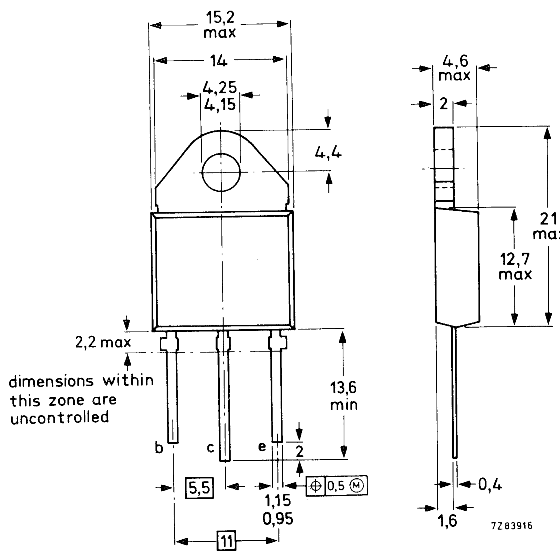
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	1500 V
Collector-emitter voltage (open base)	V_{CEO}	max.	700 V
Collector current (d.c.)	I_C	max.	8 A
Collector current (peak value)	I_{CM}	max.	15 A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	125 W
Collector-emitter saturation voltage I_C = 4,5 A; I_B = 2 A	V_{CEsat}	<	1 V
Saturation collector current	I_{Csat}	typ.	4,5 A
Fall time I_{CM} = 4,5 A; $I_{B(end)}$ = 1,4 A	t_f	typ.	0,7 μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-93A.

Collector connected to mounting base.



See also chapters Mounting instructions and Accessories.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	1500 V
Collector-emitter voltage (open base)	V_{CEO}	max.	700 V
Collector current (d.c.)	I_C	max.	8 A
Collector current (peak value)	I_{CM}	max.	15 A
Base current (d.c.)	I_B	max.	4 A
Base current (peak value)	I_{BM}	max.	6 A
Reverse base current (d.c. or average over any 20 ms period)	$-I_{B(AV)}$	max.	100 mA
Reverse base current * (peak value)	$-I_{BM}$	max.	5 A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	125 W
Storage temperature	T_{stg}		−65 to +150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current *			
$V_{BE} = 0$; $V_{CE} = V_{CESMmax}$	I_{CES}	<	1,0 mA
$V_{BE} = 0$; $V_{CE} = V_{CESMmax}$; T_j = 125 °C	I_{CES}	<	2,0 mA
Emitter cut-off current V_{EB} = 6 V; I_C = 0	I_{EBO}	<	10 mA
Saturation collector current V_{CEsat} < 1 V	I_{Csat}	typ.	4,5 A
Collector-emitter sustaining voltage I_B = 0; I_C = 100 mA; L = 25 mH	$V_{CEOsust}$	>	700 V
Saturation voltage			
I_C = 4,5 A; I_B = 2 A	V_{CEsat}	<	1 V
I_C = 4,5 A; I_B = 2 A	V_{BEsat}	<	1,3 V
Transition frequency at f = 5 MHz I_C = 0,1 A; V_{CE} = 5 V	f_T	typ.	7 MHz
Collector capacitance at f = 1 MHz $I_E = I_e = 0$; V_{CB} = 10 V	C_c	typ.	125 pF
Second-breakdown current V_{CE} = 120 V; t = 200 µs	$I_{(SB)}$	>	11 A

* Turn-off current.

** Measured with a half-sinewave voltage (curve tracer).

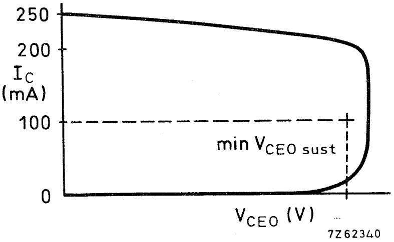


Fig. 2 Oscilloscope display for $V_{CEOsust}$.

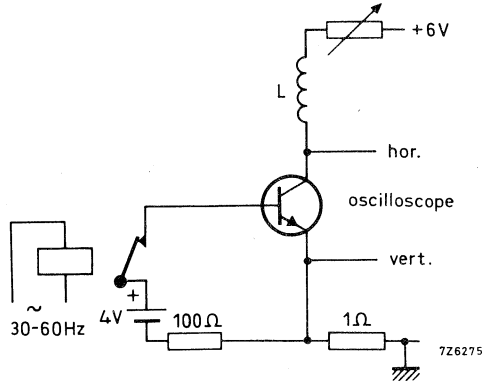


Fig. 3 Test circuit for $V_{CEOsust}$.

Switching times (in line deflection circuit)
L_B = 6 μH; $-V_{IM}$ = 4 V;
I_{CM} = 4,5 A; $I_{B(end)}$ = 1,4 A
($-dI_B/dt$ = 0,6 A/μs)

t_f	typ.	0,7 μs
t_s	typ.	6,5 μs

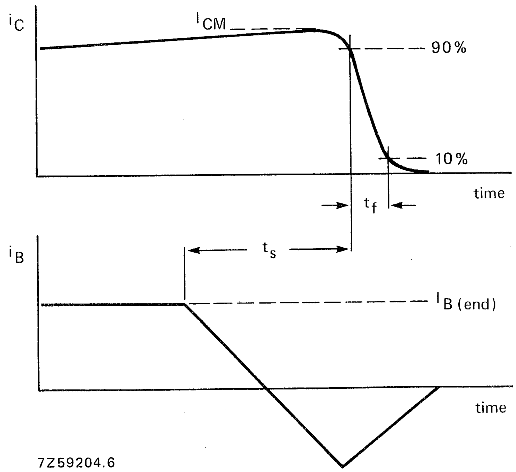


Fig. 4 Switching times waveforms.

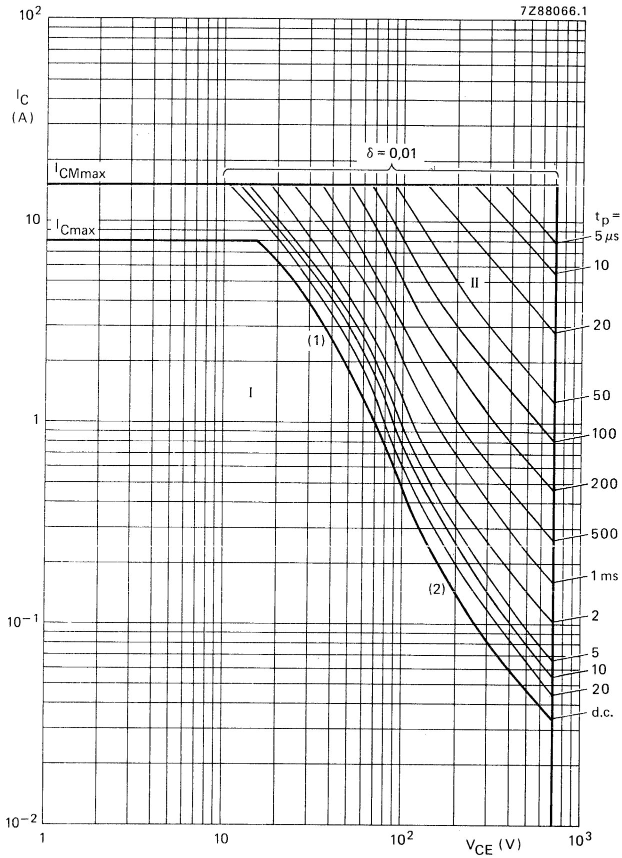


Fig. 5 Safe Operating Area; $T_{mb} \leqslant 25$ °C.

1. $P_{tot\ max}$ line.
2. Second-breakdown limits (independent of temperature)

I Region of permissible d.c.operation.

II Permissible extension for repetitive pulse operation.

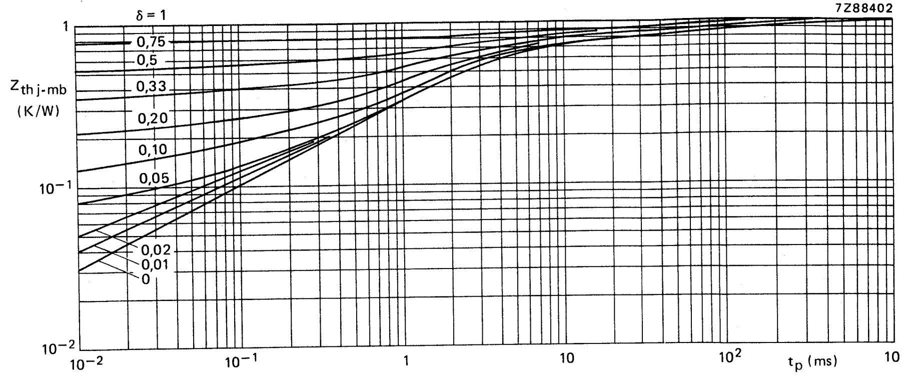


Fig. 6 Pulse power rating chart.

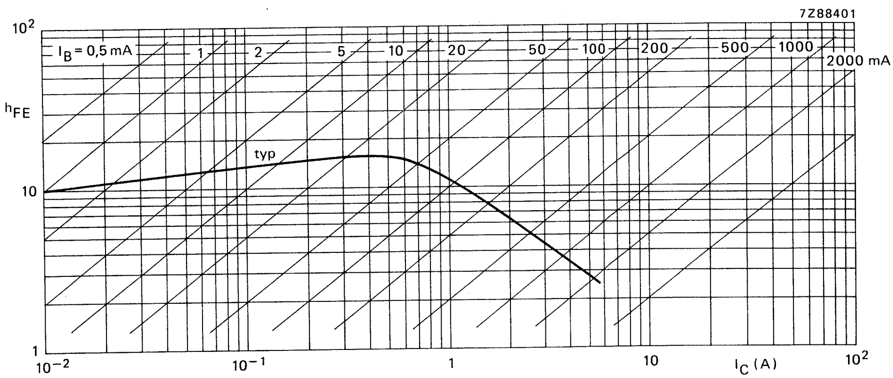


Fig. 7 Typical values d.c. current gain at V_{CE} = 5 V; T_{mb} = 25 °C.

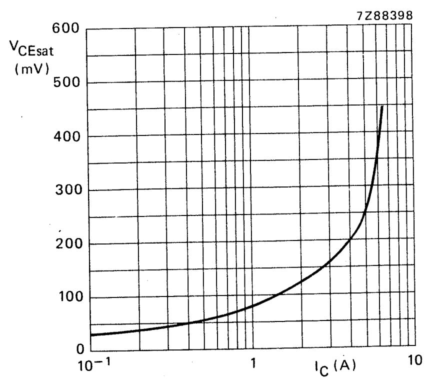


Fig. 8 Typical values I_C/I_B = 2; T_j = 25 °C.

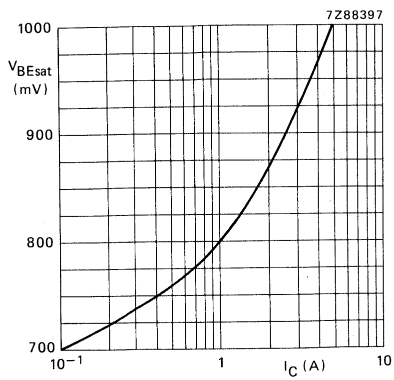


Fig. 9 Typical values I_C/I_B = 2; T_j = 25 °C.

APPLICATION INFORMATION - HORIZONTAL DEFLECTION CIRCUIT WITH BU508A

In designing horizontal deflection circuits, allowance has to be made for component and operating spreads in order not to exceed any Absolute Maximum Rating. Extensive analysis has shown that, for the peak collector current and the collector-emitter voltage of the output transistor, the total allowance need not be higher than 15%, and the following recommended base-drive and heatsink conditions are based on this figure.

To simplify the presentation, the design curves given refer to nominal conditions. Where the collector current will be modulated by the E-W correction circuit, the average value of the peak collector current applies provided the modulation is less than ± 10%.

To obtain a short fall time and minimum turn-off dissipation with a high-voltage transistor, the storage time must be sufficiently long and, during turn-off, the negative base-emitter voltage must be sufficiently high. Both requirements can easily be realized by including a small coil in series with the base of the output transistor. However, to reduce base current variations, a series base resistor is also added to most designs. This has the disadvantage of reducing the energy in the base inductance during turn-off, which in turn reduces the negative base-emitter voltage and with large resistor values may lead to an insufficient negative voltage for correct device turn-off. This can be improved by shunting the base resistor by a diode and/or a capacitor. Instead of giving various detailed base circuits based on these considerations, it is a more direct approach to specify the recommended $-dI_B/dt$, see Fig. 12.

The maximum transistor dissipation largely depends on the tolerances in the drive conditions. The dissipation given in Fig. 13 allows for base current and $-dI_B/dt$ tolerances of ± 15%.
The curve applies for a limit-case transistor at a mounting base temperature of 85 °C.

The thermal resistance for the heatsink can be calculated from $R_{th\ mb\text{-}a} = \dfrac{85 - T_{amb\ max}}{P_{tot\ max}}$ in which $T_{amb\ max}$ is the maximum ambient temperature of the transistor. In order to assure a value of thermal resistance at which thermal stability is ascertained, the minimum value for T_{amb} in the above equation is 45 °C.

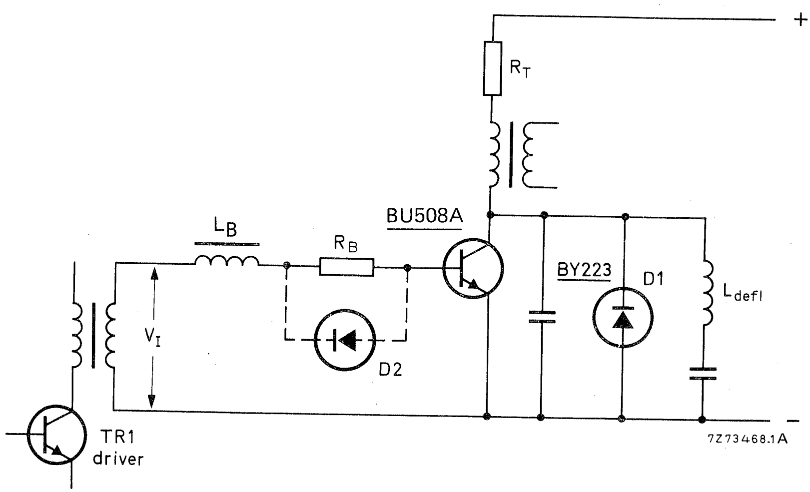


Fig. 10 Simplified horizontal deflection circuit.

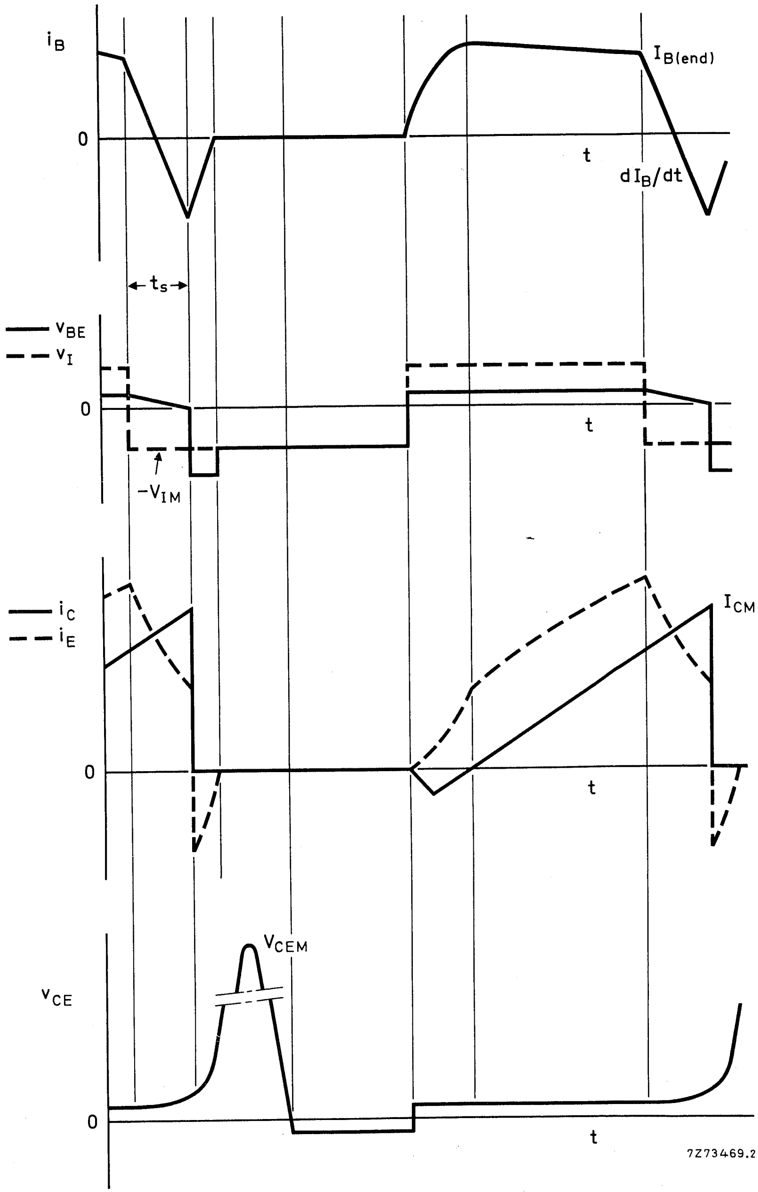


Fig. 11 Fundamental waveforms.

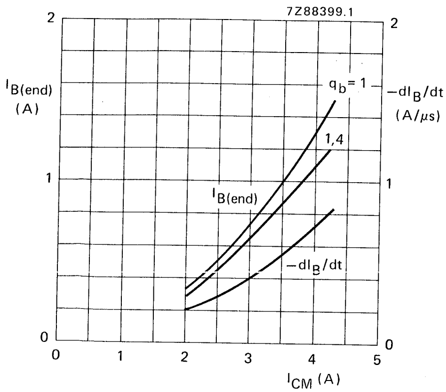


Fig. 12 Nominal end value of the base current and its rate of fall during turn-off as a function of nominal peak collector current.
A 15% spread allowance is included on these nominal values. Q_B is defined as $I_{B1}/I_{B(end)}$ (see Fig. 11). The reverse drive voltage during the storage and fall time ($-V_{IM}$) must be > 2 V).

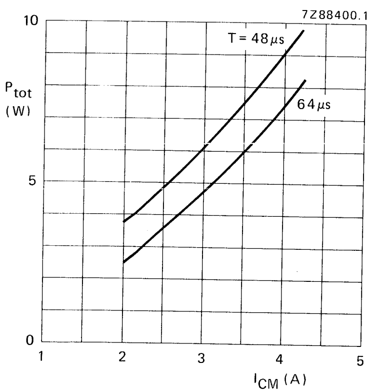


Fig. 13 Worst-case dissipation of BU508A under limited operational conditions according to Fig. 12. T_{mb} = 85 °C.

SILICON DIFFUSED POWER TRANSISTOR

High-voltage, high-speed switching, glass passivated n-p-n power transistor in a SOT-93A envelope, intended for use in horizontal deflection circuits of television receivers.

QUICK REFERENCE DATA

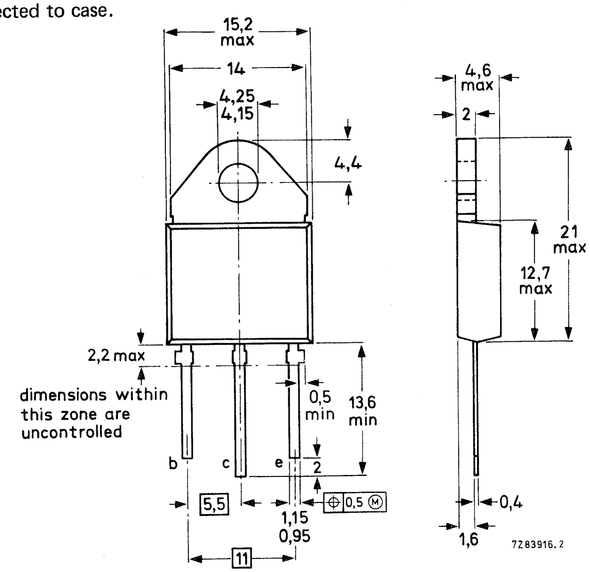
Collector-emitter voltage (V_{BE} = 0; peak value)	V_{CESM}	max.	1500	V
Collector-emitter voltage (open base)	V_{CEO}	max.	700	V
Collector current (d.c.)	I_C	max.	2,5	A
Collector current (peak value, t_p < 2 ms)	I_{CM}	max.	4	A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	75	W
Collector-emitter saturation voltage I_C = 2 A; I_B = 0,9 A	V_{CEsat}	<	5	V
Fall time I_{Con} = 2 A; $I_{B(end)}$ = 0,9 A	t_f	typ.	0,9	μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-93A.

Collector connected to case.



See also chapters Mounting instructions and Accessories.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).

Collector-emitter voltage (peak value; $V_{BE} = 0$)	V_{CESM}	max.	1500	V
Collector-emitter voltage (open base)	V_{CEO}	max.	700	V
Collector current (d.c.)	I_C	max.	2,5	A
Collector current (peak value; $t_p < 2$ ms)	I_{CM}	max.	4	A
Base current	I_B	max.	2	A
Base current (peak value; $t_p < 2$ ms)	I_{BM}	max.	4	A
Total power dissipation up to $T_{mb} = 25\ ^oC$	P_{tot}	max.	75	W
Storage temperature	T_{stg}	−65 to + 150		^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1,67	K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Collector cut-off current*				
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$	I_{CES}	<	0,15	mA
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$; $T_j = 125\ ^oC$	I_{CES}	<	1	mA
Emitter cut-off current				
$I_C = 0$; $V_{EB} = 5$ V	I_{EBO}	<	1	mA
Emitter-base voltage				
$I_C = 0$; $I_E = 10$ mA	V_{EBO}	>	6	V
Saturation voltage				
$I_C = 2$ A; $I_B = 0,9$ A	V_{CEsat}	<	5	V
	V_{BEsat}	<	1,3	V
Collector-emitter sustaining voltage				
$I_C = 100$ mA; $I_B = 0$; $L = 25$ mH	$V_{CEOsust}$	>	700	V
Collector saturation current				
$V_{CE} = 5$ V	I_{Csat}	=	2	A
D.C. current gain				
$I_C = 2$ A; $V_{CE} = 5$ V	h_{FE}	>	2,2	
Second breakdown current				
$V_{CE} = 120$ V; $t = 200\ \mu s$	$I_{(SB)}$	>	2,0	A
Transition frequency at f = 5 MHz				
$I_C = 0,1$ A; $V_{CE} = 5$ V	f_T	typ.	7	MHz
Collector capacitance at f = 1 MHz				
$I_E = I_e = 0$; $V_{CB} = 10$ V	C_c	typ.	65	pF

* Measured with a half-sinewave voltage (curve tracer).

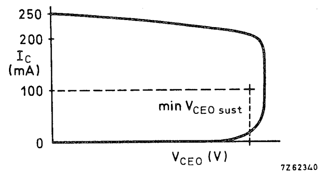


Fig. 2 Oscilloscope display for sustaining voltage.

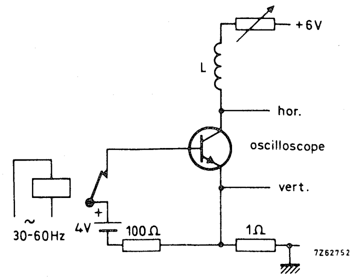


Fig. 3 Test circuit for sustaining voltage.

Switching times (in horizontal deflection circuit)
$-V_{IM} = 4$ V; $L_B = 15$ μH; $I_{CM} = 2$ A
$I_{B(end)} = 0,9$ A; $-dI_B/dt = 0,24$ A/μs

fall time	t_f	typ.	0,9 μs
storage time	t_s	typ.	7,5 μs

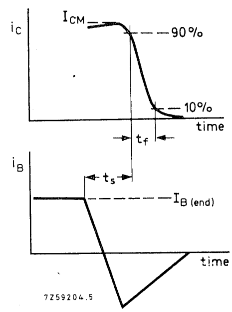


Fig. 4 Switching times waveform.

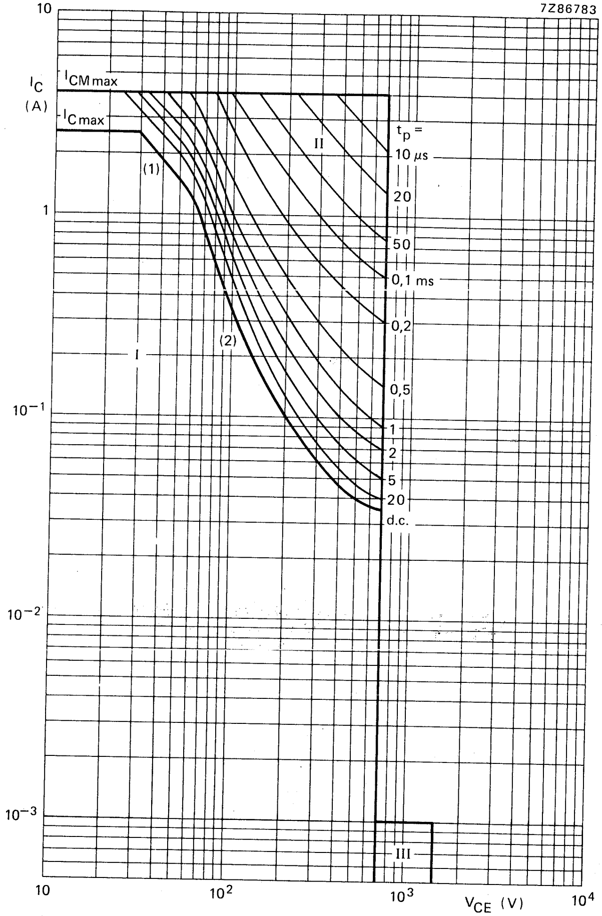


Fig. 5 Safe Operating ARea; T_{mb} = 25 °C.

(1) $P_{tot\,max}$ and $P_{peak\,max}$ lines.
(2) Second breakdown limits (independent of temperature).
I Region of permissible d.c. operation.
II Permissible extension for repetitive pulse operation.
III Repetitive pulse operation in this region is allowable, provided $R_{BE} < 100\ \Omega$, t_p = 20 μs, d = 0,25.

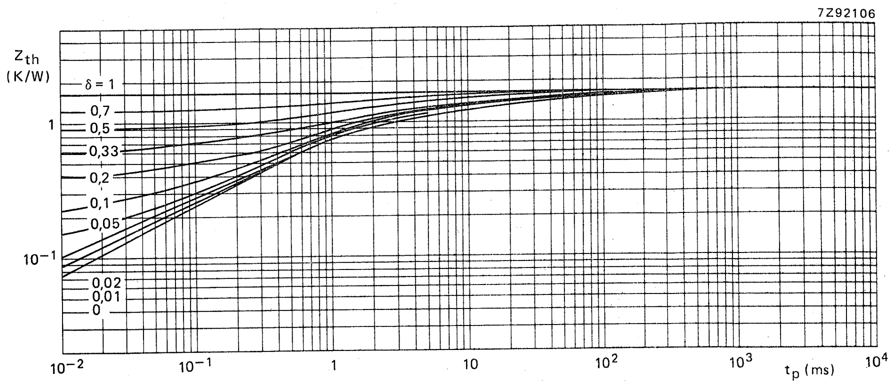


Fig. 6 Pulse power rating chart.
$R_{th\,j\text{-}mb} = 1{,}67$ K/W; $I_C = 1$ A; $V_{CE} = 25$ V; $d = \frac{t_p}{T}$.

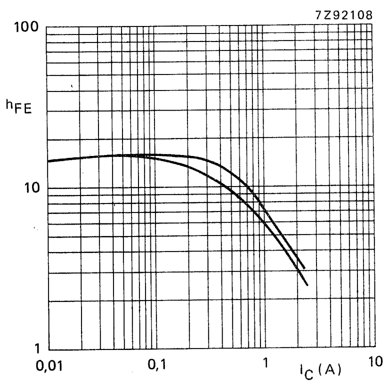


Fig. 7 Typical d.c. current gain.

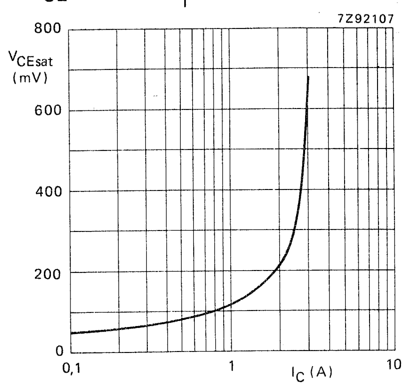


Fig. 8 Typical values V_{CEsat}
$I_C/I_B = 2$; $T_j = 25$ °C.

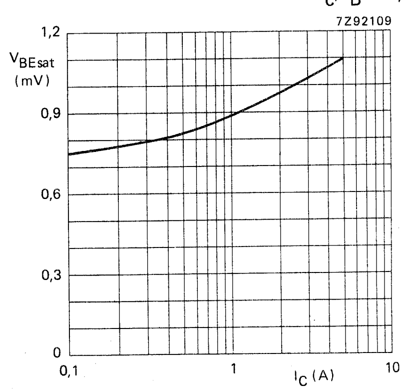


Fig. 9 Typical values V_{BEsat}; $I_C/I_B = 2$; $T_j = 25$ °C.

SILICON DARLINGTON POWER TRANSISTORS

High voltage n-p-n Darlington circuit with integrated speed-up diode in a plastic TO-220 envelope for industrial fast switching applications and horizontal deflection circuits of monitors and b/w television receivers.

QUICK REFERENCE DATA

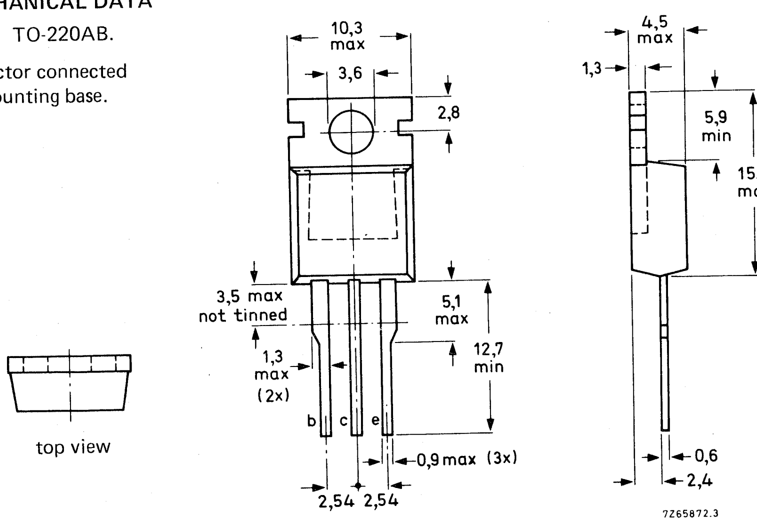
			BU806	BU807	
Collector-base voltage (open emitter)	V_{CBO}	max.	400	330	V
Collector-emitter voltage (V_{EB} = 6 V)	V_{CEX}	max.	400	330	V
Collector-emitter voltage (open base)	V_{CEO}	max.	200	150	V
Collector current (d.c.)	I_C	max.	8		A
Collector current (peak value) t_p = 0,3 ms; δ = 10%	I_{CM}	max.	15		A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	60		W
Junction temperature	T_j	max.	150		°C
Fall time I_{Con} = 5 A; I_{Bon} = 50 mA; $-I_{Boff}$ = 500 mA	t_f	typ.	0,2		μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Collector connected to mounting base.



See also chapters Mounting instructions and Accessories.

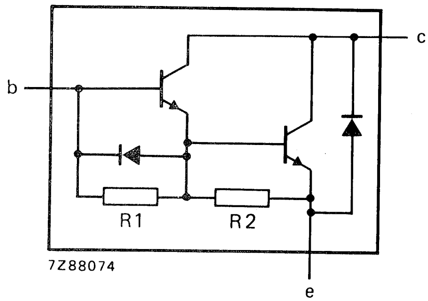


Fig. 2 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BU806	BU807	
Collector-base voltage (open emitter)	V_{CBO}	max.	400	330	V
Collector-emitter voltage (V_{EB} = 6 V)	V_{CEX}	max.	400	330	V
Collector-emitter voltage (open base)	V_{CEO}	max.	200	150	V
Emitter-base voltage (open collector)	V_{EBO}	max.	6		V
Collector current (d.c.)	I_C	max.	8		A
Collector current (peak value) t_p = 0,3 ms; δ = 0,1	I_{CM}	max.	15		A
Base current (d.c.)	I_B	max.	100		mA
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	60		W
Storage temperature	T_{stg}		−65 to +150		°C
Junction temperature*	T_j	max.	150		°C

THERMAL RESISTANCE*

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	2,08	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current** $V_{CE} = V_{CESmax}$; $V_{BE} = 0$	I_{CES}	<	100	μA
$V_{CE} = V_{CEXmax}$; V_{EB} = 6 V	I_{CEX}	<	100	μA
Emitter cut-off current $I_C = 0$; V_{EB} = 6 V	I_{EBO}	<	3	mA

			BU806	BU807	
Collector-emitter sustaining voltage I_C = 100 mA; I_{Boff} = 0; L = 25 mH	$V_{CEOsust}$	>	200	150	V

* Based on maximum average junction temperature in line with common industrial practice. The resulting higher junction temperature of the output transistor part is taken into account.

** Measured with a half sine wave voltage (curve tracer).

Saturation voltages

$I_C = 5$ A; $I_B = 50$ mA	V_{CEsat}	<	1,5 V
	V_{BEsat}	<	2,8 V
Diode, forward voltage $I_F = 4$ A	V_F	<	2 V

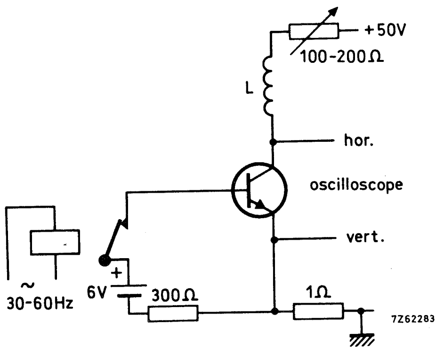


Fig. 3 Test circuit for $V_{CEOsust}$.

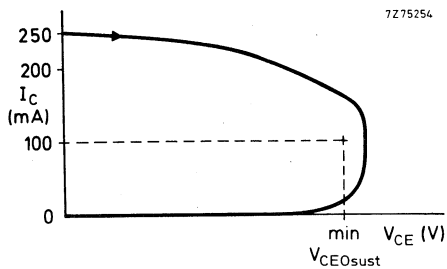


Fig. 4 Oscilloscope display for $V_{CEOsust}$.

Switching times (between 10% and 90% levels)

$I_{Con} = 5$ A; $V_{CC} = 100$ V

$I_{Bon} = 50$ mA; $-I_{Boff} = 500$ mA

Turn-on time	t_{on}	typ.	0,35 µs
Turn-off time: Storage time	t_s	typ.	0,55 µs
Fall time	t_f	typ.	0,2 µs

DEVELOPMENT SAMPLE DATA

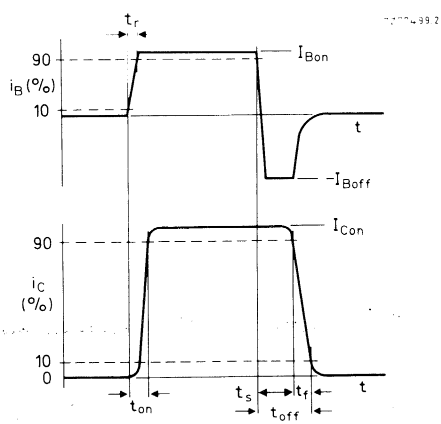


Fig. 5 Waveforms.

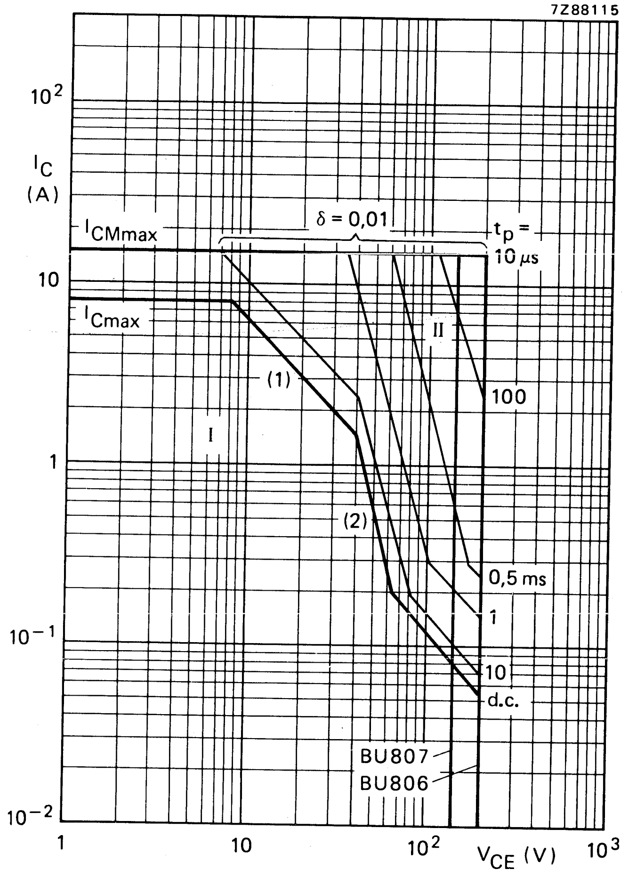


Fig. 6 D.C. Safe Operating ARea.

I Region of permissible d.c. operation.

II Permissible extension for repetitive pulse operation.

(1) $P_{tot\ max}$ and $P_{tot\ peak\ max}$ lines.

(2) Second breakdown limits (independent of temperature).

SILICON N-P-N DARLINGTON TRANSISTOR

Monolithic high voltage n-p-n Darlington transistor with integrated speed-up diode in a TO-202 envelope intended for fast switching applications such as small motor control and switch-mode power supplies.

QUICK REFERENCE DATA

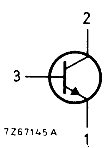
Collector-emitter voltage $V_{BE} = 0$; peak value	V_{CESM}	max.	650	V
Collector-emitter voltage (open base)	V_{CEO}	max.	375	V
Collector current (d.c.)	I_C	max.	0,5	A
Collector current (peak value)	I_{CM}	max.	1	A
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	2	W
up to $T_{mb} = 25\ ^oC$	P_{tot}	max.	12,5	W
Collector-emitter saturation voltage $I_C = 200$ mA; $I_B = 600\ \mu A$	V_{CEsat}	<	5	V
Collector saturation current	I_{Csat}		0,2	A

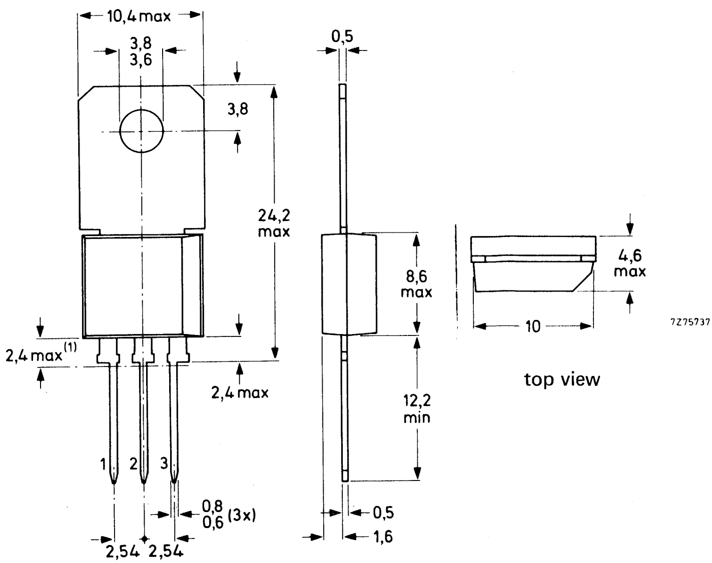
MECHANICAL DATA

Dimensions in mm

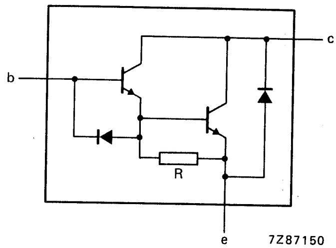
Fig. 1 TO-202.

Collector connected to mounting base.





See also chapters Mounting instructions and Accessories.



R typ. 600 Ω

Fig. 2 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage $V_{BE} = 0$; peak value	V_{CESM}	max.	650 V
Collector-emitter voltage (open base)	V_{CEO}	max.	375 V
Collector current (d.c.)	I_C	max.	0,5 A
Collector current (peak value)	I_{CM}	max.	1 A
Base current (d.c.)	I_B	max.	0,2 A
Base current	I_{BM}	max.	1 A
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	2 W
up to $T_{mb} = 25\ ^oC$	P_{tot}	max.	12,5 W
Storage temperature	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	10 K/W
From junction to ambient	$R_{th\ j\text{-}amb}$	=	62,5 K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Collector cut-off current* $V_{CE} = V_{CESMmax}$; $V_{BE} = 0$	I_{CES}	<	0,1 mA
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$; $T_j = 125\ ^oC$	I_{CES}	<	0,2 mA
Emitter cut-off current $I_C = 0$; $V_{EB} = 5$ V	I_{EBO}		3,3 to 20 mA
Collector-emitter sustaining voltage $I_B = 0$; $I_C = 250$ mA; L = 25 mH**	$V_{CEOsust}$	>	375 V
Saturation voltages $I_C = 200$ mA; $I_B = 600\ \mu A$	V_{CEsat}	<	5 V
	V_{BEsat}	<	2 V

* Measured with a half-sinewave voltage (curve tracer).
** Clamped at rated $V_{CEOsust}$.

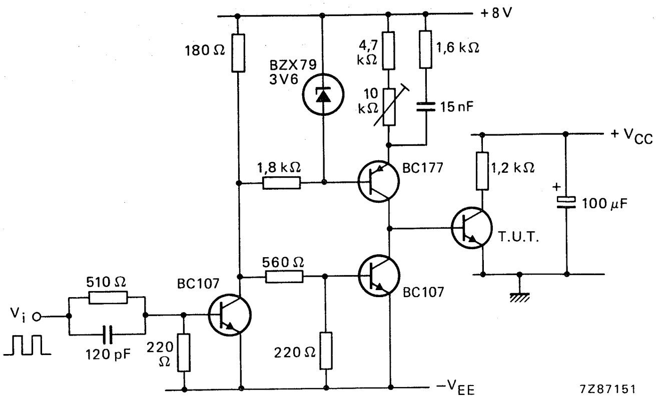


Fig. 3 Switching times test circuit.

DEVELOPMENT SAMPLE DATA

Switching times

I_{Con} = 200 mA; V_{CC} = 250 V; T_j = 100 °C;
I_{BM} = 5 mA; I_B = 0,9 mA; V_{EE} = 1 V

rise time	t_r	<	1	μs
storage time	t_s	<	1,5	μs
fall time	t_f	<	1	μs

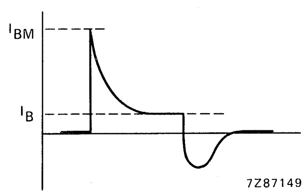


Fig. 4 Base current waveform.

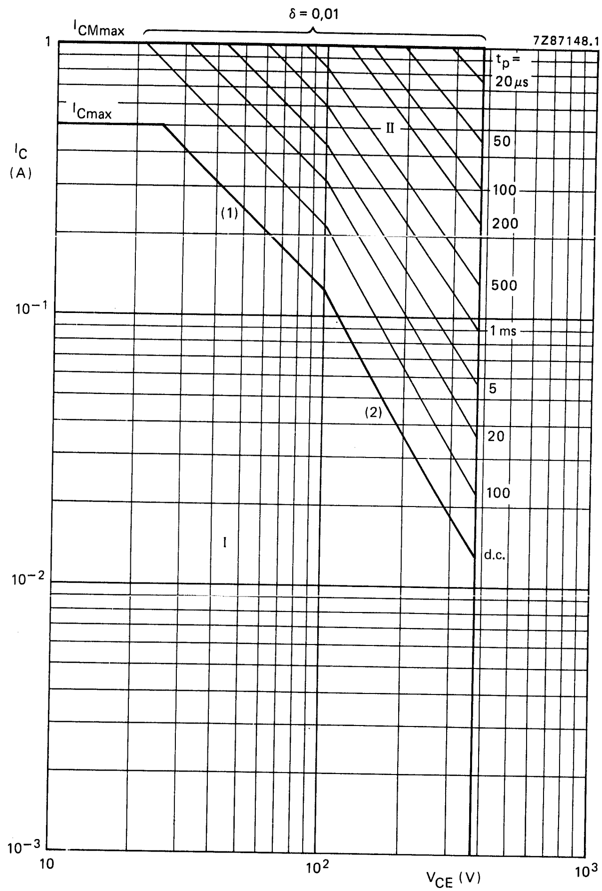


Fig. 5 Safe Operating ARea, $T_{mb} \leq 25\ ^oC$.

I Region of permissible d.c. operation.

II Permissible extension for repetitive pulse operation.

(1) $P_{tot\ max}$ and $P_{peak\ max}$ lines.

(2) Second-breakdown limits (independent of temperature).

SILICON DARLINGTON POWER TRANSISTOR

Monolithic high voltage n-p-n Darlington circuit with integrated speed-up diode in a plastic SOT-93 envelope, intended for fast switching application.

QUICK REFERENCE DATA

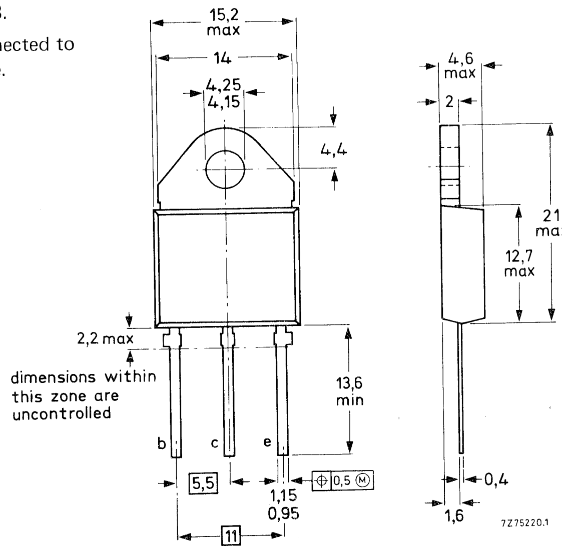
Collector-emitter voltage (V_{BE} = 0; peak value)	V_{CESM}	max.	800	V
Collector-emitter voltage (open base)	V_{CEO}	max.	375	V
Collector current (d.c.)	I_C	max.	6	A
Collector current (peak value) $t_p < 2$ ms	I_{CM}	max.	8	A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	125	W
Collector-emitter saturation voltage I_C = 2,5 A; I_B = 55 mA	V_{CEsat}	<	2,0	V
I_C = 4 A; I_B = 200 mA	V_{CEsat}	<	2,5	V
Collector saturation current	I_{Csat}	=	2,5	A
Fall time I_{Con} = 2,5A; I_{Bon} = 55 mA; $-I_{Boff}$ = 1 A	t_f	typ.	0,2	μs

MECHANICAL DATA

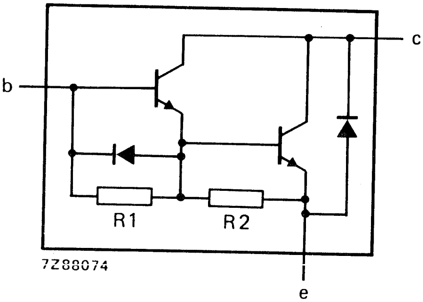
Dimensions in mm

Fig. 1 SOT-93.

Collector connected to mounting base.



See also chapters Mounting instructions and Accessories.



R1 typ. 200 Ω
R2 typ. 100 Ω

Fig. 2 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	800 V
Collector-emitter voltage (open base)	V_{CEO}	max.	375 V
Collector current (d.c.)	I_C	max.	6 A
Collector current (peak value) $t_p < 2$ ms	I_{CM}	max.	8 A
Base current (d.c.)	I_B	max.	2 A
Base current (peak value)	I_{BM}	max.	3 A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	125 W
Storage temperature	T_{stg}		−65 to + 150 °C
Junction temperature*	T_j	max.	150 °C

THERMAL RESISTANCE*

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1,0 K/W

* Based on maximum average junction temperature in line with common industrial practice. The resulting higher junction temperature of the output transistor part is taken into account.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current*			
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$	I_{CES}	<	1 mA
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$; T_j = 125 °C	I_{CES}	<	2 mA
Emitter cut-off current			
$I_C = 0$; V_{EB} = 8 V	I_{EBO}	<	150 mA
		>	50 mA
Collector-emitter sustaining voltage			
I_C = 100 mA; I_{Boff} = 0; L = 25 mH	$V_{CEOsust}$	>	375 V
Saturation voltages			
I_C = 2,5 A; I_B = 55 mA	V_{CEsat}	<	2,0 V
	V_{BEsat}	<	2,2 V
I_C = 4 A; I_B = 200 mA	V_{CEsat}	<	2,5 V
Collector saturation current			
V_{CEsat} < 2 V	I_{Csat}	=	2,5 A

DEVELOPMENT SAMPLE DATA

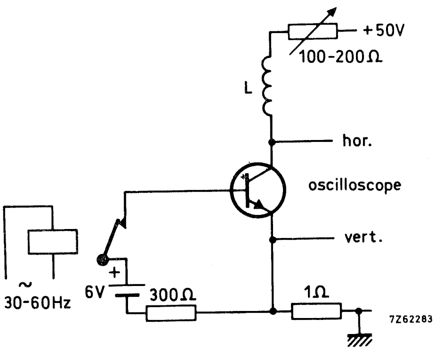


Fig. 3 Test circuit for $V_{CEOsust}$.

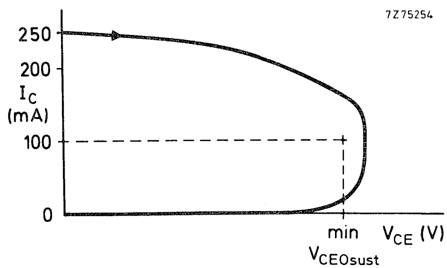


Fig. 4 Oscilloscope display for $V_{CEOsust}$.

* Measured with a half sine wave voltage (curve tracer).

CHARACTERISTICS (continued)

Switching times (between 10% and 90% levels)
I_{Con} = 2,5 A; V_{CC} = 250 V
I_{Bon} = 55 mA; $-I_{Boff}$ = 1 A

Turn-on time	t_{on}	<	1,3 µs
Turn-off time: Storage time	t_s	<	2,0 µs
Fall time	t_f	typ.	0,2 µs
Fall time; T_{mb} = 100 °C	t_f	<	0,6 µs

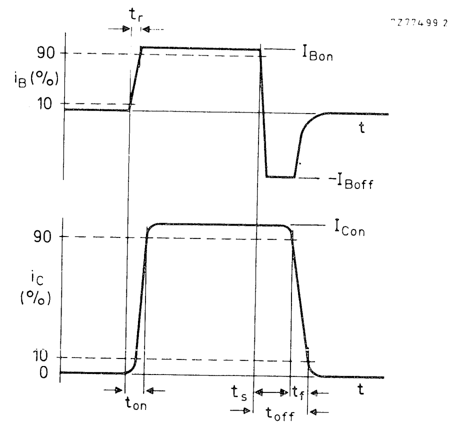


Fig. 5 Waveforms.

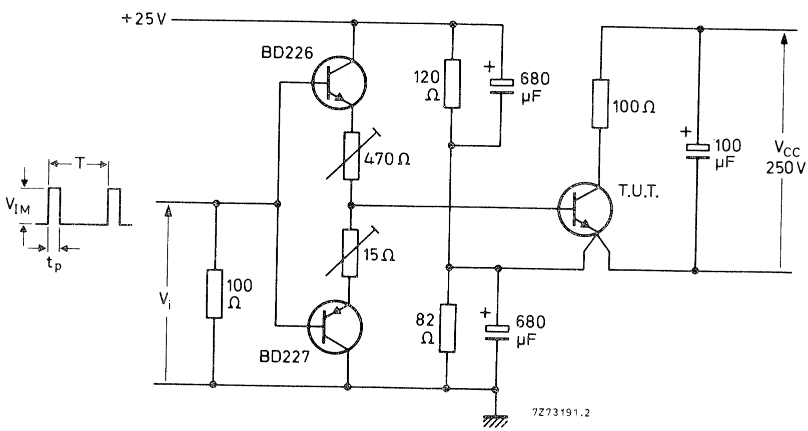


Fig. 6 Test circuit. T = 2 ms; t_p = 20 µs; V_{IM} = 15 V.

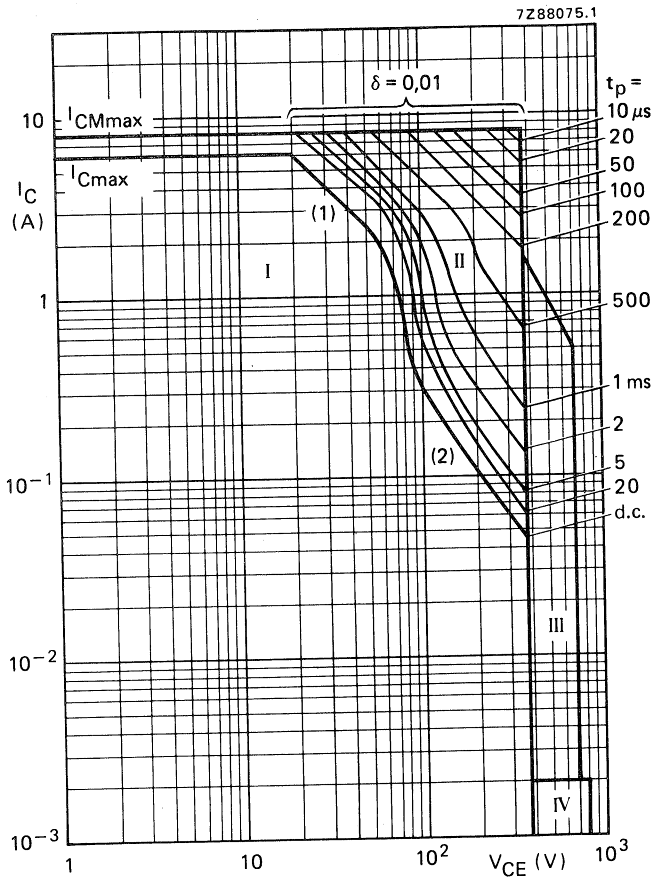


Fig. 7 Safe Operating ARea at T_{amb} = 25 °C.

I Region of permissible d.c. operation.

II Permissible extension for repetitive pulse operation.

III Area of permissible operation during turn-on in single-transistor converters, provided $t_p < 1{,}3\ \mu s$.

IV Repetitive pulse operation in this region is permissible, provided $V_{BE} \leqslant 0$ and $t_p \leqslant 2$ ms.

(1) $P_{tot\ max}$ and $P_{peak\ max}$ lines.
(2) Second-breakdown limits (independent of temperature).

DEVELOPMENT SAMPLE DATA

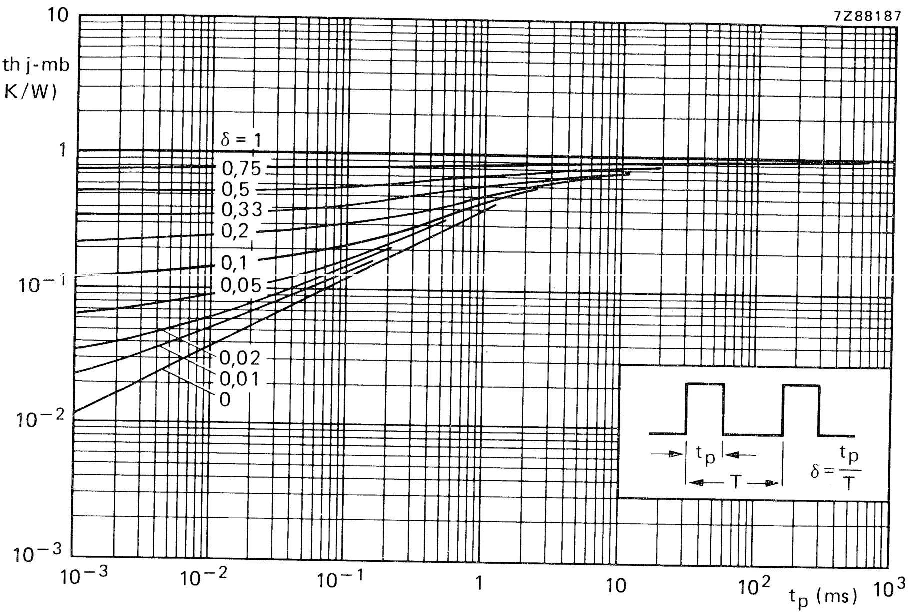


Fig. 8 Pulse power rating chart.

SILICON DIFFUSED POWER TRANSISTORS

High-voltage, high-speed, glass-passivated n-p-n power transistors in a TO-3 envelope, intended for use in converters, inverters, switching regulators, motor control systems etc.

QUICK REFERENCE DATA

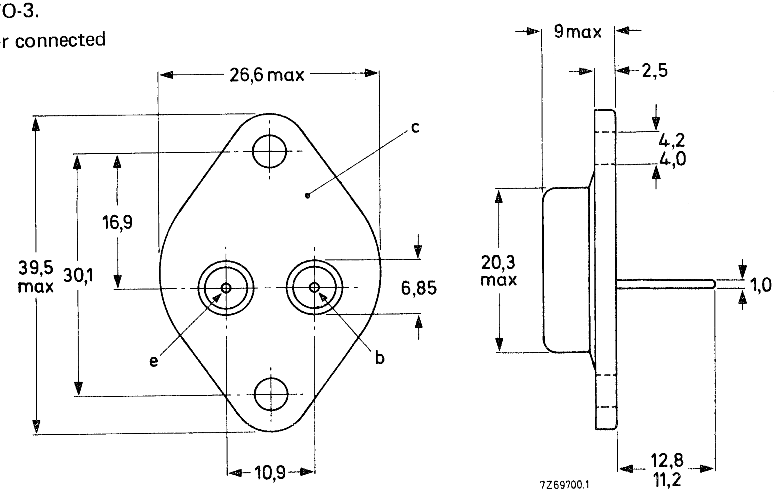
			BUS11	BUS11A	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	5		A
Collector current (peak value) $t_p \leq 2$ ms	I_{CM}	max.	10		A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	100		W
Collector-emitter saturation voltage					
I_C = 3 A; I_B = 0,6 A	V_{CEsat}	<	1,5	–	V
I_C = 2,5 A; I_B = 0,5 A	V_{CEsat}	<	–	1,5	V
Fall time (resistive load)					
I_{Con} = 3 A; I_{Bon} = $-I_{Boff}$ = 0,6 A	t_f	<	0,8	–	μs
I_{Con} = 2,5 A; I_{Bon} = $-I_{Boff}$ = 0,5 A	t_f	<	–	0,8	μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Collector connected to case.



Products approved to CECC 50 004-124 available on request.

See also chapters Mounting instructions and Accessories.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).

			BUS11	BUS11A	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	5		A
Collector current (peak value) $t_p < 2$ ms	I_{CM}	max.	10		A
Base current (d.c.)	I_B	max.	2		A
Base current (peak value); $t_p < 2$ ms	I_{BM}	max.	3		A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	100		W
Storage temperature	T_{stg}		−65 to +200		°C
Junction temperature	T_j	max.	200		°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1,75	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current *				
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$	I_{CES}	<	1	mA
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$; T_j = 125 °C	I_{CES}	<	2	mA
Emitter cut-off current				
$I_C = 0$; V_{EB} = 9 V	I_{EBO}	<	10	mA

			BUS11	BUS11A	
Saturation voltages					
I_C = 3 A; I_B = 0,6 A	V_{CEsat}	<	1,5	–	V
I_C = 2,5 A; I_B = 0,5 A	V_{CEsat}	<	–	1,5	V
I_C = 3 A; I_B = 0,6 A	V_{BEsat}	<	1,4	–	V
I_C = 2,5 A; I_B = 0,5 A	V_{BEsat}	<	–	1,4	V
Collector-emitter sustaining voltage					
I_C = 100 mA; I_{Boff} = 0; L = 25 mH	$V_{CEOsust}$	>	400	450	V
D.C. current gain					
I_C = 0,5 A; V_{CE} = 5 V	h_{FE}	typ.	30		

* Measured with a half sine-wave voltage (curve tracer).

CHARACTERISTICS (continued)

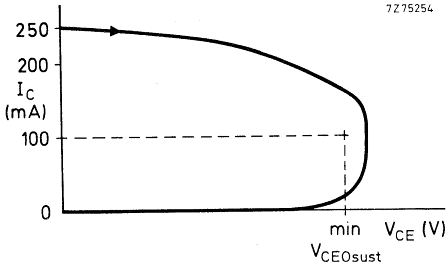


Fig. 2 Oscilloscope display for sustaining voltage.

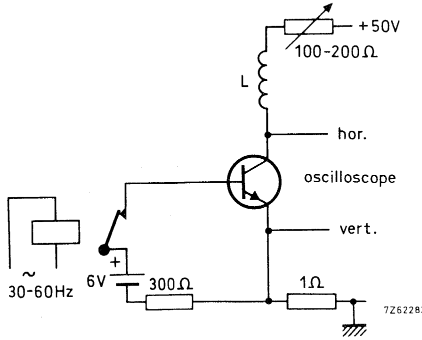
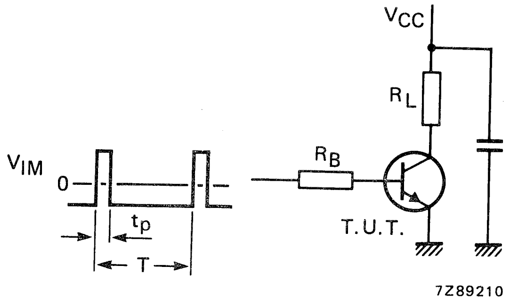


Fig. 3 Test circuit for $V_{CEOsust}$.

			BUS11	BUS11A	
Switching times resistive load (Figs 4 and 5)					
I_{Con} = 3 A; I_{Bon} = I_{Boff} = 0,6 A					
Turn-on time	t_{on}	<	1	–	μs
Turn-off: Storage time	t_s	<	4	–	μs
Fall time	t_f	<	0,8	–	μs
I_{Con} = 2,5 A; I_{Bon} = $-I_{Boff}$ = 0,5 A					
Turn-on time	t_{on}	<	–	1	μs
Turn-off: Storage time	t_s	<	–	4	μs
Fall time	t_f	<	–	0,8	μs
Switching times inductive load (Figs 6 and 7)					
I_{Con} = 3 A; I_B = 0,6 A					
Turn-off: Storage time	t_s	typ.	1,1	–	μs
		<	1,4	–	μs
Fall time	t_f	typ.	80	–	ns
		<	150	–	ns
I_{Con} = 3 A; I_B = 0,6 A; T_j = 100 °C					
Turn-off: Storage time	t_s	typ.	1,2	–	μs
		<	1,5	–	μs
Fall time	t_f	typ.	140	–	ns
		<	300	–	ns
Switching times inductive load (Figs 6 and 7)					
I_{Con} = 2,5 A; I_B = 0,5 A					
Turn-off: Storage time	t_s	typ.	–	1,1	μs
		<	–	1,4	μs
Fall time	t_f	typ.	–	80	ns
		<	–	150	ns
I_{Con} = 2,5 A; I_B = 0,5 A; T_j = 100 °C					
Turn-off: Storage time	t_s	typ.	–	1,2	μs
		<	–	1,5	μs
Fall time	t_f	typ.	–	140	ns
		<	–	300	ns



V_{CC} = 250 V
V_{IM} = −6 to + 8 V
$\frac{t_p}{T}$ = 0,01
t_p = 20 μs

Fig. 4 Test circuit resistive load.

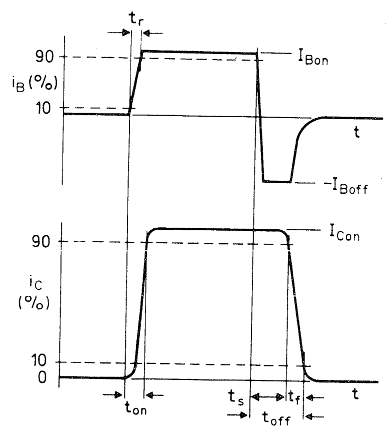


Fig. 5 Switching times waveforms with resistive load.

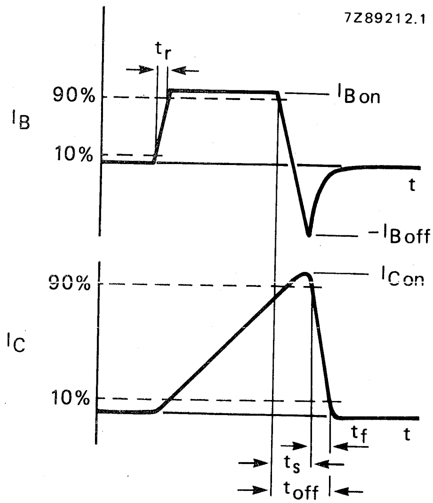
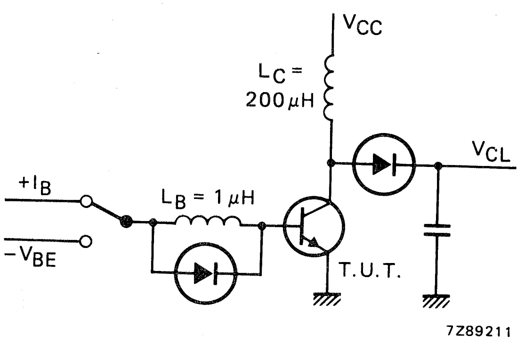
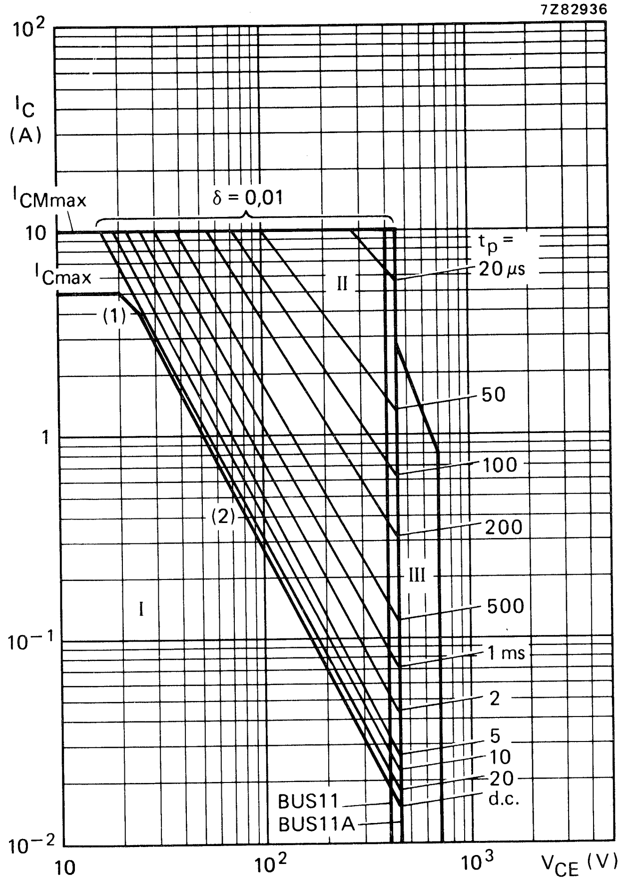


Fig. 6 Switching times waveforms with inductive load.



V_{CL} = 300 V
V_{CC} = 30 V
V_{EB} = 5 V

Fig. 7 Test circuit inductive load.



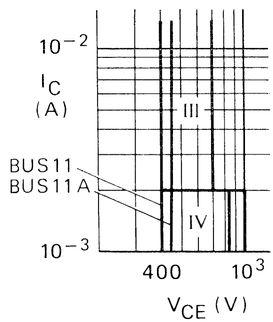


Fig. 8 Safe Operating ARea at $T_{mb} \leqslant 25\ ^{o}C$.

(1) $P_{tot\ max}$ and $P_{tot\ peak}$ max. lines.
(2) Second-breakdown limits (independent of temperature).

I Region of permissible d.c. operation
II Permissible extension for repetitive pulse operation
III Area of permissible operation during turn-on in single transistor converters, provided $R_{BE} \leqslant 100\ \Omega$ and $t_p \leqslant 0,6\ \mu s$.
IV Repetitive pulse operation in this region is permissible provided $V_{BE} \leqslant 0$ and $t_p \leqslant 2$ ms.

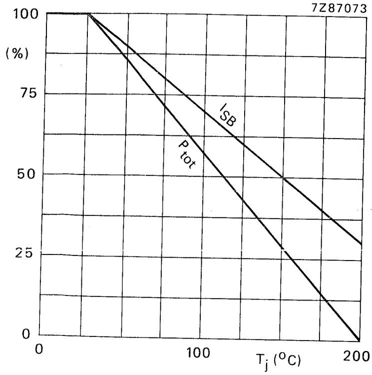


Fig. 9 Total power dissipation and second-breakdown current derating curve.

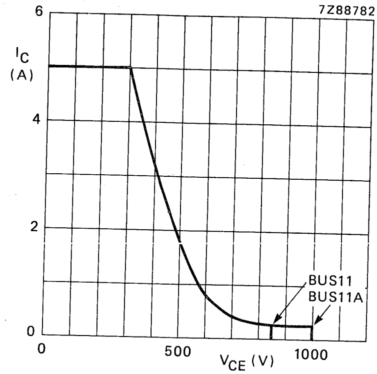


Fig. 10 Reverse bias SOAR.

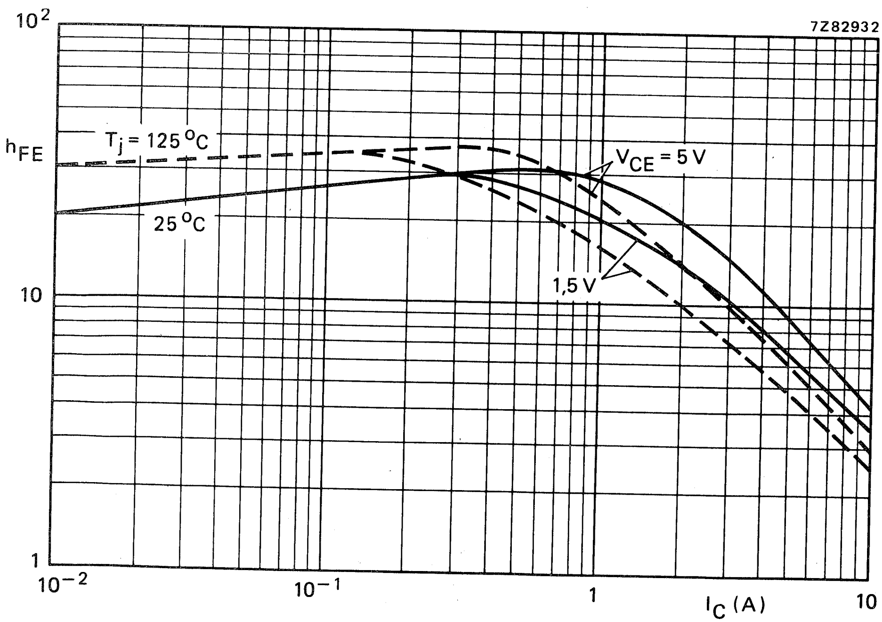


Fig. 11 D.C. current gain.

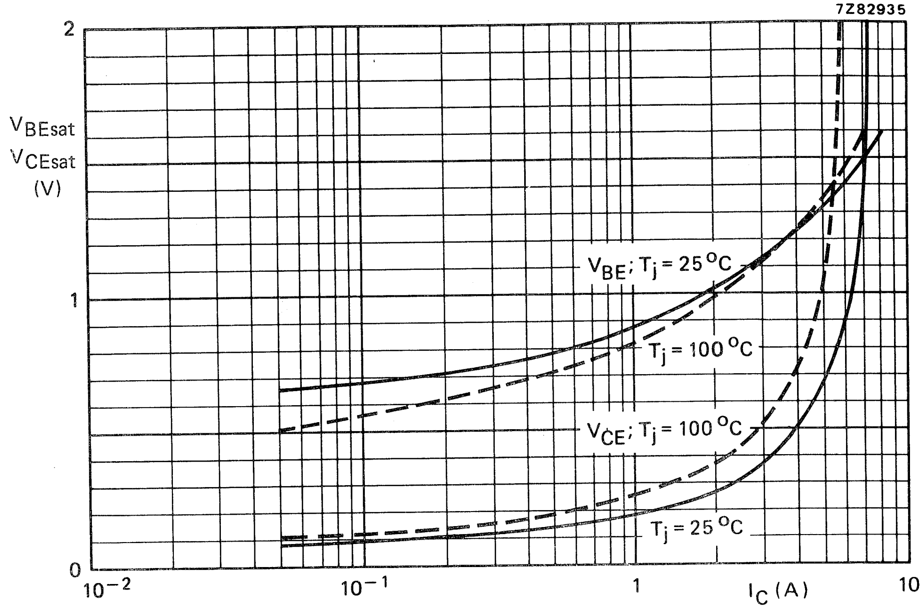


Fig. 12 Typical values base-emitter and collector-emitter voltage, $I_C/I_B = 5$.

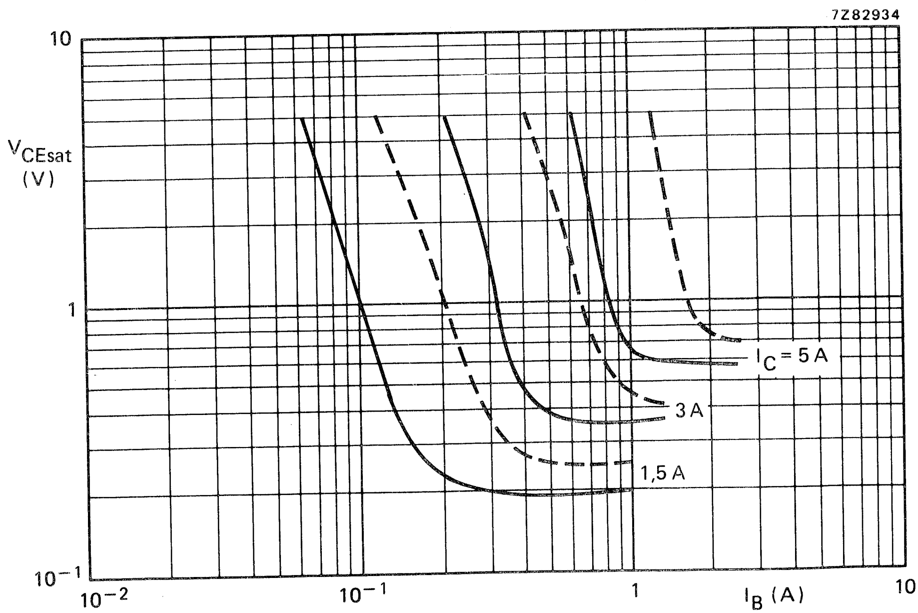


Fig. 13 Typ. (———) and max. (— — —) values collector-emitter saturation voltage at T_j = 25 °C.

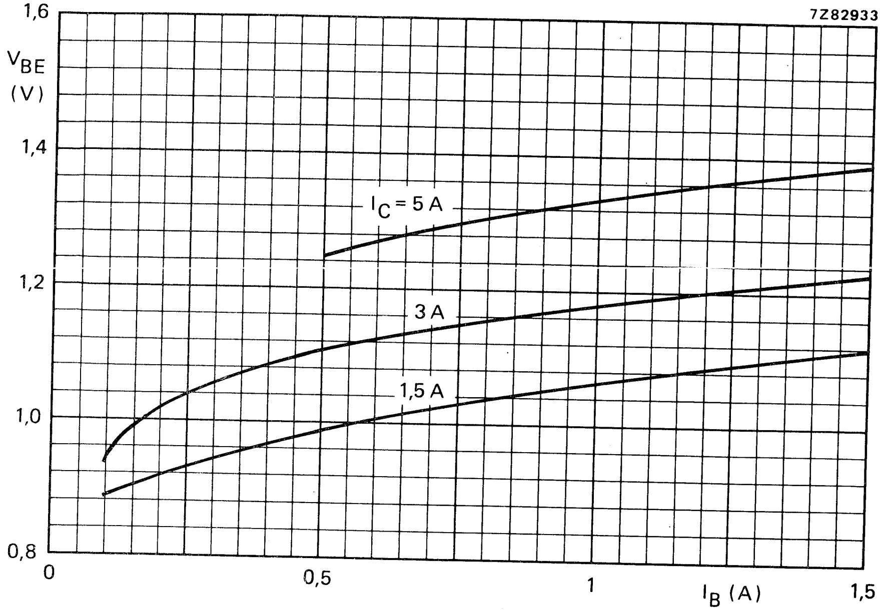


Fig. 14 Typical values at T_j = 25 °C.

APPLICATION INFORMATION

Important design factors of SMPS circuits are the maximum power losses, heatsink requirements and base drive conditions of the switching transistor. The power losses are very dependent on the operating frequency, the maximum collector current amplitude and shape.

The operating frequency is mostly set between 15 and 50 kHz. The collector current shape varies from rectangular in a forward converter to sawtooth in a flyback converter.

Information on nominal base drive, optimum base inductance and maximum transistor dissipation applied in a forward converter is given in Figs 15, 16 and 17. In these figures I_{CM} represents the maximum repetitive peak collector current, which occurs during overload. The information is derived from limit-case transistors at a mounting base temperature of 100 °C under the following conditions (see also Fig. 15):

- collector current shape $I_{C1}/I_{CM} = 0,9$
- duty factor $t_p/T = 0,45$
- rate of rise of I_C during turn-on = 4 A/μs
- rate of rise of V_{CE} during turn-off = 1 kV/μs
- reverse drive voltage during turn-off = 5 V
- base current shape $I_{B1}/I_{Be} = 1,5$

The required thermal resistance of the heatsink can be calculated from

$$R_{th\ mb\text{-}a} < \frac{100 - T_{amb}}{P_{tot}}\ \text{K/W}$$

To ensure thermal stability the value of the ambient temperature $T_{amb} > 40$ °C.

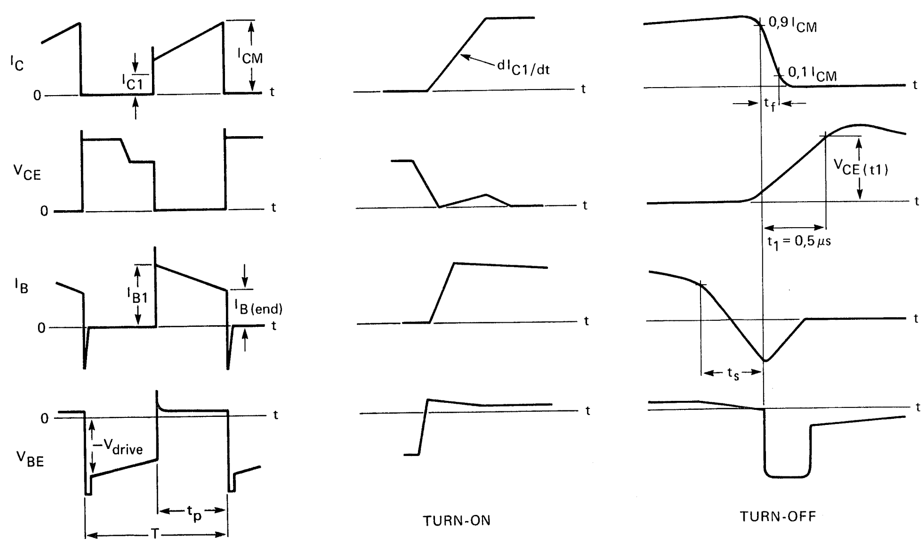


Fig. 15 Relevant waveforms of the switching transistor in a forward SMPS.

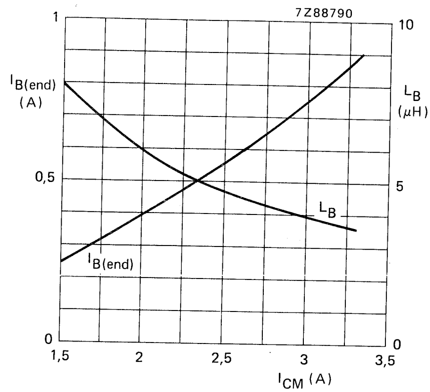


Fig. 16 Recommended nominal "end" value of the base current (I_{Be}) and optimum base inductance (L_B) at $-V_{drive}$ = 5 V versus maximum peak collector current. $dI_{B(end)}$ = ± 20%.

For other values of $-V_{drive}$ (3 V to 7 V) the related L_B is:

$$L_{Bnom} \frac{(-V_{drive}) + 1}{6}$$

L_{Bnom} is the value given in this graph.

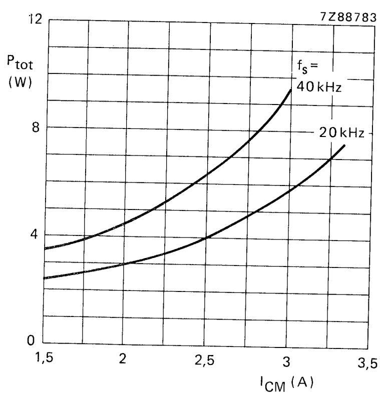


Fig. 17 Maximum transistor dissipation under worse-case operating condition versus maximum peak collector current. T_{mb} = 100 °C; $dI_{B(end)}$ = ± 20%.

SILICON DIFFUSED POWER TRANSISTORS

High-voltage, high-speed, glass-passivated n-p-n power transistors in a TO-3 envelope, intended for use in converters, inverters, switching regulators, motor control systems etc.

QUICK REFERENCE DATA

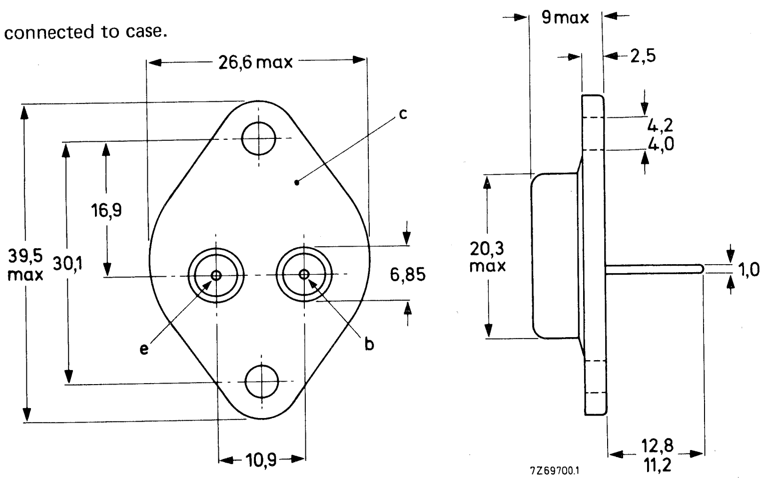
			BUS12	BUS12A	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	8	8	A
Collector current (peak value) $t_p \leq 2$ ms	I_{CM}	max.	20	20	A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	125	125	W
Collector-emitter saturation voltage					
I_C = 6 A; I_B = 1,2 A	V_{CEsat}	<	1,5	–	V
I_C = 5 A; I_B = 1 A	V_{CEsat}	<	–	1,5	V
Fall time (resistive load)					
I_{Con} = 6 A; I_{Bon} = $-I_{Boff}$ = 1,2 A	t_f	<	0,8	–	μs
I_{Con} = 5 A; I_{Bon} = $-I_{Boff}$ = 1 A	t_f	<	–	0,8	μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Collector connected to case.



See also chapters Mounting instructions and Accessories.

Products approved to CECC50 004-106 available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BUS12	BUS12A	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	8		A
Collector current (peak value); $t_p < 2$ ms	I_{CM}	max.	20		A
Base current (d.c.)	I_B	max.	4		A
Base current (peak value); $t_p \leqslant 2$ ms	I_{BM}	max.	6		A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	125		W
Storage temperature	T_{stg}		−65 to +200		°C
Junction temperature	T_j	max.	200		°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1,4	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current *				
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$	I_{CES}	<	1	mA
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$; T_j = 125 °C	I_{CES}	<	3	mA
Emitter cut-off current				
$I_C = 0$; $V_{EB} = 9$ V	I_{EBO}	<	10	mA

			BUS12	BUS12A	
Saturation voltages					
I_C = 6 A; I_B = 1,2 A	V_{CEsat}	<	1,5	–	V
I_C = 5 A; I_B = 1 A	V_{CEsat}	<	–	1,5	V
I_C = 6 A; I_B = 1,2 A	V_{BEsat}	<	1,5	–	V
I_C = 5 A; I_B = 1 A	V_{BEsat}	<	–	1,5	V
Collector-emitter sustaining voltage					
I_C = 100 mA; I_{Boff} = 0; L = 25 mH	$V_{CEOsust}$	>	400	450	V

* Measured with a half sine-wave voltage (curve tracer).

CHARACTERISTICS (continued)

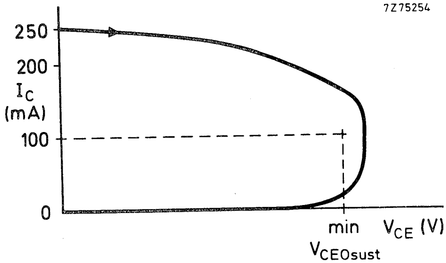


Fig. 2 Oscilloscope display for sustaining voltage.

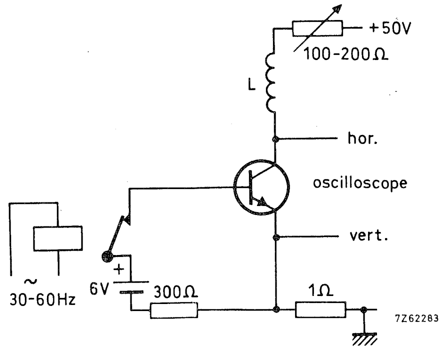


Fig. 3 Test circuit for $V_{CEOsust}$.

			BUS12	BUS12A	
Switching times resistive load (Figs 4 and 5)					
I_{Con} = 6 A; I_{Bon} = $-I_{Boff}$ = 1,2 A					
Turn-on time	t_{on}	<	1	–	μs
Turn-off: Storage time	t_s	<	4	–	μs
Fall time	t_f	<	0,8	–	μs
I_{Con} = 5 A; I_{Bon} = $-I_{Boff}$ = 1 A					
Turn-on time	t_{on}	<	–	1	μs
Turn-off: Storage time	t_s	<	–	4	μs
Fall time	t_f	<	–	0,8	μs
Switching times inductive load (Figs 6 and 7)					
I_{Con} = 6 A; I_B = 1,2 A					
Turn-off: Storage time	t_s	typ.	1,6	–	μs
		<	2,1	–	μs
Fall time	t_f	typ.	80	–	ns
		<	150	–	ns
I_{Con} = 6 A; I_B = 1,2 A; T_j = 100 °C					
Turn-off: Storage time	t_s	typ.	1,8	–	μs
		<	2,3	–	μs
Fall time	t_f	typ.	140	–	ns
		<	300	–	ns
Switching times inductive load (Figs 6 and 7)					
I_{Con} = 5 A; I_B = 1 A					
Turn-off: Storage time	t_s	typ.	–	1,6	μs
		<	–	2,1	μs
Fall time	t_f	typ.	–	80	ns
		<	–	150	ns
I_{Con} = 5 A; I_B = 1 A; T_j = 100 °C					
Turn-off: Storage time	t_s	typ.	–	1,8	μs
		<	–	2,3	μs
Fall time	t_f	typ.	–	140	ns
		<	–	300	ns

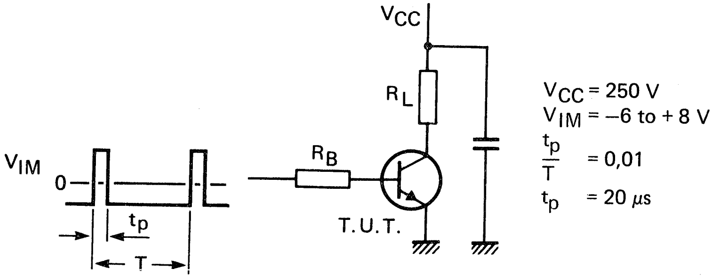


Fig. 4 Test circuit resistive load.

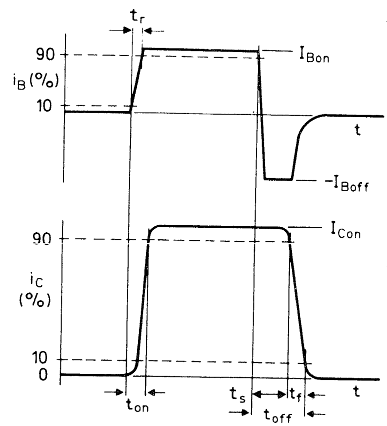


Fig. 5 Switching times waveforms with resistive load.

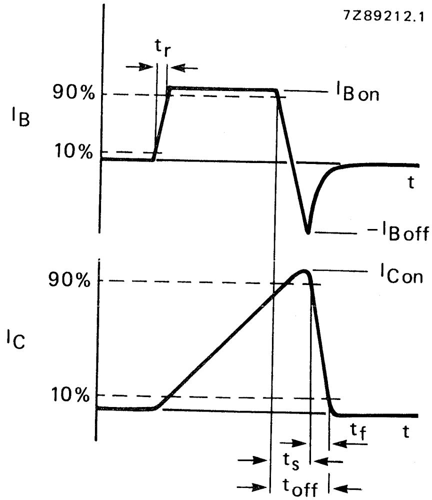


Fig. 6 Switching times waveforms with inductive load.

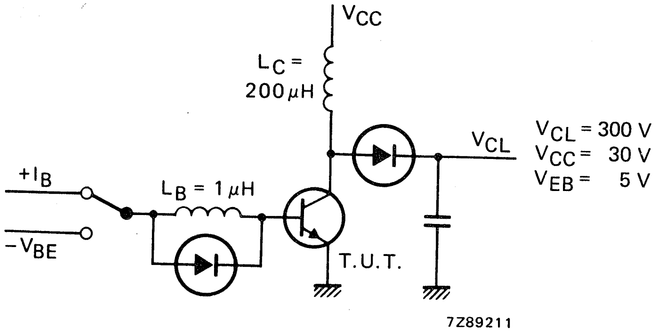


Fig. 7 Test circuit inductive load.

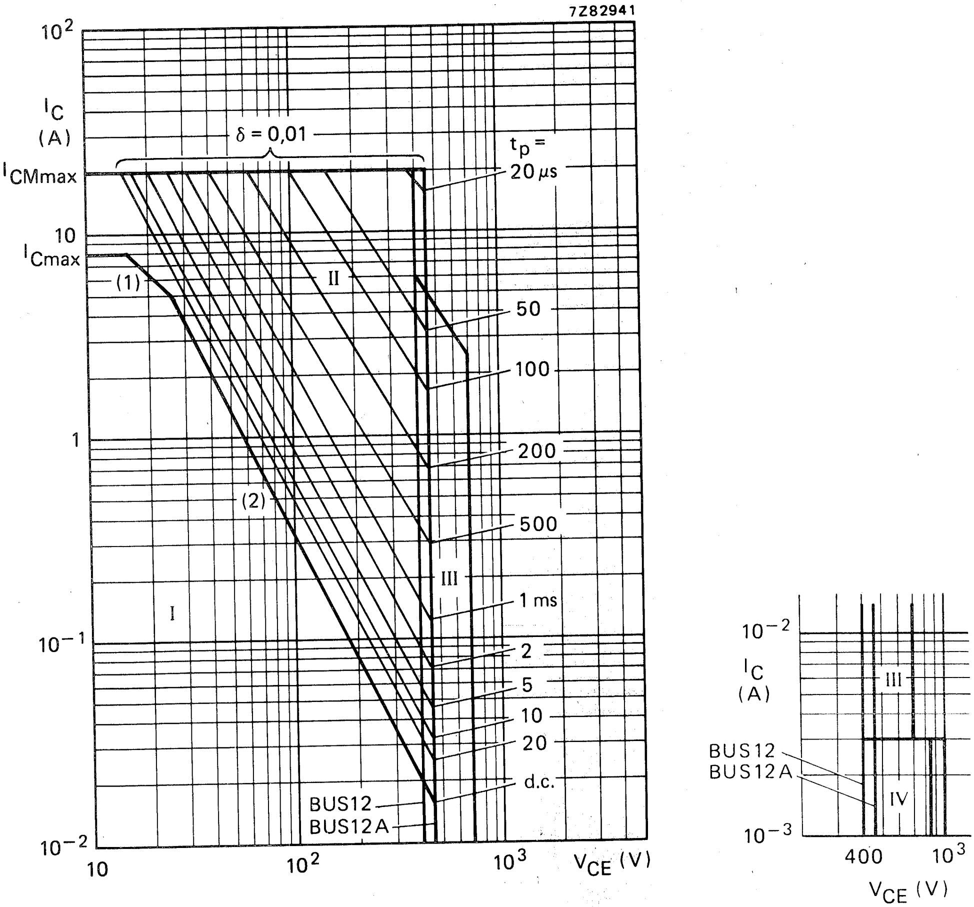


Fig. 8 Safe Operating ARea at $T_{mb} \leqslant 25$ °C.

(1) $P_{tot\ max}$ and $P_{tot\ peak\ max}$ lines.
(2) Second-breakdown limits (independent of temperature).

I Region of permissible d.c. operation.
II Permissible extension for repetitive pulse operation
III Area of permissible operation during turn-on in single transistor converters, provided $R_{BE} \leqslant 100\ \Omega$ and $t_p \leqslant 0{,}6\ \mu s$.
IV Repetitive pulse operation in this region is permissible provided $V_{BE} \leqslant 0$ and $t_p \leqslant 2$ ms.

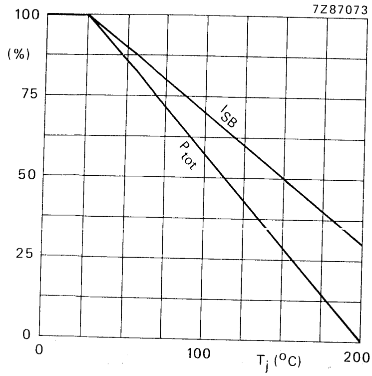


Fig. 9 Total power dissipation and second-breakdown current derating curve.

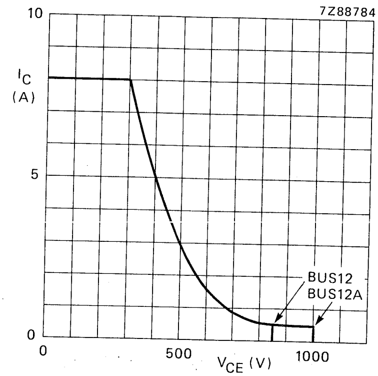


Fig. 10 Reverse bias SOAR.

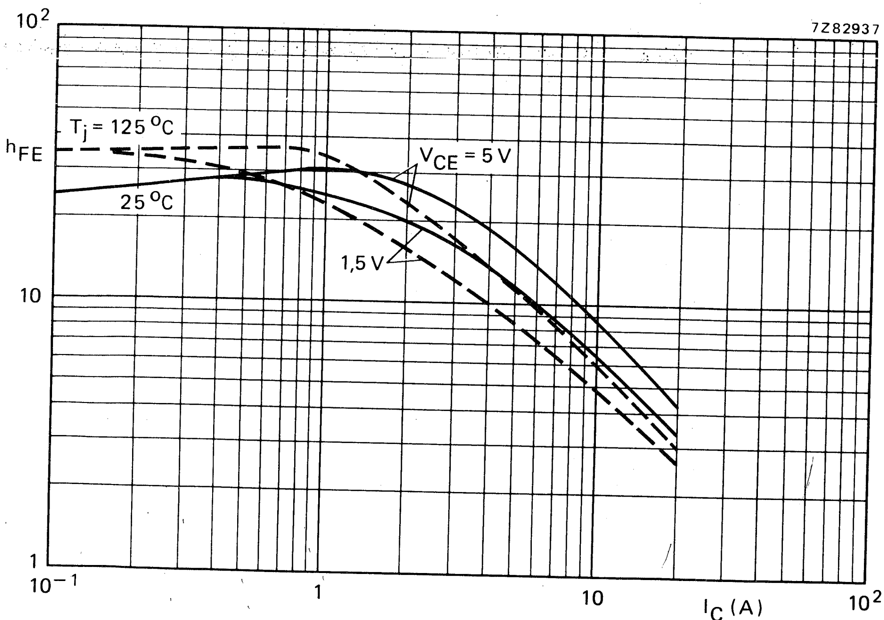


Fig. 11 Typical values d.c. current gain.

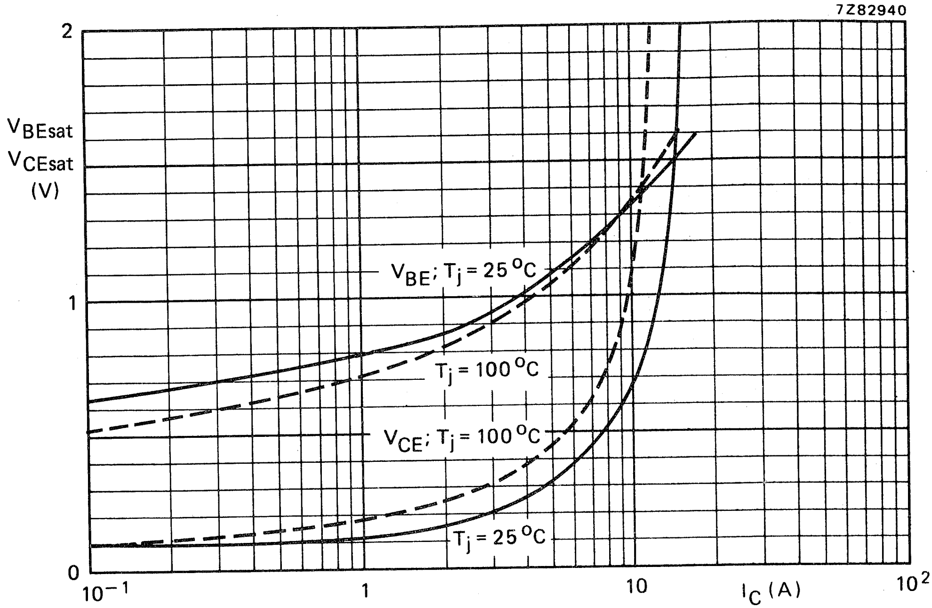


Fig. 12 Typical values base and collector voltage at $I_C/I_B = 5$.

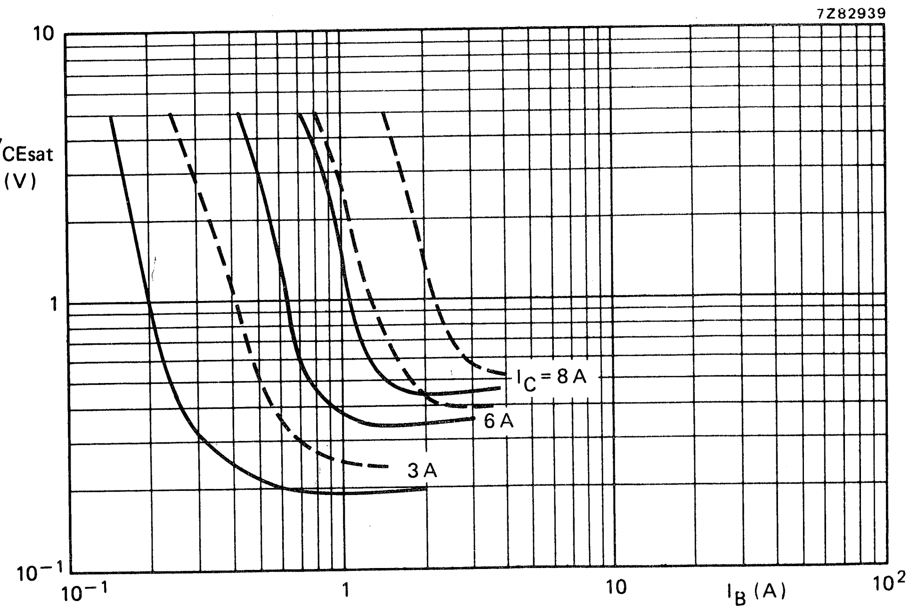


Fig. 13 Typ. (——) and max. (– – –) values collector-emitter saturation voltage at T_j = 25 °C.

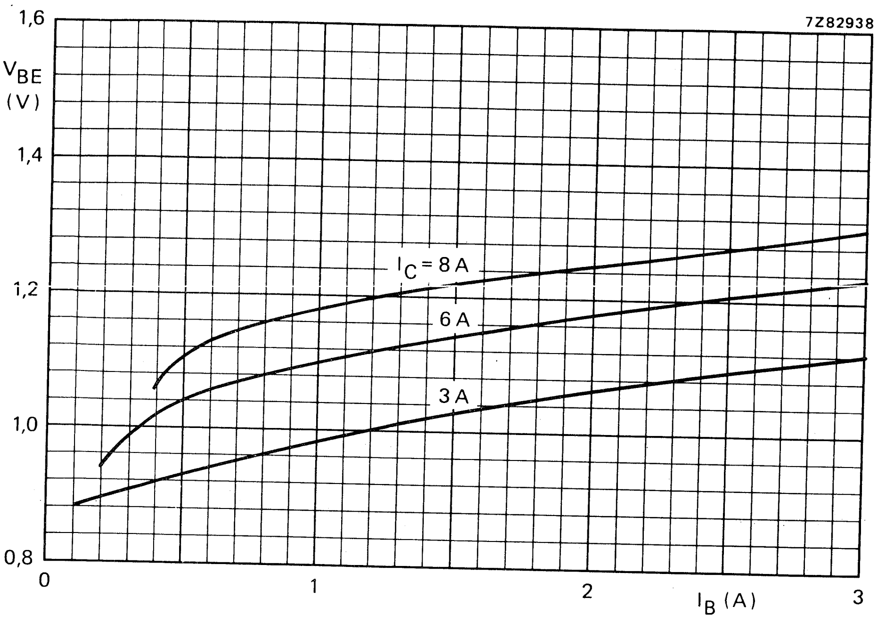


Fig. 14 Typical values base-emitter voltage at T_j = 25 °C.

APPLICATION INFORMATION

Important design factors of SMPS circuits are the maximum power losses, heatsink requirements and base drive conditions of the switching transistor. The power losses are very dependent on the operating frequency, the maximum collector current amplitude and shape.

The operating frequency is mostly set between 15 and 50 kHz. The collector current shape varies from rectangular in a forward converter to sawtooth in a flyback converter.

Information on nominal base drive, optimum base inductance and maximum transistor dissipation applied in a forward converter is given in Figs 15, 16 and 17. In these figures I_{CM} represents the maximum repetitive peak collector current, which occurs during overload. The information is derived from limit-case transistors at a mounting base temperature of 100 °C under the following conditions (see also Fig. 15):

- collector current shape $I_{C1}/I_{CM} = 0{,}9$
- duty factor $t_p/T = 0{,}45$
- rate of rise of I_C during turn-on = 8 A/μs
- rate of rise of V_{CE} during turn-off = 1 kV/μs
- reverse drive voltage during turn-off = 5 V
- base current shape $I_{B1}/I_{Be} = 1{,}5$

The required thermal resistance of the heatsink can be calculated from

$$R_{th\ mb\text{-}a} < \frac{100 - T_{amb}}{P_{tot}} \text{ K/W}$$

To ensure thermal stability the value of the ambient temperature $T_{amb} > 40$ °C.

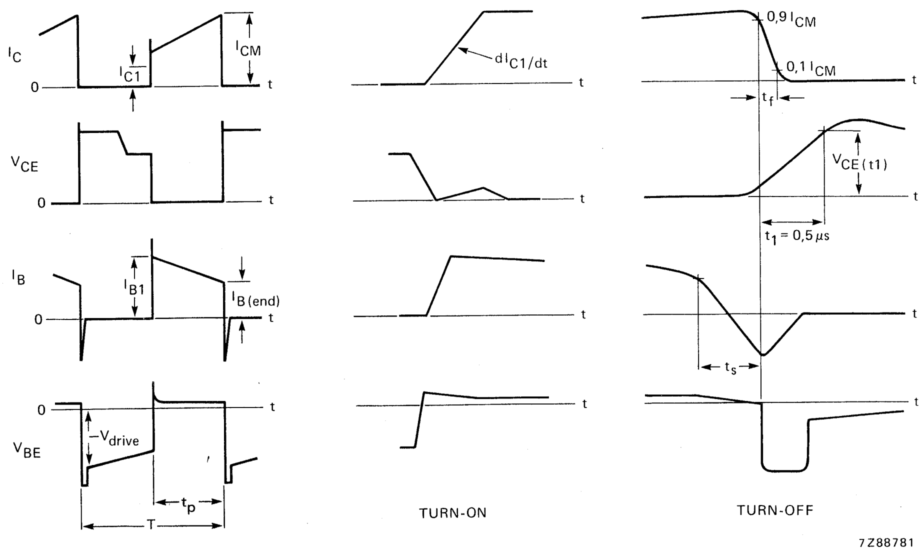


Fig. 15 Relevant waveforms of the switching transistor in a forward SMPS.

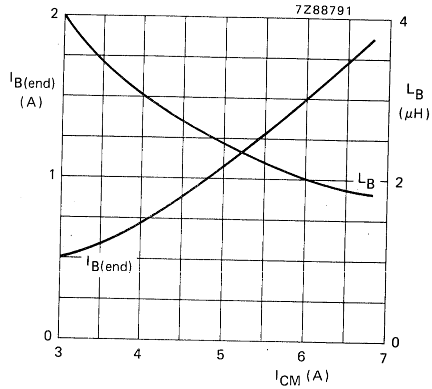


Fig. 16 Recommended nominal "end" value of the base current (I_{Be}) and optimum base inductance (L_B) at $-V_{drive}$ = 5 V versus maximum peak collector current. $dI_{B(end)}$ = ± 20%.

For other values of $-V_{drive}$ (3 V to 7 V) the related L_B is:

$$L_{Bnom} \frac{(-V_{drive}) + 1}{6}$$

L_{Bnom} is the value given in this graph.

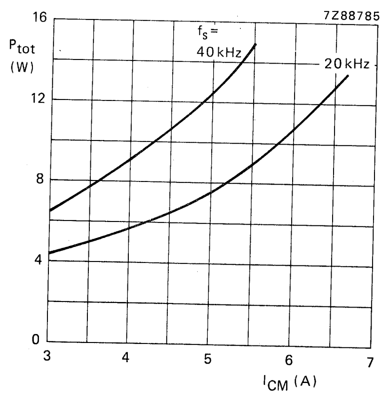


Fig. 17 Maximum transistor dissipation under worse-case operating condition versus maximum peak collector current. T_{mb} = 100 °C; $dI_{B(end)}$ = ± 20%.

SILICON DIFFUSED POWER TRANSISTORS

High-voltage, high-speed, glass-passivated n-p-n power transistors in a TO-3 envelope, intended for use in converters, inverters, switching regulators, motor control systems etc.

QUICK REFERENCE DATA

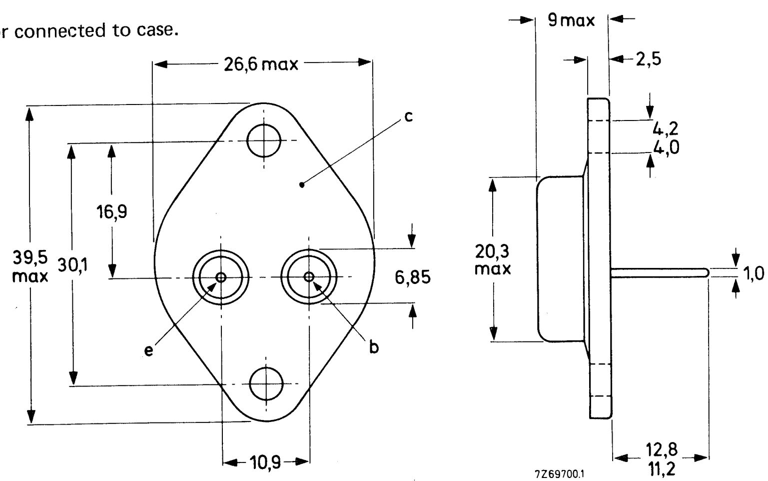
			BUS13	BUS13A	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	15	15	A
Collector current (peak value) t_p < 2 ms	I_{CM}	max.	30	30	A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	175	175	W
Collector-emitter saturation voltage					
I_C = 10 A; I_B = 2 A	V_{CEsat}	<	1,5	—	V
I_C = 8 A; I_B = 1,6 A	V_{CEsat}	<	—	1,5	V
Fall time (resistive load)					
I_{Con} = 10 A; I_{Bon} = $-I_{Boff}$ = 2 A	t_f	<	0,8	—	µs
I_{Con} = 8 A; I_{Bon} = $-I_{Boff}$ = 1,6 A	t_f	<	—	0,8	µs

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Collector connected to case.



Products approved to CECC 50 004—125 available on request.
See also chapters Mounting instructions and Accessories.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BUS13	BUS13A	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	15		A
Collector current (peak value); $t_p < 2$ ms	I_{CM}	max.	30		A
Base current (d.c.)	I_B	max.	6		A
Base current (peak value); $t_p < 2$ ms	I_{BM}	max.	9		A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	175		W
Storage temperature	T_{stg}		−65 to +200		°C
Junction temperature	T_j	max.	200		°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1,0	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current *				
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$	I_{CES}	<	1	mA
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$; T_j = 125 °C	I_{CES}	<	4	mA
Emitter cut-off current				
$I_C = 0$; V_{EB} = 9 V	I_{EBO}	<	10	mA

			BUS13	BUS13A	
Saturation voltages					
I_C = 10 A; I_B = 2 A	V_{CEsat}	<	1,5	–	V
I_C = 8 A; I_B = 1,6 A	V_{CEsat}	<	–	1,5	V
I_C = 10 A; I_B = 2 A	V_{BEsat}	<	1,6	–	V
I_C = 8 A; I_B = 1,6 A	V_{BEsat}	<	–	1,6	V
Collector-emitter sustaining voltage					
I_C = 100 mA; I_{Boff} = 0; L = 25 mH	$V_{CEOsust}$	>	400	450	V

* Measured with a half sine-wave voltage (curve tracer).

CHARACTERISTICS (continued)

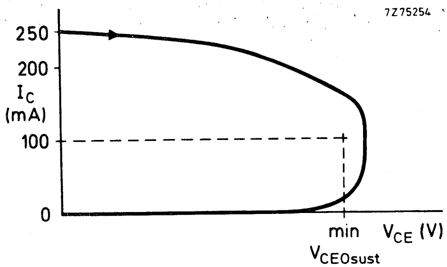


Fig. 2 Oscilloscope display for sustaining voltage.

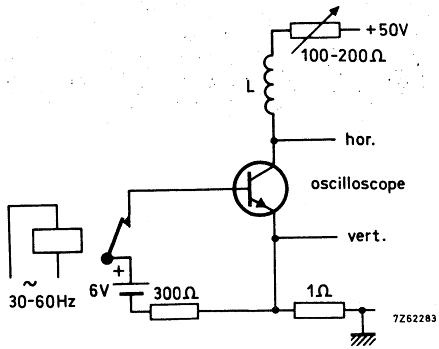


Fig. 3 Test circuit for $V_{CEOsust}$.

			BUS13	BUS13A	
Switching times resistive load (Figs 4 and 5)					
I_{Con} = 10 A; I_{Bon} = $-I_{Boff}$ = 2 A					
Turn-on time	t_{on}	<	1	–	µs
Turn-off: Storage time	t_s	<	4	–	µs
Fall time	t_f	<	0,8	–	µs
I_{Con} = 8 A; I_{Bon} = $-I_{Boff}$ = 1,6 A					
Turn-on time	t_{on}	<	–	1	µs
Turn-off: Storage time	t_s	<	–	4	µs
Fall time	t_f	<	–	0,8	µs
Switching times inductive load (Figs 6 and 7)					
I_{Con} = 10 A; I_B = 2 A					
Turn-off: Storage time	t_s	typ.	2,3	–	µs
		<	3,0	–	µs
Fall time	t_f	typ.	80	–	ns
		<	150	–	ns
I_{Con} = 10 A; I_B = 2 A; T_j = 100 °C					
Turn-off: Storage time	t_s	typ.	2,5	–	µs
		<	3,2	–	µs
Fall time	t_f	typ.	140	–	ns
		<	300	–	ns
Switching times inductive load (Figs 6 and 7)					
I_{Con} = 8 A; I_B = 1,6 A					
Turn-off: Storage time	t_s	typ.	–	2,3	µs
		<	–	3,0	µs
Fall time	t_f	typ.	–	80	ns
		<	–	150	ns
I_{Con} = 8 A; I_B = 1,6 A; T_j = 100 °C					
Turn-off: Storage time	t_s	typ.	–	2,5	µs
		<	–	3,2	µs
Fall time	t_f	typ.	–	140	ns
		<	–	300	ns

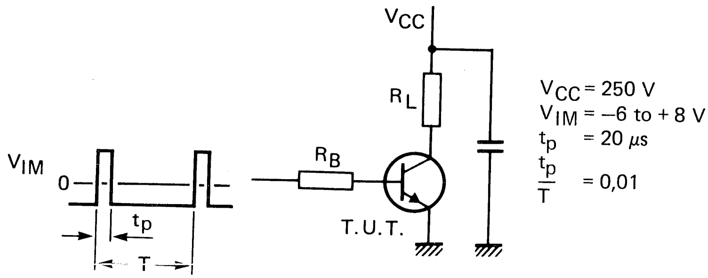


Fig. 4 Test circuit resistive load.

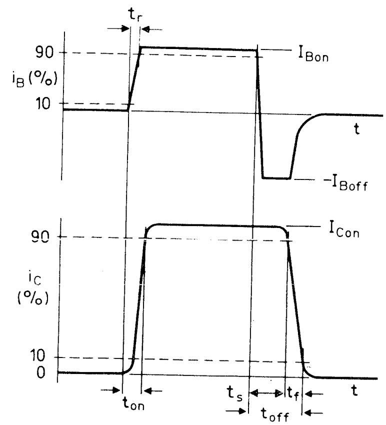


Fig. 5 Switching times waveforms with resistive load.

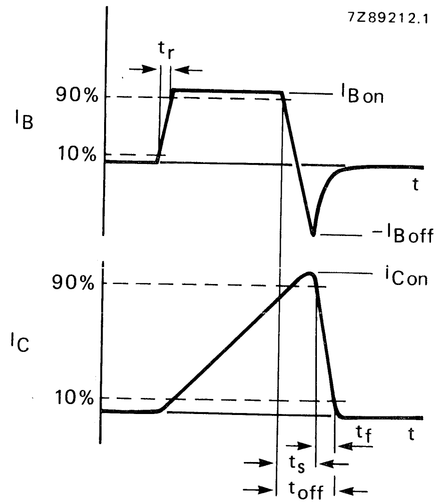


Fig. 6 Switching times waveforms with inductive load.

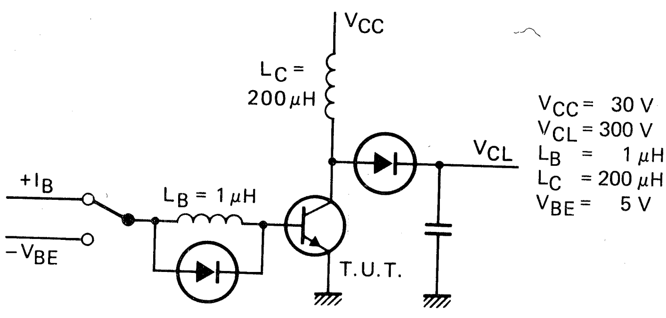
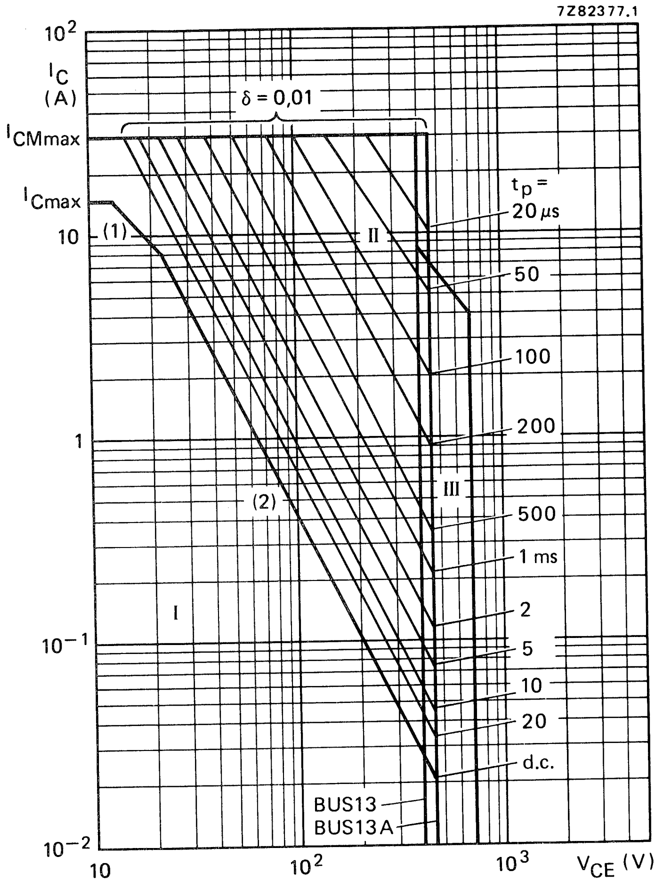


Fig. 7 Test circuit inductive load.



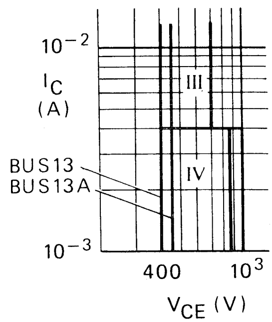


Fig. 8 Safe Operating ARea at $T_{mb} \leqslant 25\ ^{o}C$.

(1) $P_{tot\ max}$ and $P_{tot\ peak\ max}$ lines.
(2) Second-breakdown limits (independent of temperature).

I Region of permissible d.c. operation
II Permissible extension for repetitive pulse operation
III Area of permissible operation during turn-on in single transistor converters, provided $R_{BE} \leqslant 100\ \Omega$ and $t_p \leqslant 0,6\ \mu s$.
IV Repetitive pulse operation in this region is permissible provided $V_{BE} \leqslant 0$ and $t_p \leqslant 2$ ms.

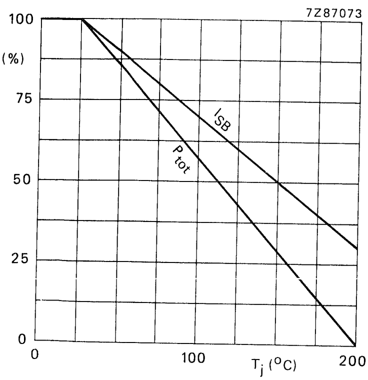


Fig. 9 Total power dissipation and second-breakdown current derating curve.

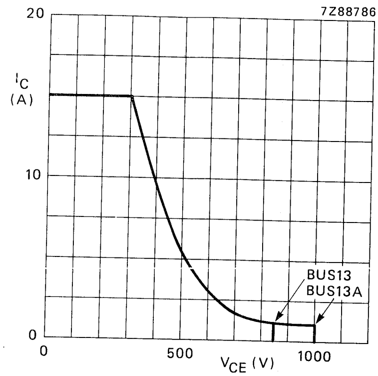


Fig. 10 Reverse bias SOAR.

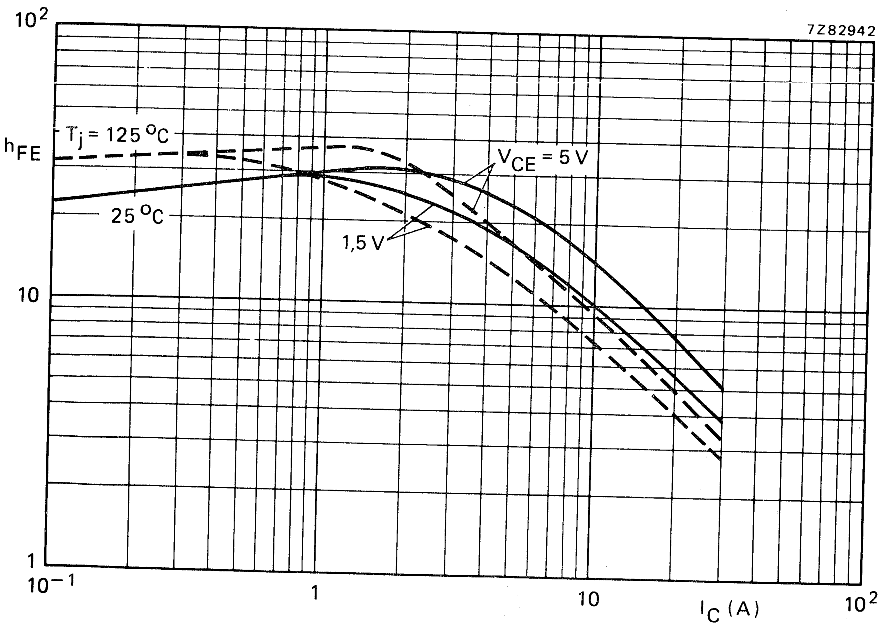


Fig. 11 Typical values d.c. current gain.

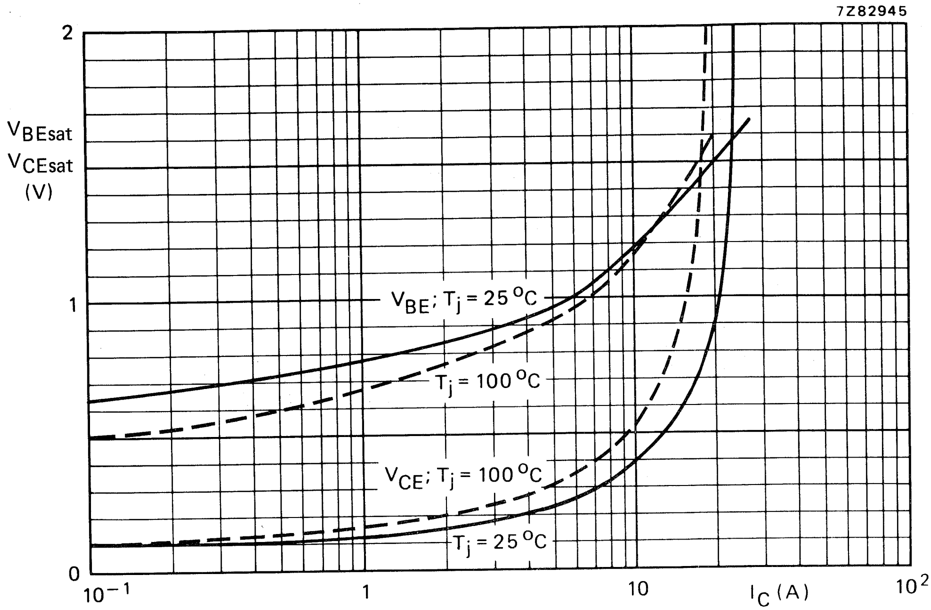


Fig. 12 Typical values base and collector voltage at $I_C/I_B = 5$.

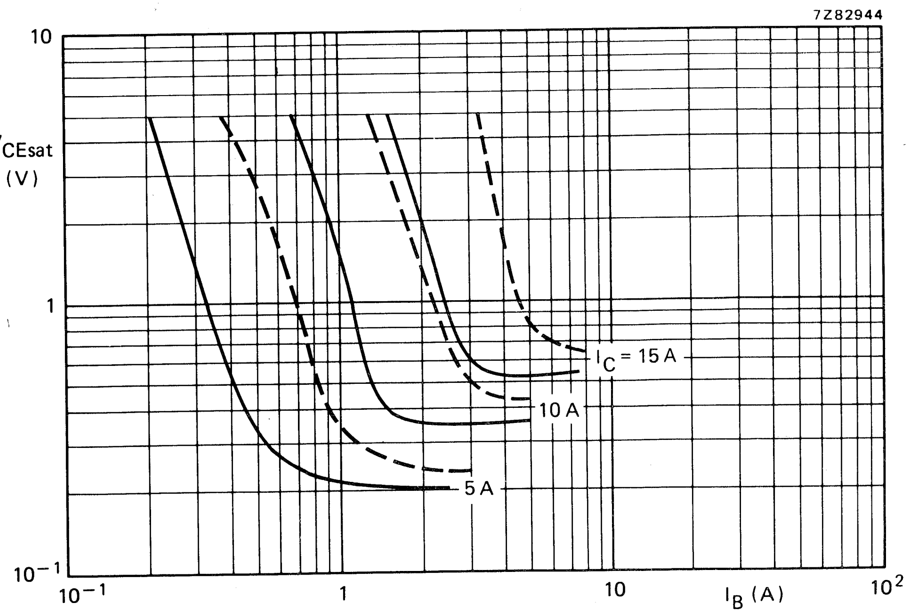


Fig. 13 Typical (——) and maximum (– – –) values saturation voltage. T_j = 25 °C.

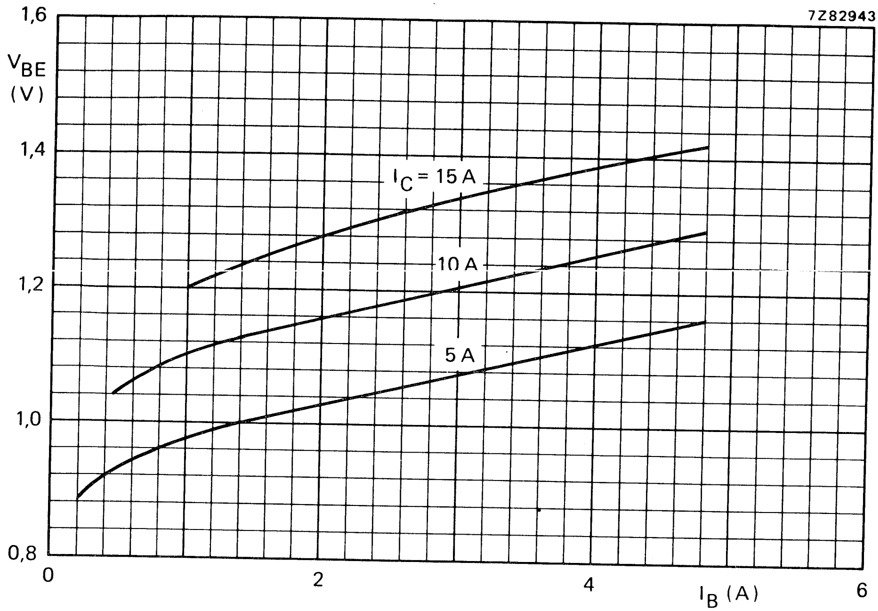


Fig. 14 Typical values base-emitter voltage at T_j = 25 °C.

APPLICATION INFORMATION

Important design factors of SMPS circuits are the maximum power losses, heatsink requirements and base drive conditions of the switching transistor. The power losses are very dependent on the operating frequency, the maximum collector current amplitude and shape.

The operating frequency is mostly set between 15 and 50 kHz. The collector current shape varies from rectangular in a forward converter to sawtooth in a flyback converter.

Information on nominal base drive, optimum base inductance and maximum transistor dissipation applied in a forward converter is given in Figs 15, 16 and 17. In these figures I_{CM} represents the maximum repetitive peak collector current, which occurs during overload. The information is derived from limit-case transistors at a mounting base temperature of 100 °C under the following conditions (see also Fig. 15):

- collector current shape $I_{C1}/I_{CM} = 0,9$
- duty factor $t_p/T = 0,45$
- rate of rise of I_C during turn-on = 10 A/µs
- rate of rise of V_{CE} during turn-off = 1 kV/µs
- reverse drive voltage during turn-off = 5 V
- base current shape $I_{B1}/I_{Be} = 1,5$

The required thermal resistance of the heatsink can be calculated from

$$R_{th\ mb\text{-}a} < \frac{100 - T_{amb}}{P_{tot}}\ \text{K/W}$$

To ensure thermal stability the value of the ambient temperature $T_{amb} > 40$ °C.

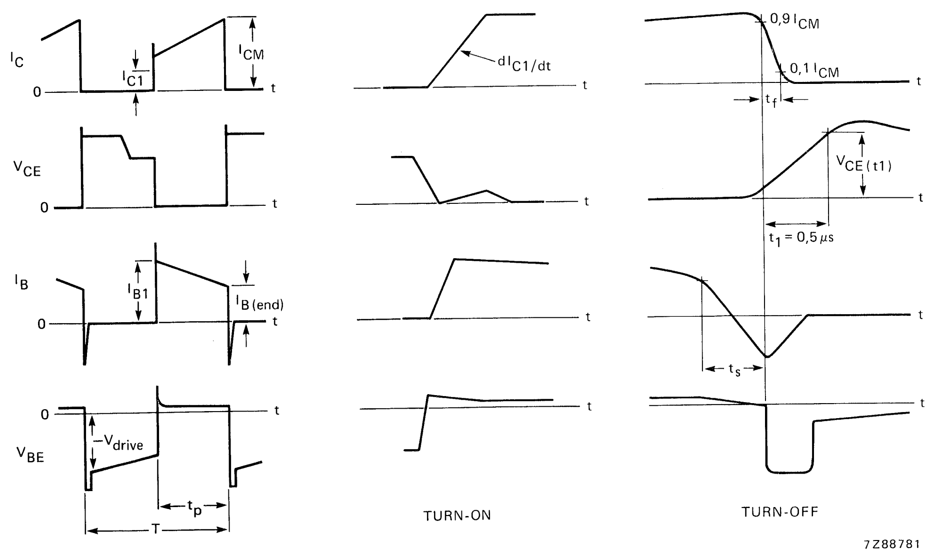


Fig. 15 Relevant waveforms of the switching transistor in a forward SMPS.

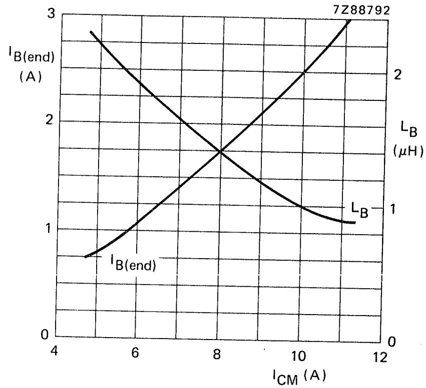


Fig. 16 Recommended nominal "end" value of the base current (I_{Be}) and optimum base inductance (L_B) at $-V_{drive}$ = 5 V versus maximum peak collector current. $dI_{B(end)} = \pm 20\%$.

For other values of $-V_{drive}$ (3 V to 7 V) the related L_B is:

$$L_{Bnom} \frac{(-V_{drive}) + 1}{6}$$

L_{Bnom} is the value given in this graph.

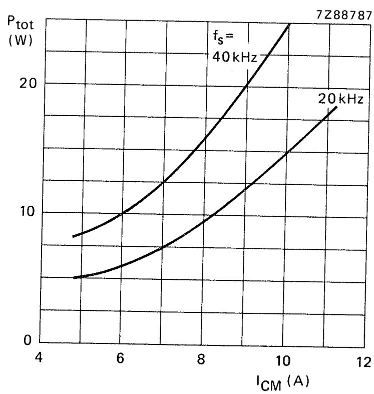


Fig. 17 Maximum transistor dissipation under worse-case operating condition versus maximum peak collector current. T_{mb} = 100 °C; $dI_{B(end)} = \pm 20\%$.

SILICON DIFFUSED POWER TRANSISTORS

High-voltage, high-speed, glass-passivated n-p-n power transistors in a TO-3 envelope, indended for use in converters, inverters, switching regulators, motor control systems etc.

QUICK REFERENCE DATA

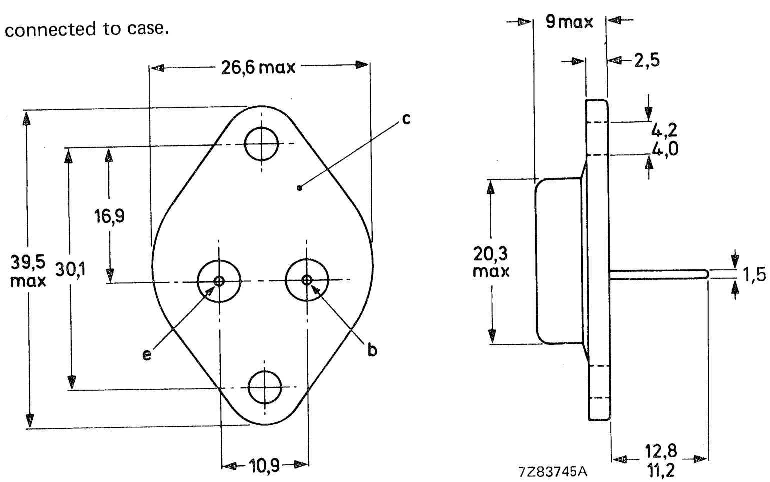
			BUS14	BUS14A	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	30	30	A
Collector current (peak value) $t_p \leq 2$ ms	I_{CM}	max.	50	50	A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	250	250	W
Collector-emitter saturation voltage					
I_C = 20 A; I_B = 4 A	V_{CEsat}	<	1,5	—	V
I_C = 16 A; I_B = 3,2 A	V_{CEsat}	<	—	1,5	V
Fall time (resistive load)					
I_{Con} = 20 A; I_{Bon} = $-I_{Boff}$ = 4 A	t_f	<	0,8	—	μs
I_{Con} = 16 A; I_{Bon} = $-I_{Boff}$ = 3,2 A	t_f	<	—	0,8	μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Collector connected to case.



See also chapters Mounting instructions and Accessories.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BUS14	BUS14A	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	30		A
Collector current (peak value); $t_p < 2$ ms	I_{CM}	max.	50		A
Base current (d.c.)	I_B	max.	6		A
Base current (peak value); $t_p < 2$ ms	I_{BM}	max.	10		A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	250		W
Storage temperature	T_{stg}		−65 to +200		°C
Junction temperature	T_j	max.	200		°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	0,7	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current *				
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$	I_{CES}	<	1	mA
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$; T_j = 125 °C	I_{CES}	<	5	mA
Emitter cut-off current				
$I_C = 0$; V_{EB} = 9 V	I_{EBO}	<	10	mA

			BUS14	BUS14A	
Saturation voltages					
I_C = 20 A; I_B = 4 A	V_{CEsat}	<	1,5	–	V
I_C = 16 A; I_B = 3,2 A	V_{CEsat}	<	–	1,5	V
I_C = 20 A; I_B = 4 A	V_{BEsat}	<	1,7	–	V
I_C = 16 A; I_B = 3,2 A	V_{BEsat}	<	–	1,7	V
Collector-emitter sustaining voltage					
I_C = 100 mA; I_{Boff} = 0; L = 25 mH	$V_{CEOsust}$	>	400	450	V

* Measured with a half sine-wave voltage (curve tracer).

CHARACTERISTICS (continued)

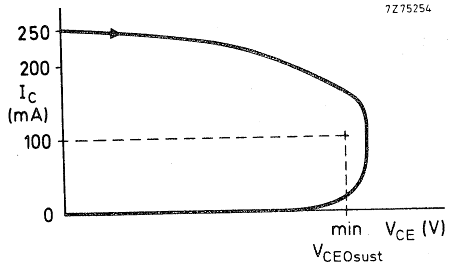


Fig. 2 Oscilloscope display for sustaining voltage.

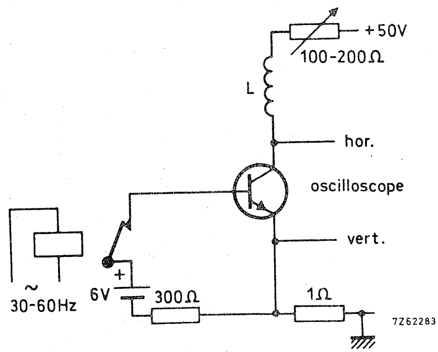


Fig. 3 Test circuit for $V_{CEOsust}$.

			BUS14	BUS14A	
Switching times resistive load (Figs 4 and 5)					
I_{Con} = 20 A; $I_{Bon} = -I_{Boff}$ = 4 A					
Turn-on time	t_{on}	<	1	–	μs
Turn-off: Storage time	t_s	<	4	–	μs
Fall time	t_f	<	0,8	–	μs
I_{Con} = 16 A; $I_{Bon} = -I_{Boff}$ = 3,2 A					
Turn-on time	t_{on}	<	–	1	μs
Turn-off: Storage time	t_s	<	–	4	μs
Fall time	t_f	<	–	0,8	μs
Switching times inductive load (Figs 6 and 7)					
I_{Con} = 20 A; I_B = 4 A					
Turn-off: Storage time	t_s	typ.	2,8	–	μs
		<	3,6	–	μs
Fall time	t_f	typ.	80	–	ns
		<	150	–	ns
I_{Con} = 20 A; I_B = 4 A; T_j = 100 °C					
Turn-off: Storage time	t_s	typ.	3,1	–	μs
		<	4,0	–	μs
Fall time	t_f	typ.	140	–	ns
		<	300	–	ns
Switching times inductive load (Figs 6 and 7)					
I_{Con} = 16 A; I_B = 3,2 A					
Turn-off: Storage time	t_s	typ.	–	28	μs
		<	–	3,6	μs
Fall time	t_f	typ.	–	80	ns
		<	–	150	ns
I_{Con} = 16 A; I_B = 3,2 A; T_j = 100 °C					
Turn-off: Storage time	t_s	typ.	–	3,1	μs
		<	–	4,0	μs
Fall time	t_f	typ.	–	140	ns
		<	–	300	ns

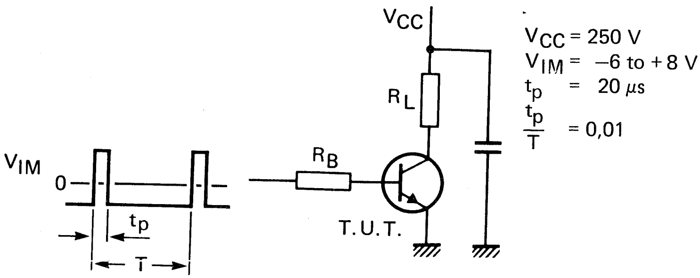


Fig. 4 Test circuit resistive load.

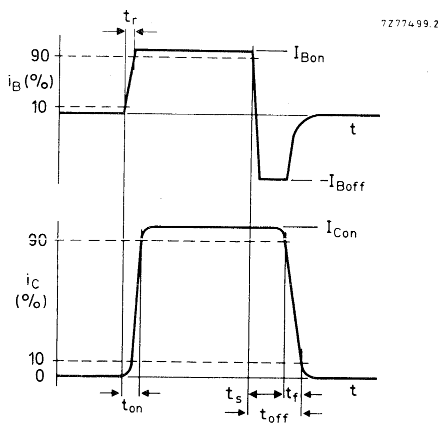


Fig. 5 Switching times waveforms with resistive load.

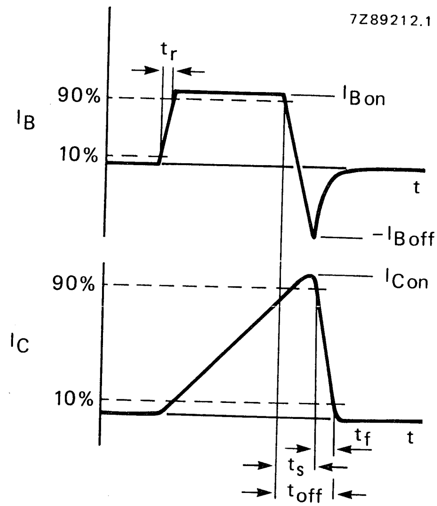


Fig. 6 Switching times waveforms with inductive load.

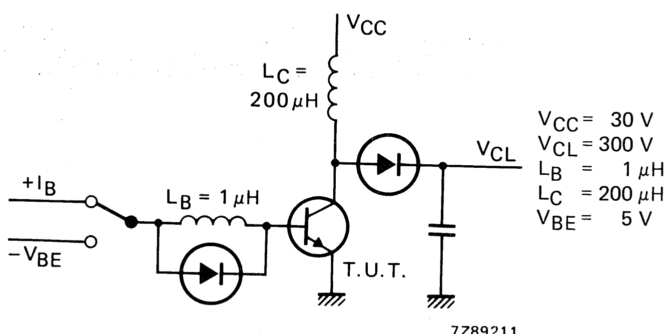


Fig. 7 Test circuit inductive load.

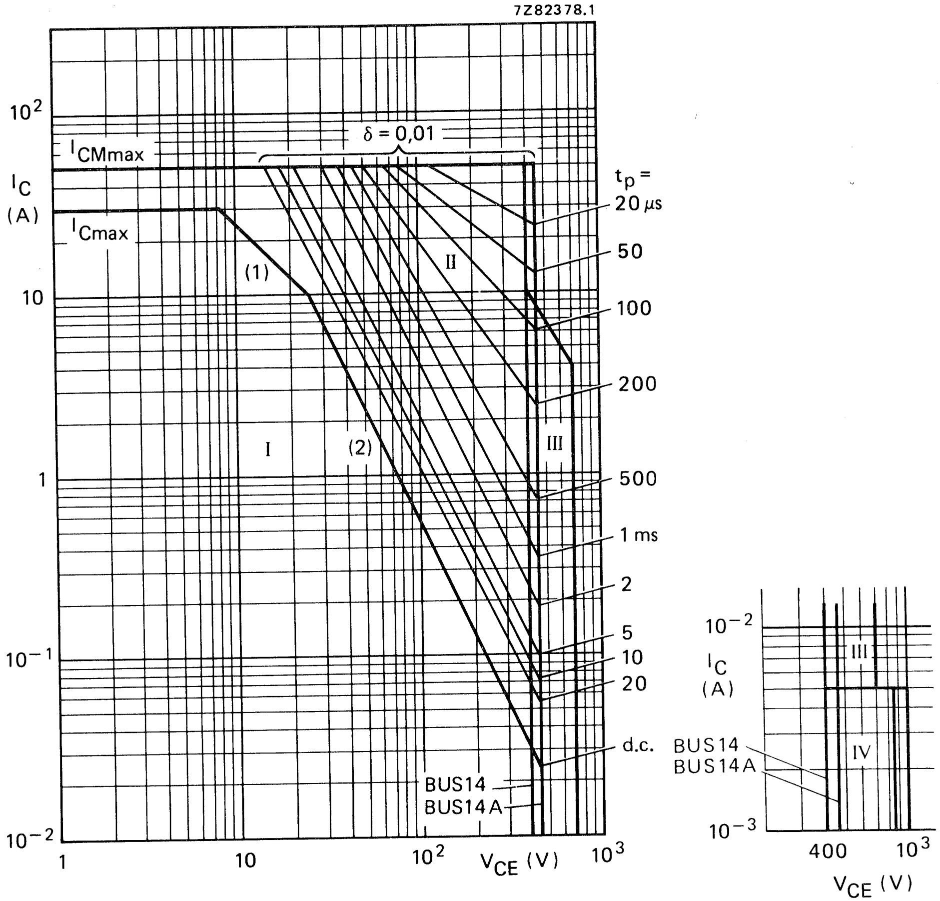


Fig. 8 Safe Operating ARea at $T_{mb} \leqslant 25\ ^oC$.

(1) $P_{tot\,max}$ and $P_{peak\,max}$ lines.
(2) Second-breakdown limits (independent of temperature).
I Region of permissible d.c. operation
II Permissible extension for repetitive pulse operation
III Area of permissible operation during turn-on in single transistor converters, provided $R_{BE} \leqslant 100\ \Omega$ and $t_p \leqslant 0,6\ \mu s$
IV Repetitive pulse operation in this region is permissible provided $V_{BE} \leqslant 0$ and $t_p \leqslant 2$ ms.

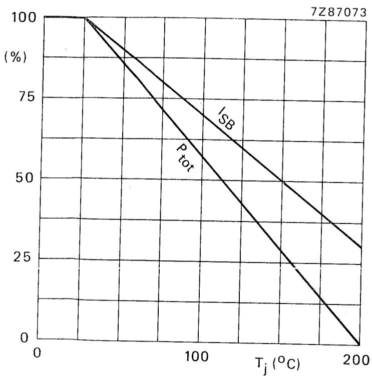


Fig. 9 Total power dissipation and second-breakdown current derating curve.

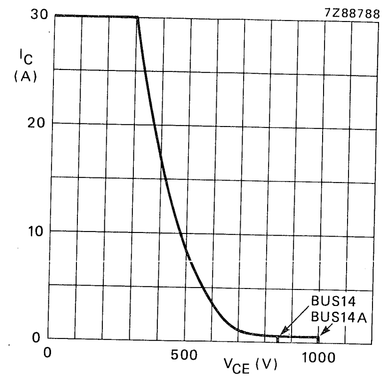


Fig. 10 Reverse bias SOAR.

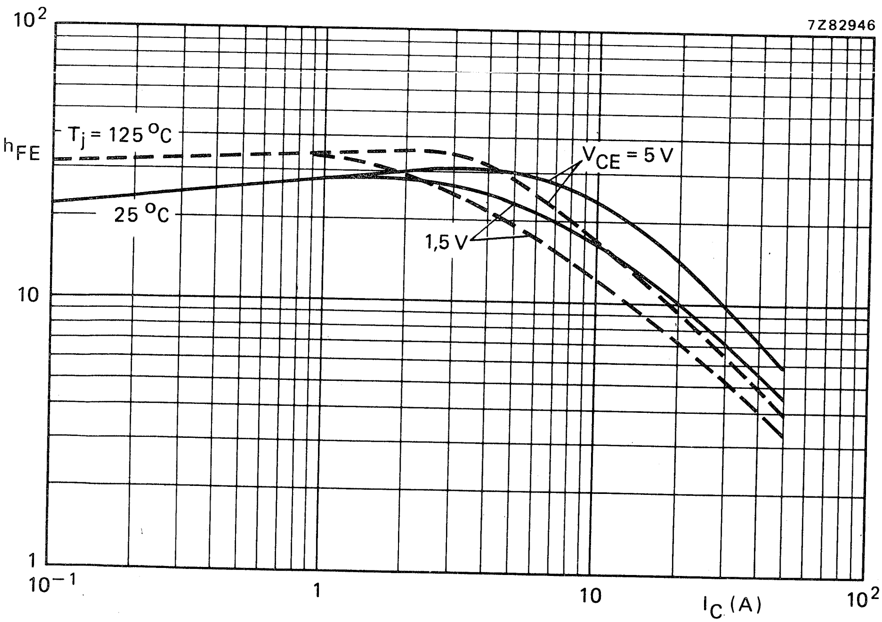


Fig. 11 Typical values d.c. current gain.

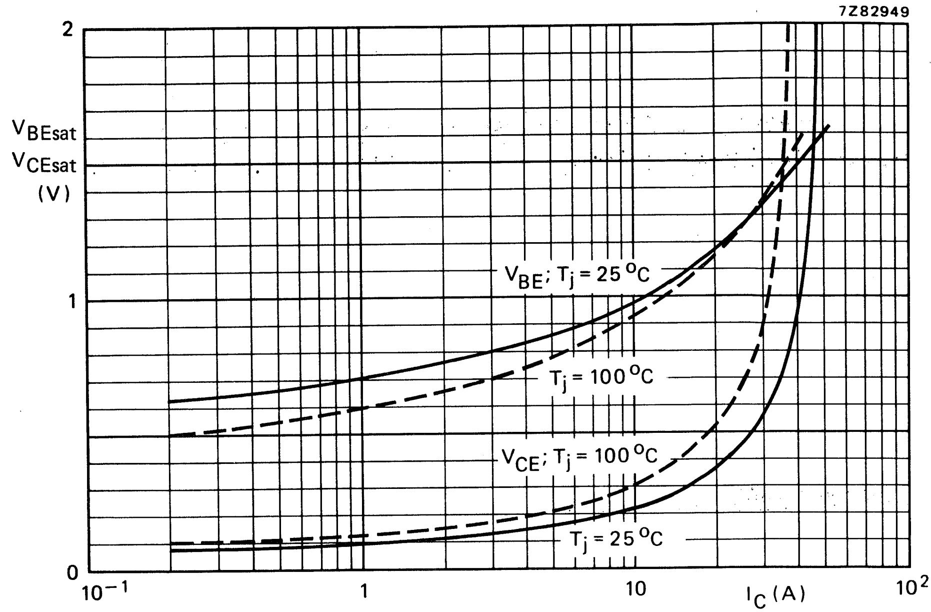


Fig. 12 Typical values base and collector voltage. $I_C/I_B = 5$.

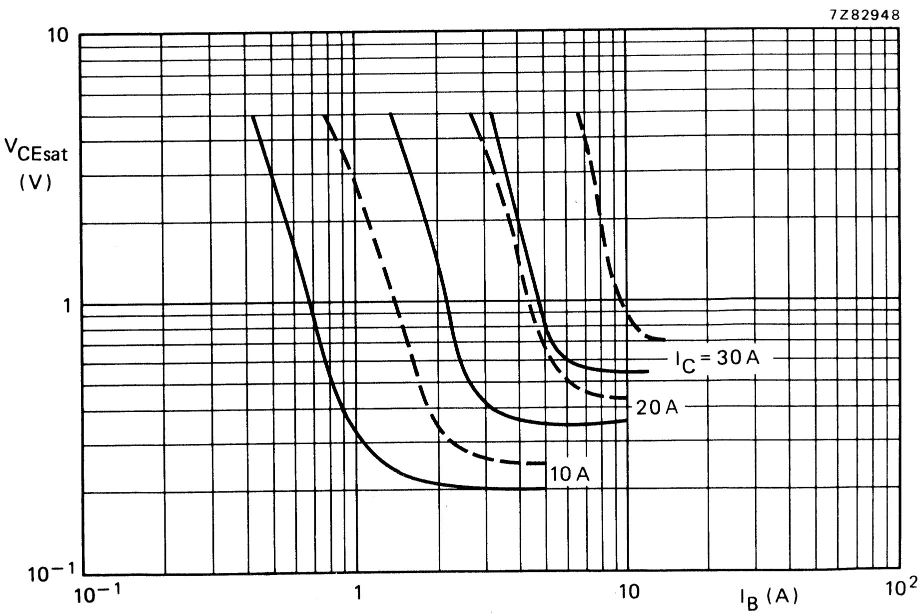


Fig. 13 Typical (——) and maximum (– – –) values saturation voltage. T_j = 25 °C.

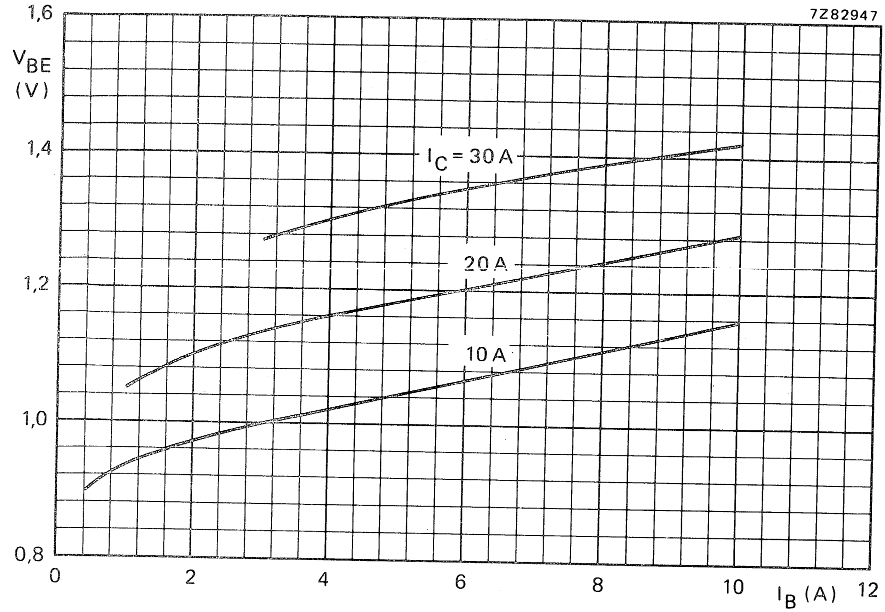


Fig. 14 Typical values at T_j = 25 °C.

APPLICATION INFORMATION

Important design factors of SMPS circuits are the maximum power losses, heatsink requirements and base drive conditions of the switching transistor. The power losses are very dependent on the operating frequency, the maximum collector current amplitude and shape.

The operating frequency is mostly set between 15 and 50 kHz. The collector current shape varies from rectangular in a forward converter to sawtooth in a flyback converter.

Information on nominal base drive, optimum base inductance and maximum transistor dissipation applied in a forward converter is given in Figs 15, 16 and 17. In these figures I_{CM} represents the maximum repetitive peak collector current, which occurs during overload. The information is derived from limit-case transistors at a mounting base temperature of 100 °C under the following conditions (see also Fig. 15):

- collector current shape $I_{C1}/I_{CM} = 0,9$
- duty factor $t_p/T = 0,45$
- rate of rise of I_C during turn-on = 20 A/μs
- rate of rise of V_{CE} during turn-off = 1 kV/μs
- reverse drive voltage during turn-off = 5 V
- base current shape $I_{B1}/I_{Be} = 1,5$

The required thermal resistance of the heatsink can be calculated from

$$R_{th\ mb\text{-}a} < \frac{100 - T_{amb}}{P_{tot}}\ \text{K/W}$$

To ensure thermal stability the value of the ambient temperature $T_{amb} > 40$ °C.

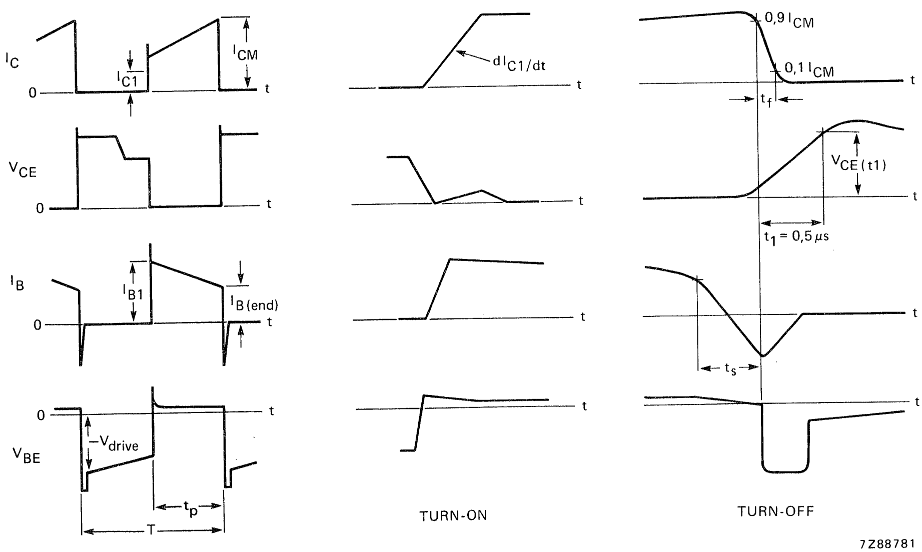


Fig. 15 Relevant waveforms of the switching transistor in a forward SMPS.

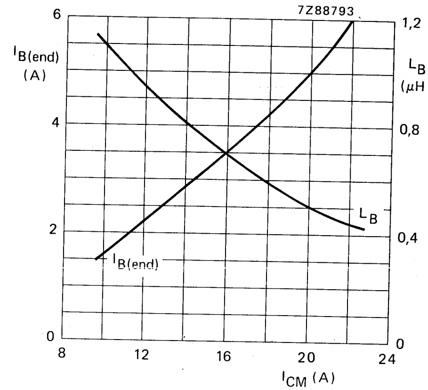


Fig. 16 Recommended nominal "end" value of the base current (I_{Be}) and optimum base inductance (L_B) at $-V_{drive} = 5$ V versus maximum peak collector current. $dI_{B(end)} = \pm 20\%$.

For other values of $-V_{drive}$ (3 V to 7 V) the related L_B is:

$$L_{Bnom} \frac{(-V_{drive}) + 1}{6}$$

L_{Bnom} is the value given in this graph.

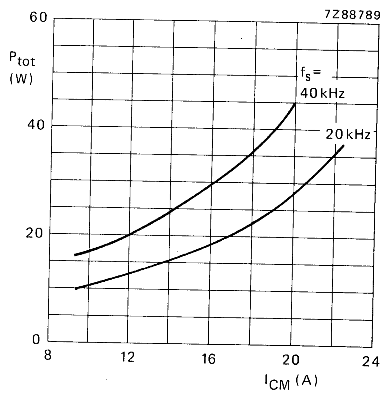


Fig. 17 Maximum transistor dissipation under worse-case operating condition versus maximum peak collector current. $T_{mb} = 100$ °C; $dI_{B(end)} = \pm 20\%$.

SILICON DIFFUSED POWER TRANSISTORS

High-voltage, high-speed, glass-passivated n-p-n power transistors in a TO-220 envelope, intended for use in converters, inverters, switching regulators, motor control systems etc.

QUICK REFERENCE DATA

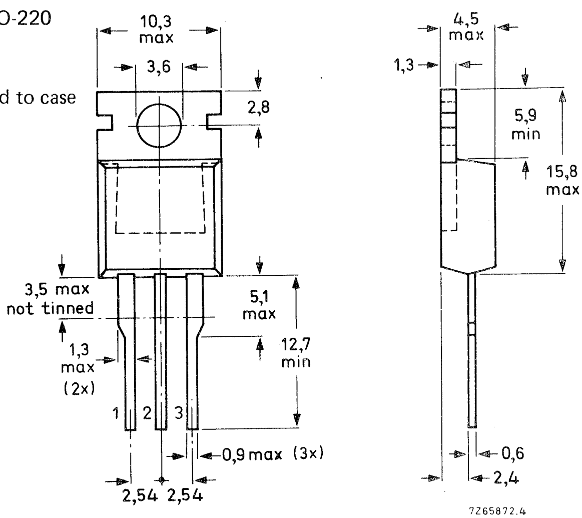
			BUT11	BUT11A	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	5		A
Collector current (peak value) $t_p \leq 2$ ms	I_{CM}	max.	10		A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	100		W
Collector-emitter saturation voltage					
I_C = 3 A; I_B = 0,6 A	V_{CEsat}	<	1,5	–	V
I_C = 2,5 A; I_B = 0,5 A	V_{CEsat}	<	–	1,5	V
Fall time					
I_{Con} = 3 A; I_{Bon} = $-I_{Boff}$ = 0,6 A	t_f	<	0,8	–	µs
I_{Con} = 2,5 A; I_{Bon} = $-I_{Boff}$ = 0,5 A	t_f	<	–	0,8	µs

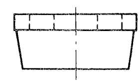
MECHANICAL DATA

Dimensions in mm

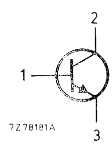
Fig. 1 TO-220

Collector connected to case





top view



See also chapters Mounting instructions and Accessories.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).

			BUT11	BUT11A	
Collector-emitter voltage (peak value, $V_{BE} = 0$)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	5		A
Collector current (peak value) $t_p < 2$ ms	I_{CM}	max.	10		A
Base current (d.c.)	I_B	max.	2		A
Base current (peak value); $t_p < 2$ ms	I_{BM}	max.	4		A
Total power dissipation up to $T_{mb} = 25\ ^oC$	P_{tot}	max.	100		W
Storage temperature	T_{stg}		−65 to + 150		^oC
Junction temperature	T_j	max.	150		^oC

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1,25	K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

			BUT11	BUT11A	
Collector cut-off current *					
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$	I_{CES}	<	1		mA
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$; $T_j = 125\ ^oC$	I_{CES}	<	2		mA
Emitter cut-off current					
$I_C = 0$; $V_{EB} = 9$ V	I_{EBO}	<	10		mA
Saturation voltages					
$I_C = 3$ A; $I_B = 0,6$ A	V_{CEsat}	<	1,5	–	V
	V_{BEsat}	<	1,3	–	V
$I_C = 2,5$ A; $I_B = 0,5$ A	V_{CEsat}	<	–	1,5	V
	V_{BEsat}	<	–	1,3	V
Collector-emitter sustaining voltage					
$I_C = 100$ mA; $I_{Boff} = 0$; L = 25 mA	$V_{CEOsust}$	>	400	450	V

* Measured with a half sine-wave voltage (curve tracer).

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

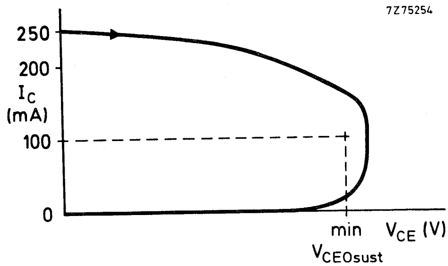


Fig. 2 Oscilloscope display for sustaining voltage.

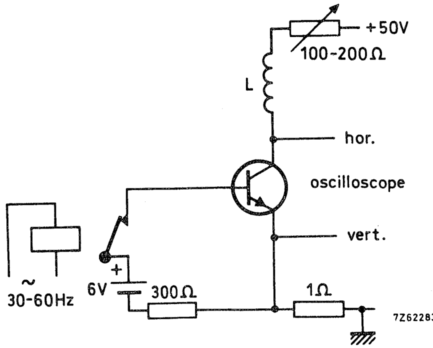
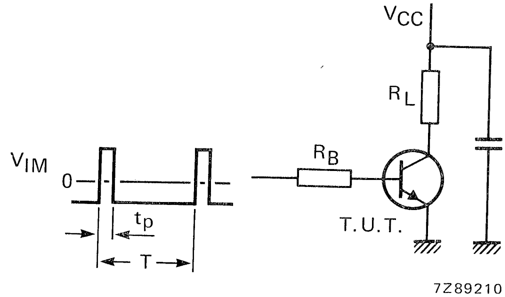


Fig. 3 Test circuit for $V_{CEOsust}$.

			BUT11	BUT11A	
Switching times resistive load (Figs 4 and 5)					
I_{Con} = 3 A; $I_{Bon} = -I_{Boff}$ = 0,6 A					
Turn-on time	t_{on}	<	1	–	μs
Turn-off: Storage time	t_s	<	4	–	μs
Fall time	t_f	<	0,8	–	μs
I_{Con} = 2,5 A; $I_{Bon} = -I_{Boff}$ = 0,5 A					
Turn-on time	t_{on}	<	–	1	μs
Turn-off: Storage time	t_s	<	–	4	μs
Fall time	t_f	<	–	0,8	μs
Switching times inductive load (Figs 6 and 7)					
I_{Con} = 3 A; I_B = 0,6 A					
Turn-off: Storage time	t_s	typ.	1,1	–	μs
		<	1,4	–	μs
Fall time	t_f	typ.	80	–	ns
		<	150	–	ns
I_{Con} = 3 A; I_B = 0,6 A; T_j = 100 °C					
Turn-off: Storage time	t_s	typ.	1,2	–	μs
		<	1,5	–	μs
Fall time	t_f	typ.	140	–	ns
		<	300	–	ns
Switching times inductive load (Figs 6 and 7)					
I_{Con} = 2,5 A; I_B = 0,5 A					
Turn-off: Storage time	t_s	typ.	–	1,1	μs
		<	–	1,4	μs
Fall time	t_f	typ.	–	80	ns
		<	–	150	ns
I_{Con} = 2,5 A; I_B = 0,5 A; T_j = 100 °C					
Turn-off: Storage time	t_s	typ.	–	1,2	μs
		<	–	1,5	μs
Fall time	t_f	typ.	–	140	ns
		<	–	300	ns



V_{CC} = 250 V
V_{IM} = −6 to +8 V
$\frac{t_p}{T}$ = 0,01
t_p = 20 μs

The values of R_B and R_L are selected in accordance with I_{Con} and I_B requirements.

Fig. 4 Test circuit resistive load.

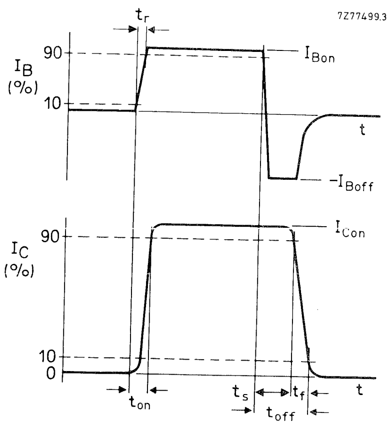


Fig. 5 Switching times waveforms with resistive load.

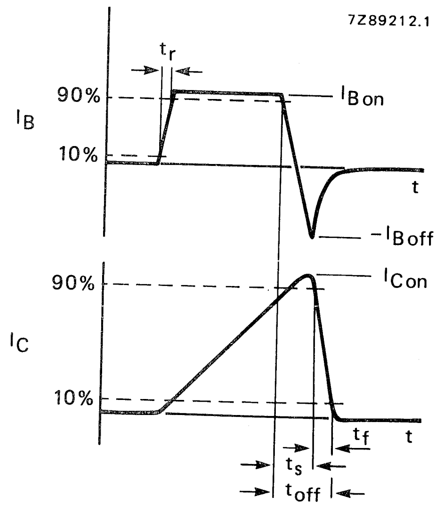
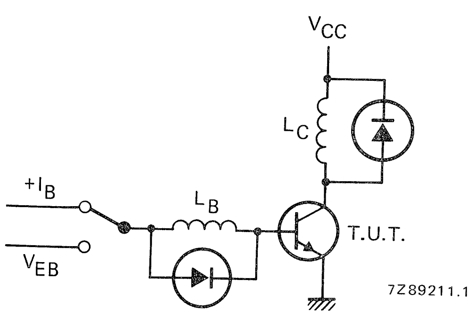


Fig. 6 Switching times waveforms with inductive load.



V_{CL} = 300 V
V_{CC} = 30 V
V_{EB} = 5 V

Fig. 7 Test circuit inductive load.

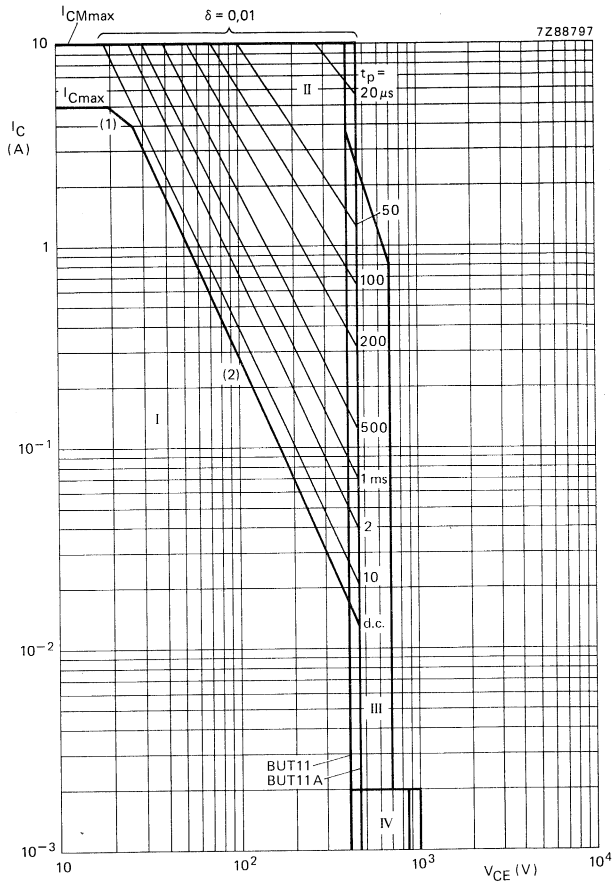


Fig. 8 Safe Operating ARea at $T_{mb} \leqslant 25$ °C.

(1) $P_{tot\,max}$ and $P_{tot\,peak}$ max. lines.
(2) Second-breakdown limits (independent of temperature).

I Region of permissible d.c. operation
II Permissible extension for repetitive pulse operation
III Area of permissible operation during turn-on in single transistor converters, provided $R_{BE} \leqslant 100\ \Omega$ and $t_p \leqslant 0{,}6$ μs.
IV Repetitive pulse operation in this region is permissible provided $V_{BE} \leqslant 0$ and $t_p \leqslant 5$ ms.

DEVELOPMENT SAMPLE DATA

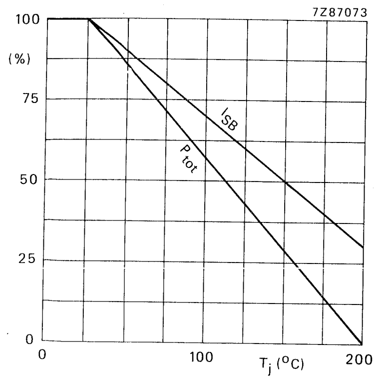


Fig. 9 Total power dissipation and second-breakdown current derating curve.

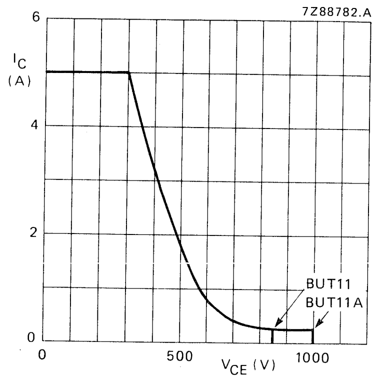


Fig. 10 Reverse bias SOAR.

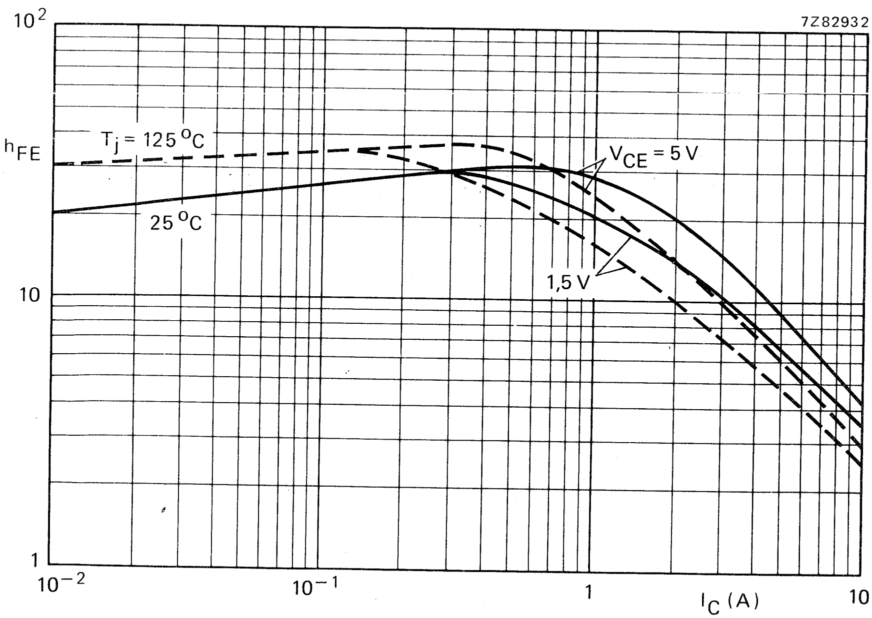


Fig. 11 D.C. current gain.

DEVELOPMENT SAMPLE DATA

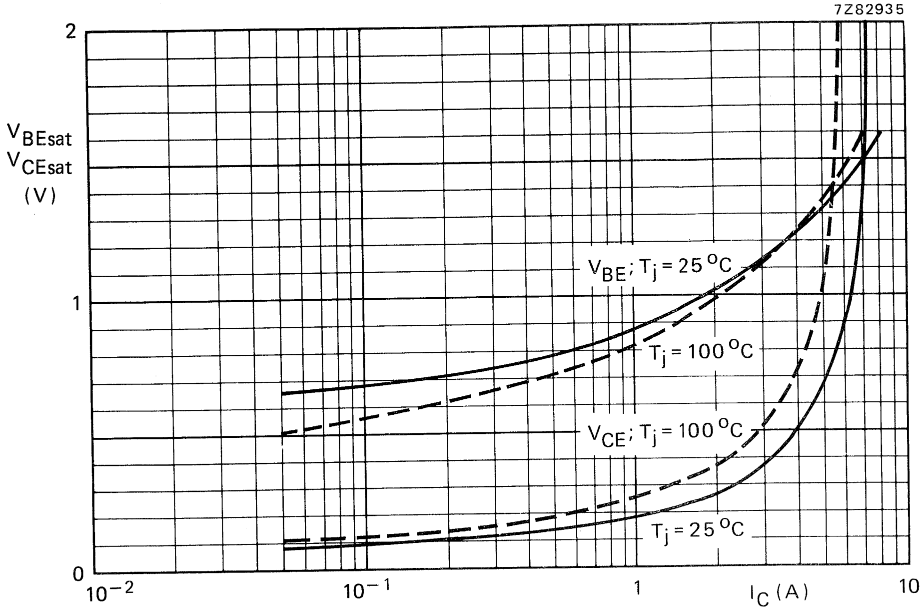


Fig. 12 Typical values base-emitter and collector-emitter voltage, $I_C/I_B = 5$.

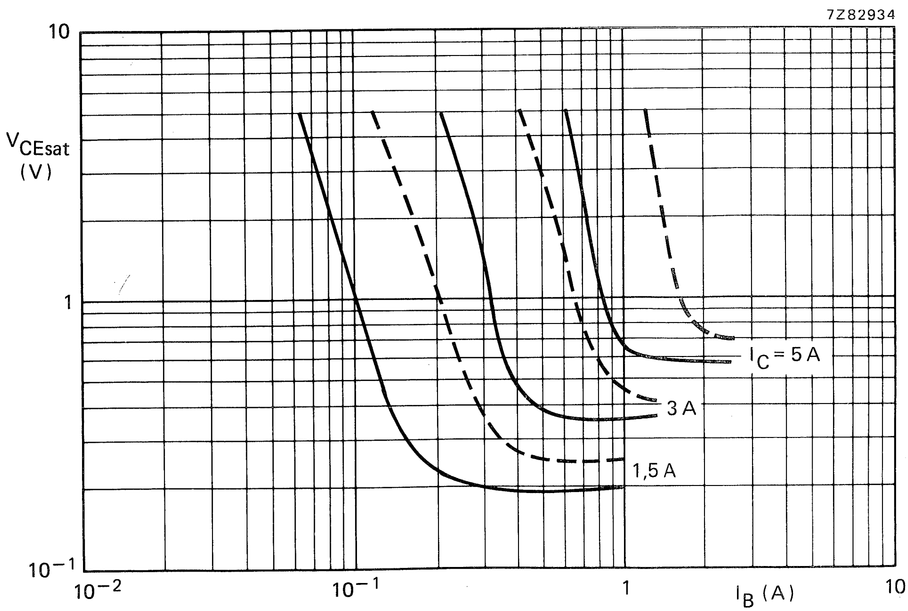


Fig. 13 Typ. (——) and max. (– – –) values collector-emitter saturation voltage at T_j = 25 °C.

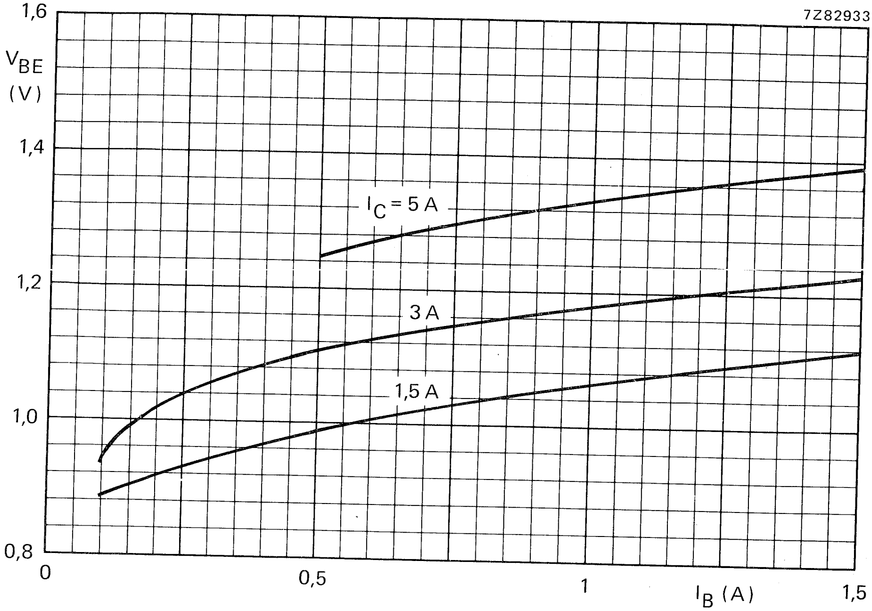


Fig. 14 Typical values at T_j = 25 °C.

APPLICATION INFORMATION

Important design factors of SMPS circuits are the maximum power losses, heatsink requirements and base drive conditions of the switching transistor. The power losses are very dependent on the operating frequency, the maximum collector current amplitude and shape.

The operating frequency is mostly set between 15 and 50 kHz. The collector current shape varies from rectangular in a forward converter to sawtooth in a flyback converter.

Information on nominal base drive, optimum base inductance and maximum transistor dissipation applied in a forward converter is given in Figs 15, 16 and 17. In these figures I_{CM} represents the maximum repetitive peak collector current, which occurs during overload. The information is derived from limit-case transistors at a mounting base temperature of 100 °C under the following conditions (see also Fig. 15):

- collector current shape $I_{C1}/I_{CM} = 0,9$
- duty factor $(t_p/T) = 0,45$
- rate of rise of I_C during turn-on = 4 A/µs
- rate of rise of V_{CE} during turn-off = 1 kV/µs
- reverse drive voltage during turn-off = 5 V
- base current shape $I_{B1}/I_{Be} = 1,5$

The required thermal resistance of the heatsink can be calculated from

$$R_{th\ mb\text{-}a} < \frac{100 - T_{amb}}{P_{tot}}\ \text{K/W}$$

To ensure thermal stability the value of the ambient temperature $T_{amb} > 40$ °C.

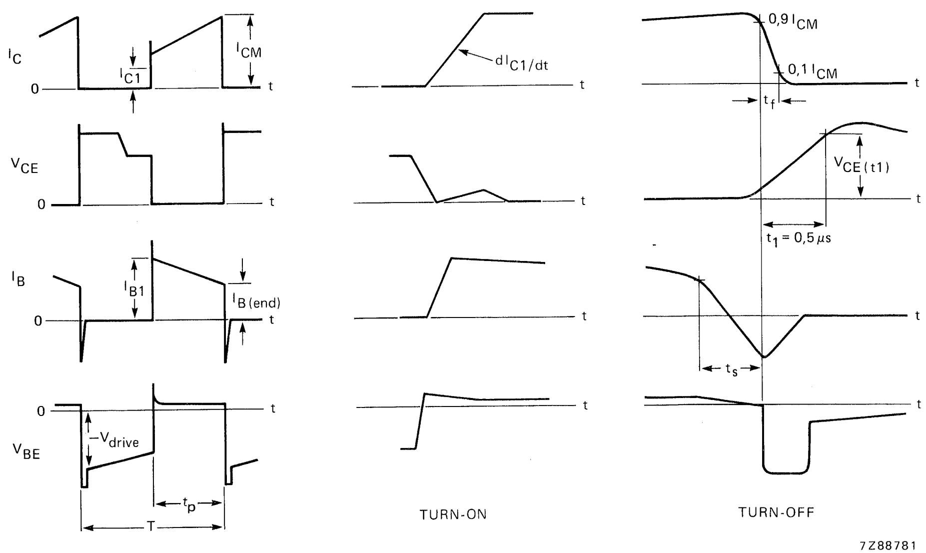


Fig. 15 Relevant waveforms of the switching transistor in a forward SMPS.

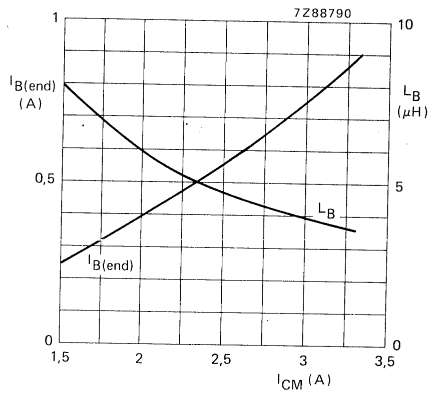


Fig. 16 Recommended nominal "end" value of the base current (I_{Be}) and optimum base inductance (L_B) at $-V_{drive}$ = 5 V versus maximum peak collector current. $dI_{B(end)}$ = ± 20%.

For other values of $-V_{drive}$ (3 V to 7 V) the related L_B is:

$$L_{Bnom} \frac{(-V_{drive}) + 1}{6}$$

L_{Bnom} is the value given in this graph.

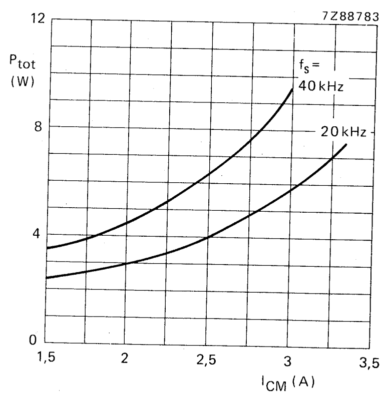


Fig. 17 Maximum transistor dissipation under worse-case operating condition versus maximum peak collector current. T_{mb} = 100 °C; $dI_{B(end)}$ = ± 20%.

SILICON DIFFUSED POWER TRANSISTORS

High voltage, high speed switching n-p-n power transistor in plastic SOT-93 envelope, intended for use in converters, inverters, switching regulators, motor control systems and switching applications.

QUICK REFERENCE DATA

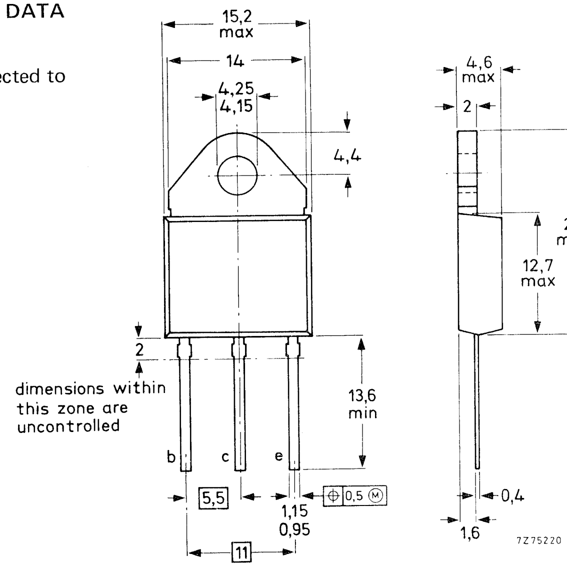
			BUV82	BUV83	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (R_{BE} = 100 Ω)	V_{CER}	max.	500	500	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	6		A
Collector current (peak value) t_p = 2 ms	I_{CM}	max.	10		A
Total power dissipation up to T_{mb} = 73 °C	P_{tot}	max.	70		W
Collector-emitter saturation voltage I_C = 2,5 A; I_B = 0,5 A	V_{CEsat}	<	1,5		V
Fall time I_{Con} = 2,5 A; I_{Bon} = 0,5 A; $-I_{Boff}$ = 1 A	t_f	typ.	0,3		μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-93.

Collector connected to mounting base



See also chapters Mounting instructions and Accessories.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BUV82	BUV83	
Collector-emitter voltage (V_{BE} = 0; peak value)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (R_{BE} = 100 Ω)	V_{CER}	max.	500	500	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	6		A
Collector current (peak value) t_p = 2 ms	I_{CM}	max.	10		A
Base current (d.c.)	I_B	max.	2		A
Base current (peak value)	I_{BM}	max.	3		A
Reverse base current (d.c. or average over any 20 ms period)	$-I_{B(AV)}$	max.	100		mA
Reverse base current (peak value)*	$-I_{BM}$	max.	3		A
Total power dissipation up to T_{mb} = 73 °C	P_{tot}	max.	70		W
Storage temperature	T_{stg}		−65 to + 150		°C
Junction temperature	T_j	max.	150		°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1,1	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current**				
$V_{CEM} = V_{CESMmax}$; $V_{BE} = 0$	I_{CES}	<	1	mA
$V_{CEM} = V_{CESMmax}$; $V_{BE} = 0$; T_j = 125 °C	I_{CES}	<	2	mA
D.C. current gain				
I_C = 0,6 A; V_{CE} = 5 V	h_{FE}	typ.	35	

* Turn-off current.

** Measured with a half sine wave voltage (curve tracer).

CHARACTERISTICS (continued)

T_j = 25 °C unless otherwise specified

Emitter cut-off current					
I_C = 0; V_{EB} = 10 V	I_{EBO}	<	10		mA
Saturation voltages					
I_C = 2,5 A; I_B = 0,5 A	V_{CEsat}	<	1,5		V
	V_{BEsat}	<	1,4		V
I_C = 4 A; I_B = 1,25 A	V_{CEsat}	<	3		V
	V_{BEsat}	<	1,6		V
			BUV82	BUV83	
Collector-emitter sustaining voltages					
I_C = 100 mA; I_{Boff} = 0; L = 25 mH	$V_{CEOsust}$	>	400	450	V
I_C = 100 mA; R_{BE} = 100 Ω; L = 15 mH	$V_{CERsust}$	>	500	500	V

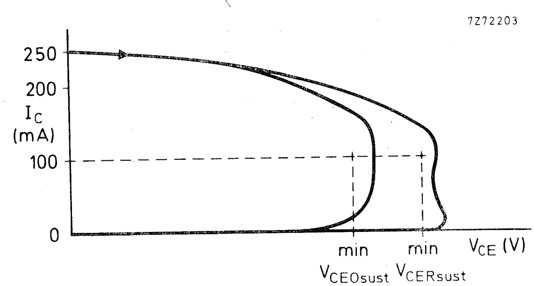


Fig. 2 Oscilloscope display for sustaining voltages.

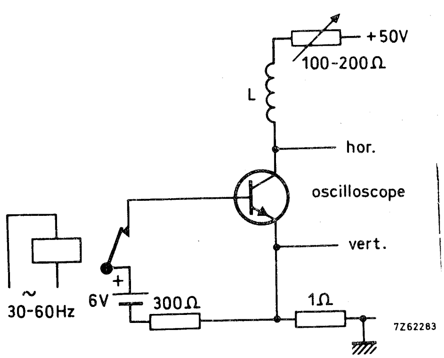


Fig. 3 Test circuit for $V_{CEOsust}$.

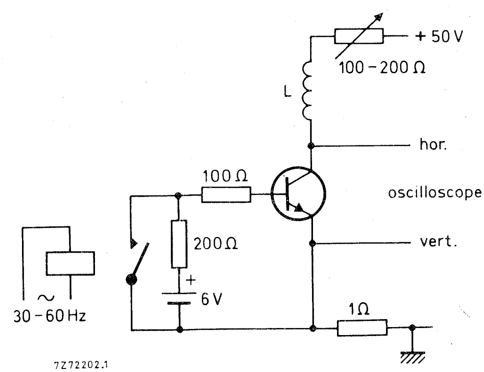


Fig. 4 Test circuit for $V_{CERsust}$.

CHARACTERISTICS (continued)

T_j = 25 °C unless otherwise specified

Transition frequency at f = 1 MHz I_C = 0,2 A; V_{CE} = 10 V	f_T	typ.	6 MHz
Switching times I_{Con} = 2,5 A; V_{CC} = 250 V I_{Bon} = 0,5 A; $-I_{Boff}$ = 1 A Turn-on time	t_{on}	typ. <	0,3 µs 0,6 µs
Turn-off: Storage time	t_s	typ. <	2 µs 3,5 µs
Fall time	t_f	typ.	0,3 µs
Fall time, T_{mb} = 95 °C	t_f	<	0,75 µs

Waveform

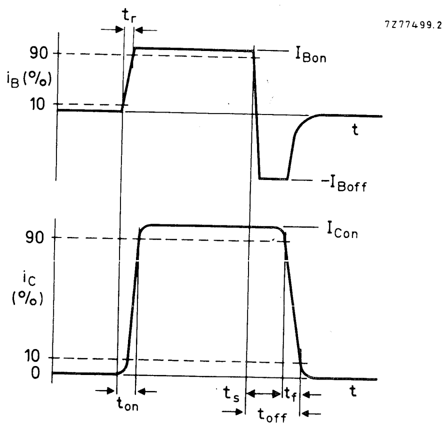
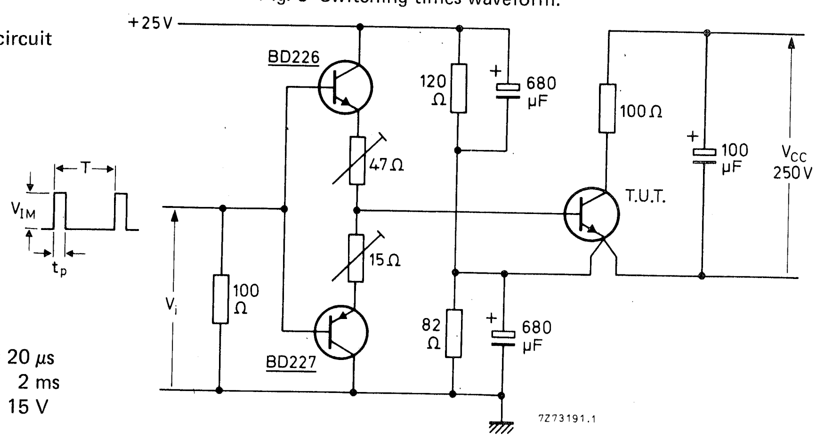


Fig. 5 Switching times waveform.

Test circuit



t_p = 20 µs
T = 2 ms
V_{IM} = 15 V

Fig. 6 Switching times test circuit.

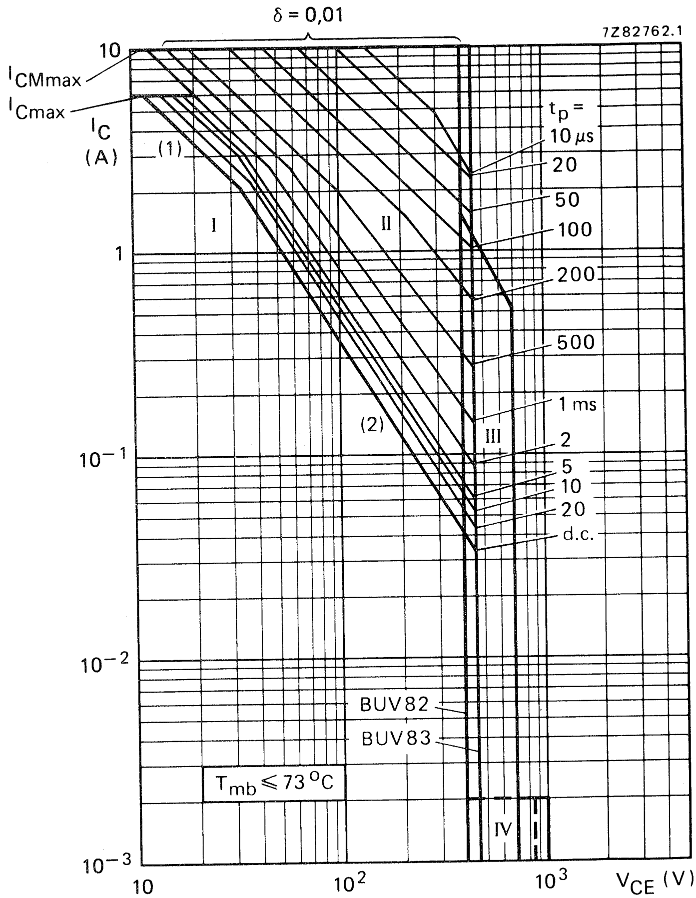


Fig. 7 Safe Operating ARea.

I Region of permissible d.c. operation.

II Permissible extension for repetitive pulse operation.

III Area of permissible operation during turn-on in single-transistor converters, provided $R_{BE} \leqslant 100\ \Omega$ and $t_p \leqslant 0,6\ \mu s$.

IV Repetitive pulse operation in this region is permissible, provided $V_{BE} \leqslant 0$ and $t_p \leqslant 2$ ms.

(1) $P_{tot\,max}$ and $P_{peak\,max}$ lines.

(2) Second-breakdown limits (independent of temperature).

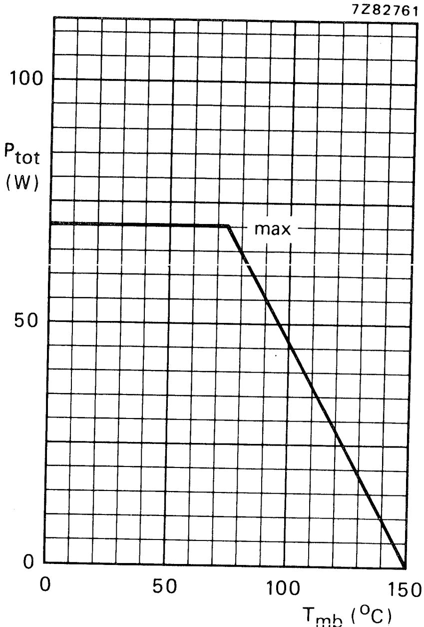


Fig. 8 Power derating curve.

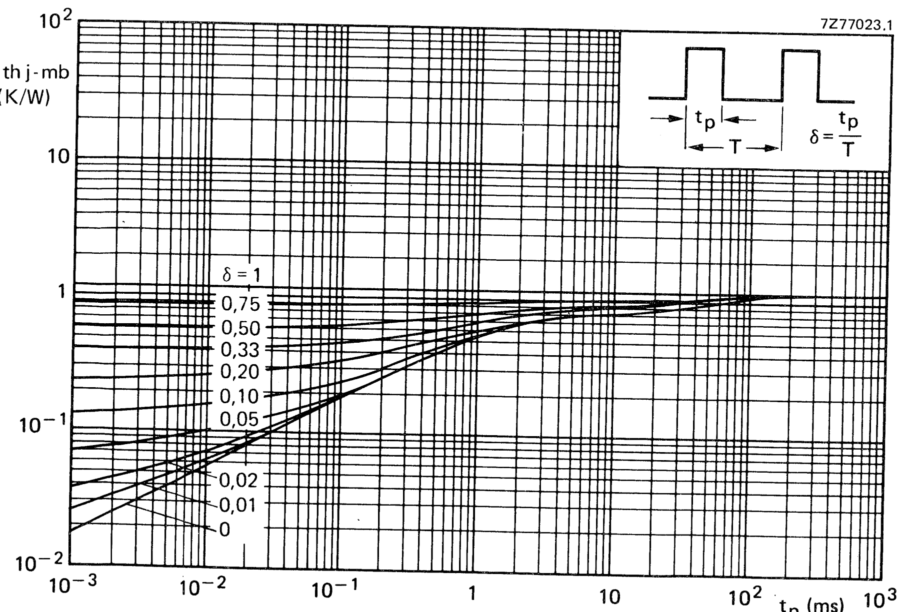


Fig. 9 Pulse power rating chart.

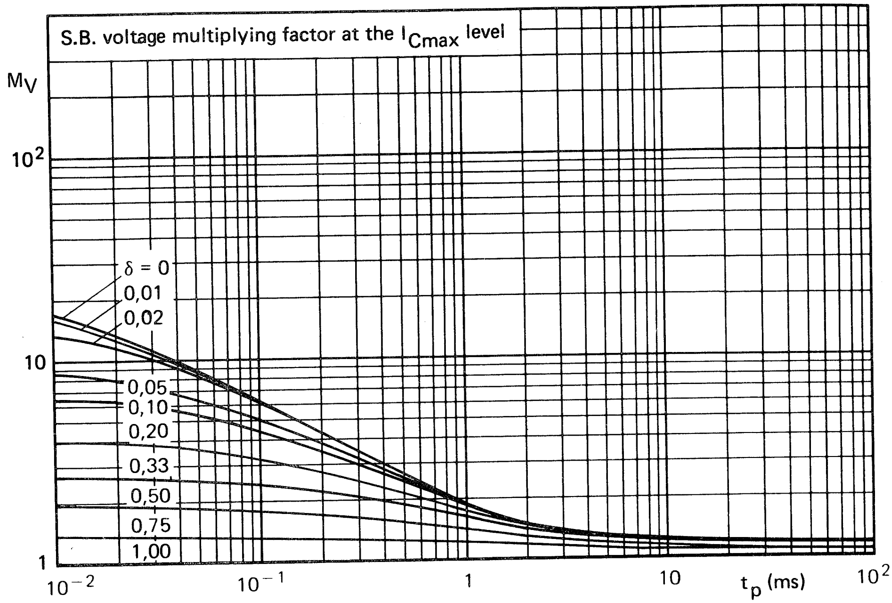


Fig. 10 S.B. voltage multiplying factor at the I_{Cmax} level.

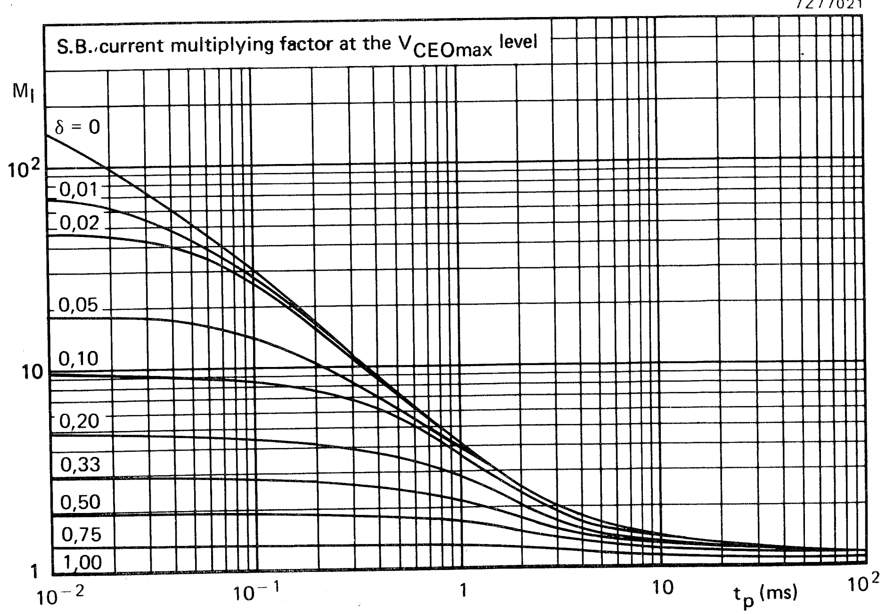


Fig. 11 S.B. current multiplying factor at the V_{CEOmax} level.

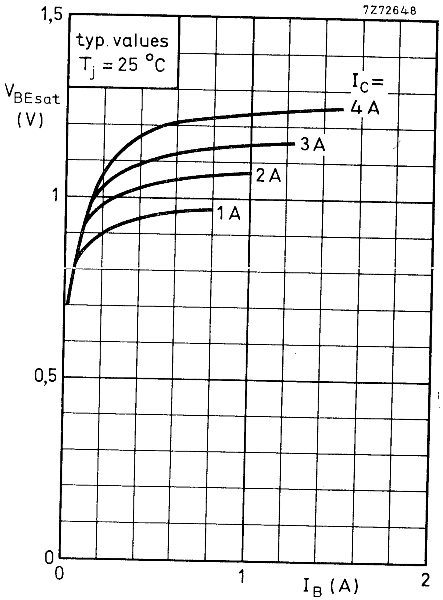


Fig. 12 Base-emitter saturation voltage.

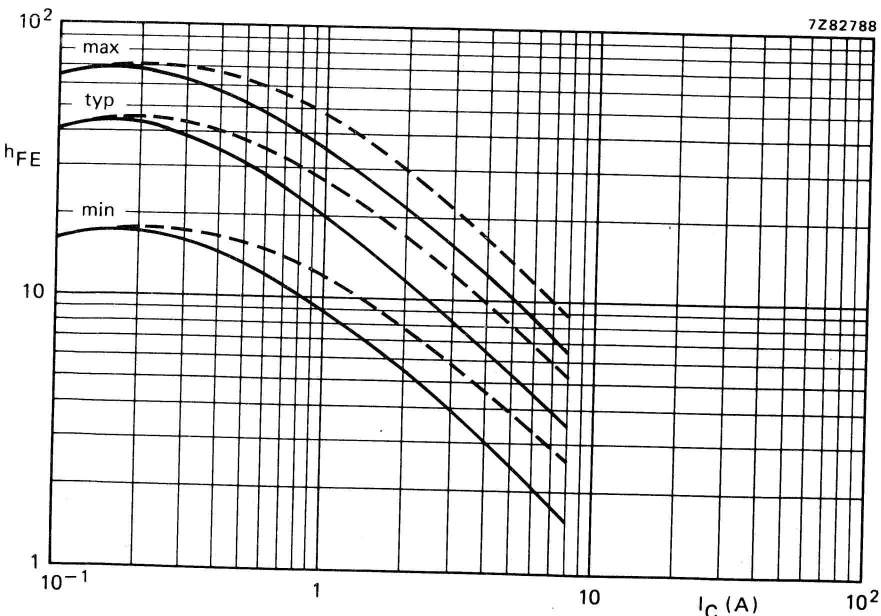


Fig. 13 D.C. current gain. T_j = 25 °C; — — — at V_{CE} = 5 V; —— at V_{CE} = 1 V.

SILICON DIFFUSED POWER TRANSISTOR

High-voltage, high-speed switching n-p-n transistor in a plastic SOT-93 envelope especially intended for use in a.c. motor control systems from three-phase mains.

QUICK REFERENCE DATA

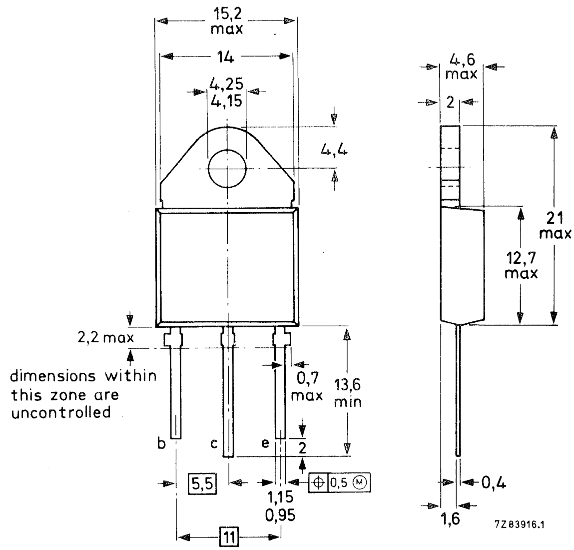
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	1200	V
Collector-emitter voltage (open base)	V_{CEO}	max.	800	V
Collector current (d.c.)	I_C	max.	8	A
Collector current (peak value)	I_{CM}	max.	15	A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	125	W
Collector-emitter saturation voltage I_C = 4,5 A; I_B = 2 A	V_{CEsat}	<	1	V
Turn-on fall time	t_f	typ.	0,5	μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT93A

Collector connected to mounting base.



See also chapters Mounting instructions and Accessories

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

→ Collector-emitter voltage (peak value; $V_{BE} = 0$)	V_{CESM}	max.	1200	V
Collector-emitter voltage (open base)	V_{CEO}	max.	800	V
Collector current (d.c.)	I_C	max.	8	A
Collector current (peak value)	I_{CM}	max.	15	A
Base current (d.c.)	I_B	max.	4	A
Base current (peak value)	I_{BM}	max.	6	A
Total power dissipation up to $T_{mb} = 25\ ^oC$	P_{tot}	max.	125	W
Storage temperature	T_{stg}		−65 to + 150	^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1,0	K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Collector cut-off current*				
$V_{BE} = 0$; $V_{CE} = V_{CESMmax}$	I_{CES}	<	1,0	mA
$V_{BE} = 0$; $V_{CE} = V_{CESMmax}$; $T_j = 125\ ^oC$	I_{CES}	<	2,0	mA
Emitter cut-off current				
$V_{EB} = 5$ V; $I_C = 0$	I_{EBO}	<	10	mA
Collector-emitter sustaining voltage				
$I_B = 0$; $I_C = 100$ mA; L = 25 mH	$V_{CEOsust}$	>	800	V
Saturation voltage				
$I_C = 4,5$ A; $I_B = 2$ A	V_{CEsat}	<	1	V
	V_{BEsat}	<	1,3	V
$I_C = 6$ A; $I_B = 3$ A	V_{CEsat}	typ.	1	V
Transition frequency at f = 5 MHz				
$I_C = 0,1$ A; $V_{CE} = 5$ V	f_T	typ.	7	MHz
Collector capacitance at f = 1 MHz				
$I_E = I_e = 0$; $V_{CB} = 10$ V	C_c	typ.	125	pF
Switching times in resistive switching circuit (Fig. 5)				
$I_{Con} = 4,5$ A; $I_{Bon} = -I_{Boff} = 2$ A				
Turn-on time	t_{on}	typ.	0,2	μs
Storage time	t_s	typ.	3,5	μs
Fall time	t_f	typ.	0,5	μs
Second-breakdown current				
$V_{CE} = 100$ V; $t_p = 1$ s	$I_{(SB)}$	>	0,3	A

* Measured with a half-sinewave voltage (curve tracer).

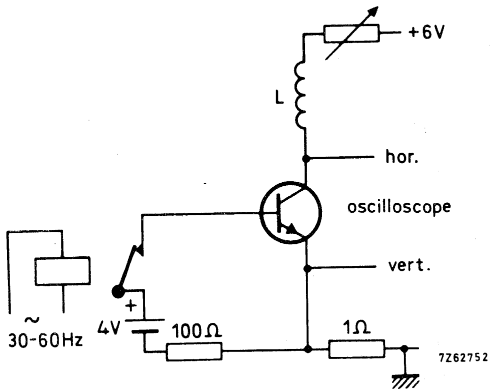


Fig. 2 Test circuit for $V_{CEOsust}$

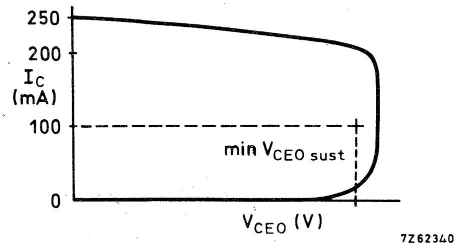


Fig. 3 Oscilloscope display for $V_{CEOsust}$.

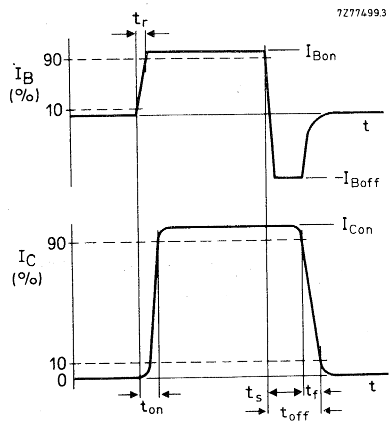


Fig. 4 Waveforms.

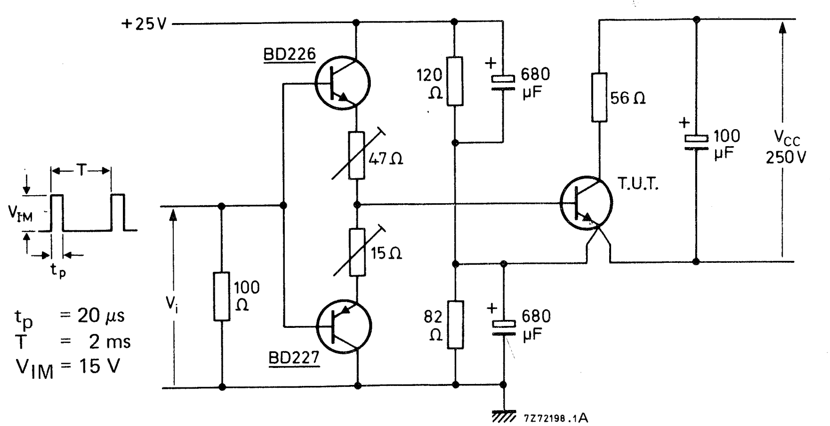


Fig. 5 Switching times test circuit.

DEVELOPMENT SAMPLE DATA

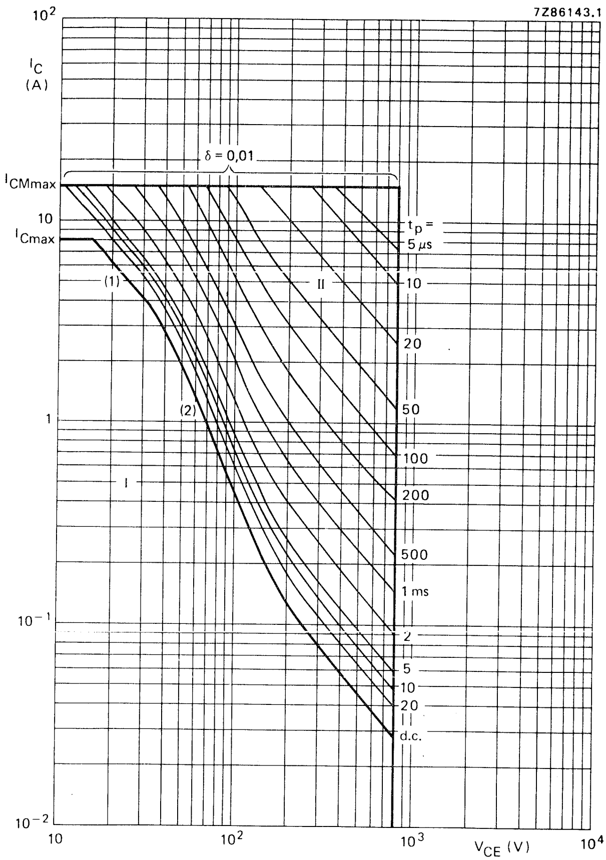


Fig. 6 Safe Operating ARea; $T_{mb} \leqslant 25\ ^{o}C$.

1. $P_{tot\ max}$ and $P_{tot\ peak}$ max. lines.
2. Second-breakdown limits (independent of temperature)

I Region of permissible d.c. operation.
II Permissible extension for repetitive pulse operation.

SILICON DIFFUSED POWER TRANSISTORS

High-voltage, high-speed, glass-passivated n-p-n power transistors in a SOT-93 envelope, intended for use in converters, inverters, switching regulators, motor control systems etc.

QUICK REFERENCE DATA

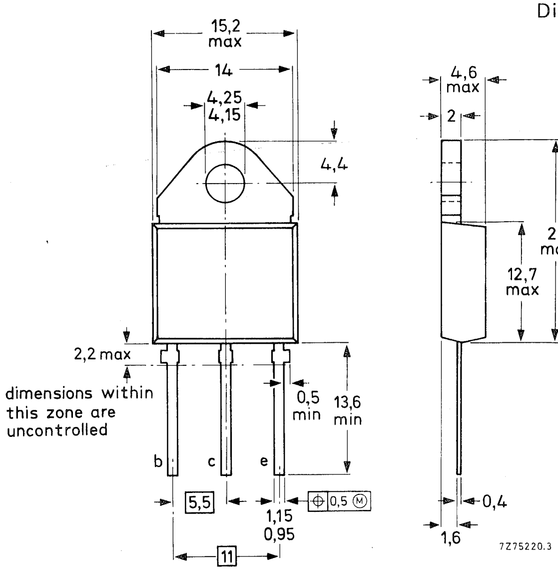
			BUW11	BUW11A	
Collector-emitter voltage ($V_{BE} = 0$, peak value)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	5		A
Collector current (peak value) $t_p \leq 2$ ms	I_{CM}	max.	10		A
Total power dissipation up to $T_{mb} = 25\ ^oC$	P_{tot}	max.	100		W
Collector-emitter saturation voltage					
$I_C = 3$ A; $I_B = 0,6$ A	V_{CEsat}	<	1,5	—	V
$I_C = 2,5$ A; $I_B = 0,5$ A	V_{CEsat}	<	—	1,5	V
Fall time (resistive load)					
$I_{Con} = 3$ A; $I_{Bon} = -I_{Boff} = 0,6$ A	t_f	<	0,8	—	μs
$I_{Con} = 2,5$ A; $I_{Bon} = -I_{Boff} = 0,5$ A	t_f	<	—	0,8	μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-93.

Collector connected to mounting base.



See also chapters Mounting instructions and Accessories.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BUW11	BUW11A	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	5		A
Collector current (peak value) $t_p < 2$ ms	I_{CM}	max.	10		A
Base current (d.c.)	I_B	max.	2		A
Base current (peak value); $t_p < 2$ ms	I_{BM}	max.	4		A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	100		W
Storage temperature	T_{stg}		−65 to + 150		°C
Junction temperature	T_j	max.	150		°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1,25	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current*				
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$	I_{CES}	<	1	mA
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$; T_j = 125 °C	I_{CES}	<	2	mA
Emitter cut-off current				
$I_C = 0$; $V_{EB} = 9$ V	I_{EBO}	<	10	mA

			BUW11	BUW11A	
Saturation voltages					
I_C = 3 A; I_B = 0,6 A	V_{CEsat}	<	1,5	–	V
	V_{BEsat}	<	1,4	–	V
I_C = 2,5 A; I_B = 0,5 A	V_{CEsat}	<	–	1,5	V
	V_{BEsat}	<	–	1,4	V
Collector-emitter sustaining voltage					
I_C = 100 mA; I_{Boff} = 0; L = 25 mH	$V_{CEOsust}$	>	400	450	V
Collector saturation current					
V_{CE} = 1,5 V	I_{Csat}	<	3	2,5	A

* Measured with a half sine-wave voltage (curve tracer).

CHARACTERISTICS (continued)

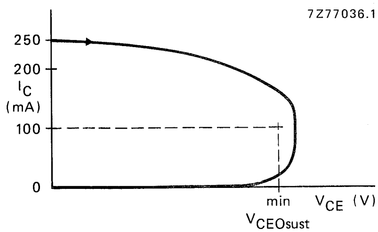


Fig. 2 Oscilloscope display for sustaining voltage.

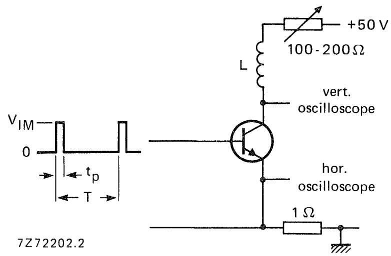
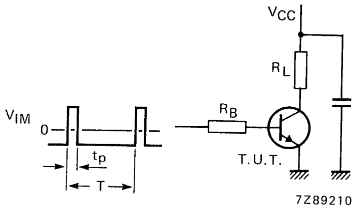


Fig. 3 Test circuit for $V_{CEOsust}$.

DEVELOPMENT SAMPLE DATA

			BUW11	BUW11A	
Switching times resistive load (Figs 4 and 5)					
I_{Con} = 3 A; I_{Bon} = I_{Boff} = 0,6 A					
Turn-on time	t_{on}	<	1	–	μs
Turn-off: Storage time	t_s	<	4	–	μs
Fall time	t_f	<	0,8	–	μs
I_{Con} = 2,5 A; I_{Bon} = $-I_{Boff}$ = 0,5 A					
Turn-on time	t_{on}	<	–	1	μs
Turn-off: Storage time	t_s	<	–	4	μs
Fall time	t_f	<	–	0,8	μs
Switching times inductive load (Figs 6 and 7)					
I_{Con} = 3 A; I_B = 0,6 A					
Turn-off: Storage time	t_s	typ.	1,1	–	μs
		<	1,4	–	μs
Fall time	t_f	typ.	80	–	ns
		<	150	–	ns
I_{Con} = 3 A; I_B = 0,6 A; T_j = 100 °C					
Turn-off: Storage time	t_s	typ.	1,2	–	μs
		<	1,5	–	μs
Fall time	t_f	typ.	140	–	ns
		<	300	–	ns
Switching times inductive load (Figs 6 and 7)					
I_{Con} = 2,5 A; I_B = 0,5 A					
Turn-off: Storage time	t_s	typ.	–	1,1	μs
		<	–	1,4	μs
Fall time	t_f	typ.	–	80	ns
		<	–	150	ns
I_{Con} = 2,5 A; I_B = 0,5 A; T_j = 100 °C					
Turn-off: Storage time	t_s	typ.	–	1,2	μs
		<	–	1,5	μs
Fall time		typ.	–	140	ns
		<	–	300	ns



V_{CC} = 250 V
V_{IM} = −6 to + 8 V
$\frac{t_p}{T}$ = 0,01
t_p = 20 μs
The values of R_B and R_L are selected in accordance with I_{Con} and I_B requirements.

Fig. 4 Test circuit resistive load.

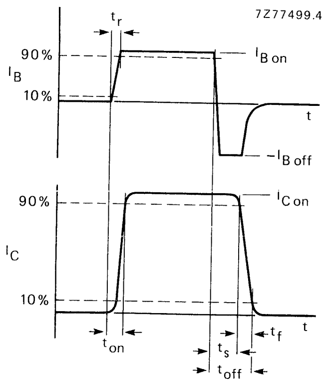


Fig. 5 Switching times waveforms with resistive load.

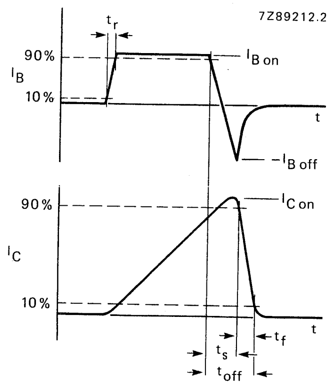
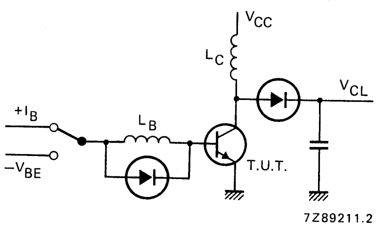


Fig. 6 Switching times waveforms with inductive load.



V_{CL} = 300 V
V_{CC} = 30 V
$-V_{BE}$ = 5 V
L_B = 1 μH
L_C = 200 μH

Fig. 7 Test circuit inductive load.

DEVELOPMENT SAMPLE DATA

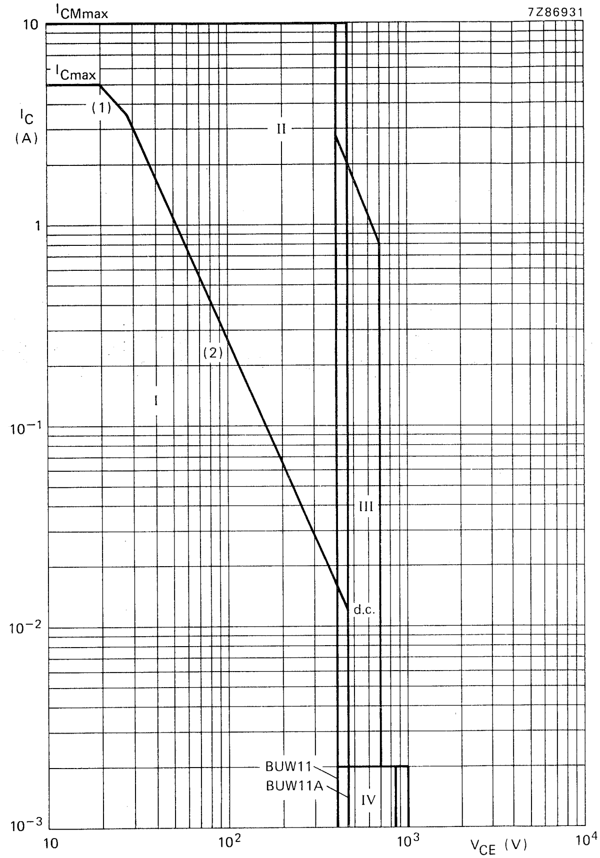


Fig. 8 Safe Operating ARea at $T_{mb} \leqslant 25\ ^oC$.

(1) $P_{tot\ max}$ line.
(2) Second-breakdown limits (independent of temperature).

I   Region of permissible d.c. operation
II Permissible extension for repetitive pulse operation
III Area of permissible operation during turn-on in single transistor converters, provided $R_{BE} \leqslant 100\ \Omega$ and $t_p \leqslant 0{,}6\ \mu s$.
IV Repetitive pulse operation in this region is permissible provided $V_{BE} \leqslant 0$ and $t_p \leqslant 5$ ms.

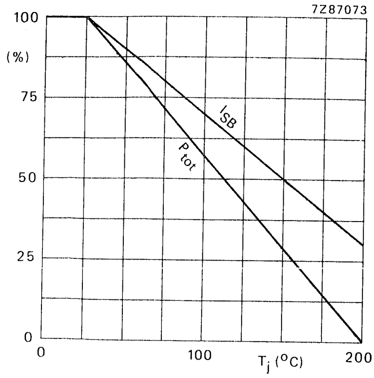


Fig. 9 Total power dissipation and second-breakdown current derating curve.

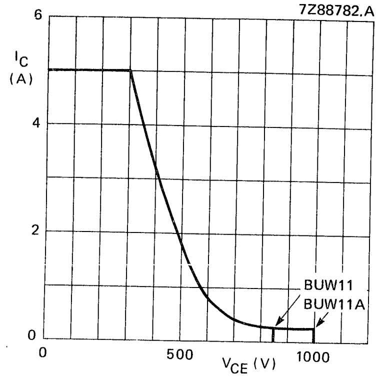


Fig. 10 Reverse bias SOAR.

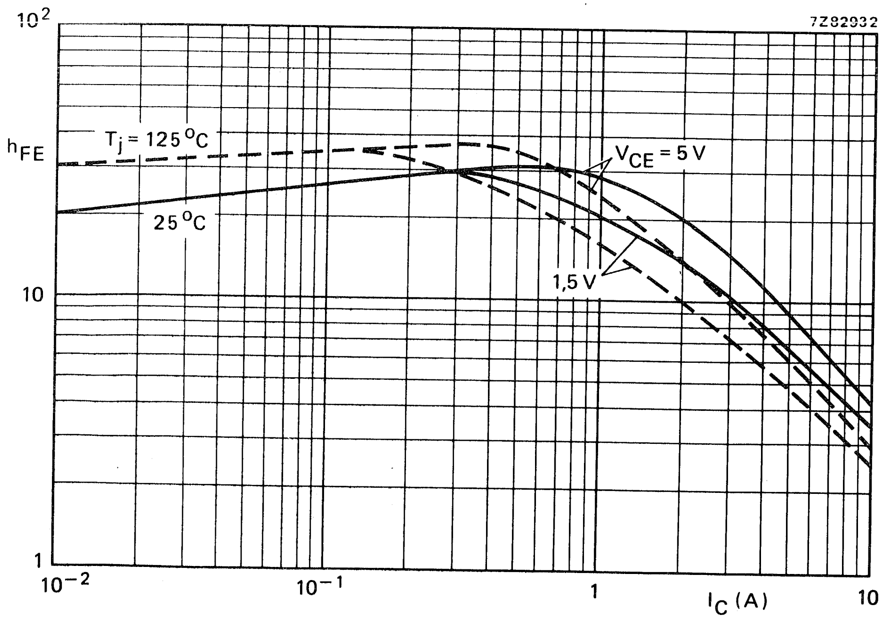


Fig. 11 Typical values d.c. current gain.

DEVELOPMENT SAMPLE DATA

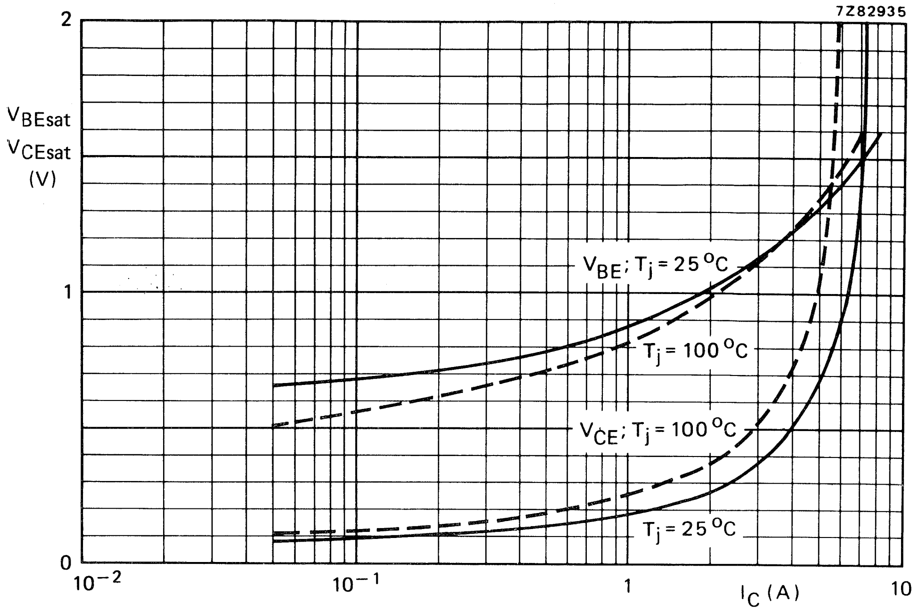


Fig. 12 Typical values base-emitter and collector-emitter voltage, $I_C/I_B = 5$.

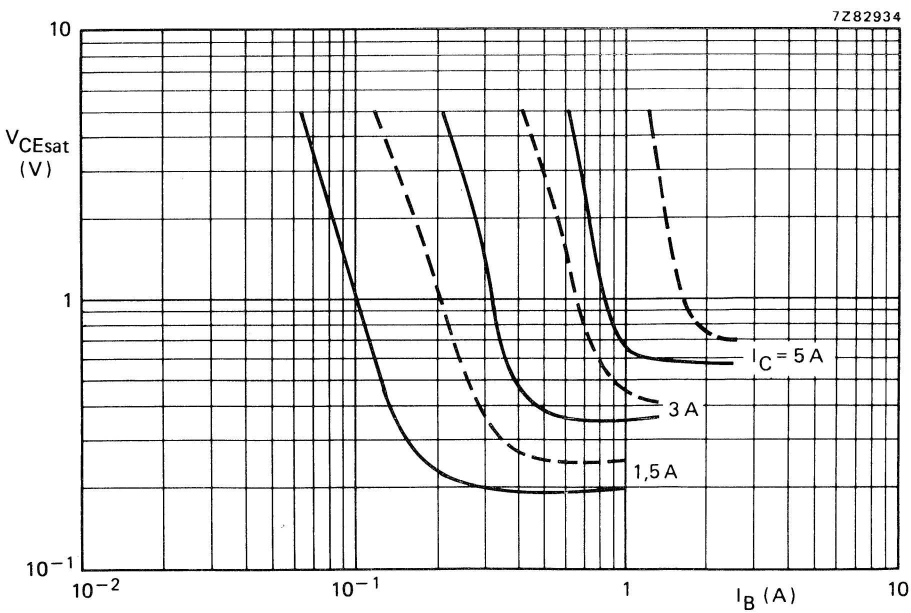


Fig. 13 Typ. (——) and max. (– – –) values collector-emitter saturation voltage at T_j = 25 °C.

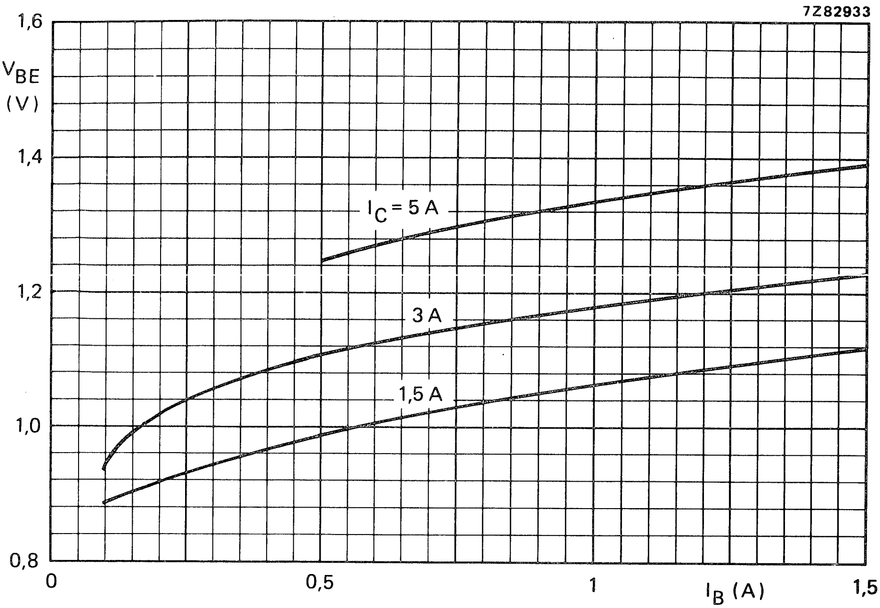


Fig. 14 Typical values at T_j = 25 °C.

APPLICATION INFORMATION

Important design factors of SMPS circuits are the maximum power losses, heatsink requirements and base drive conditions of the switching transistor. The power losses are very dependent on the operating frequency, the maximum collector current amplitude and shape.

The operating frequency is mostly set between 15 and 50 kHz. The collector current shape varies from rectangular in a forward converter to sawtooth in a flyback converter.

Information on nominal base drive, optimum base inductance and maximum transistor dissipation applied in a forward converter is given in Figs 15, 16 and 17. In these figures I_{CM} represents the maximum repetitive peak collector current, which occurs during overload. The information is derived from limit-case transistors at a mounting base temperature of 100 ^oC under the following conditions (see also Fig. 15):

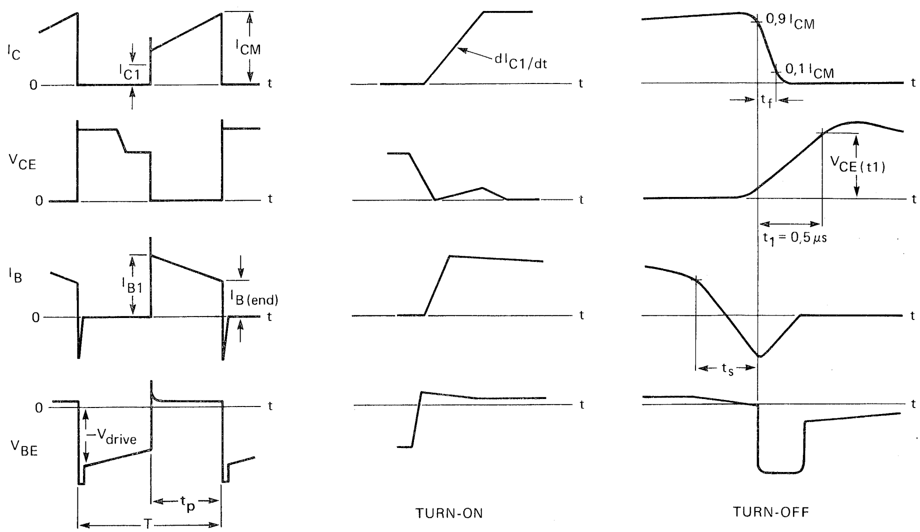
– collector current shape I_{C1}/I_{CM} = 0,9
– duty factor t_p/T = 0,45
– rate of rise of I_C during turn-on = 4 A/µs
– rate of rise of V_{CE} during turn-off = 1 kV/µs
– reverse drive voltage during turn-off = 5 V
– base current shape I_{B1}/I_{Be} = 1,5

The required thermal resistance of the heatsink can be calculated from

$$R_{th\ mb\text{-}a} < \frac{100 - T_{amb}}{P_{tot}}\ \text{K/W}$$

To ensure thermal stability the value of the ambient temperature $T_{amb} > 40\ ^oC$.

DEVELOPMENT SAMPLE DATA



7Z88781

Fig. 15 Relevant waveforms of the switching transistor in a forward SMPS.

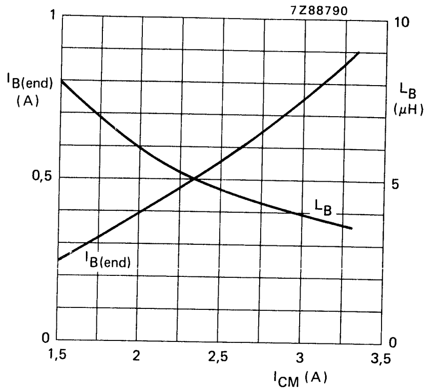


Fig. 16 Recommended nominal "end" value of the base current (I_{Be}) and optimum base inductance (L_B) at $-V_{drive}$ = 5 V versus maximum peak collector current. $dI_{B(end)} = \pm 20\%$.

For other values of $-V_{drive}$ (3 V to 7 V) the related L_B is:

$$L_{Bnom} \frac{(-V_{drive}) + 1}{6}$$

L_{Bnom} is the value given in this graph.

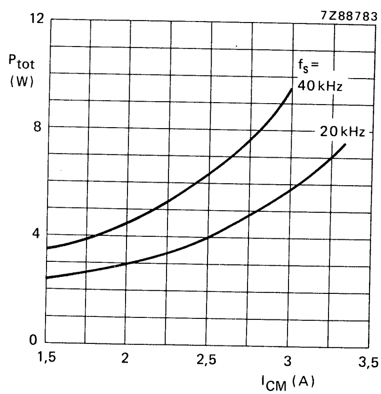


Fig. 17 Maximum transistor dissipation under worse-case operating condition versus maximum peak collector current. T_{mb} = 100 °C; $dI_{B(end)} = \pm 20\%$.

SILICON DIFFUSED POWER TRANSISTORS

High-voltage, high-speed, glass-passivated n-p-n power transistors in a SOT-93 envelope, intended for use in converters, inverters, switching regulators, motor control systems etc.

QUICK REFERENCE DATA

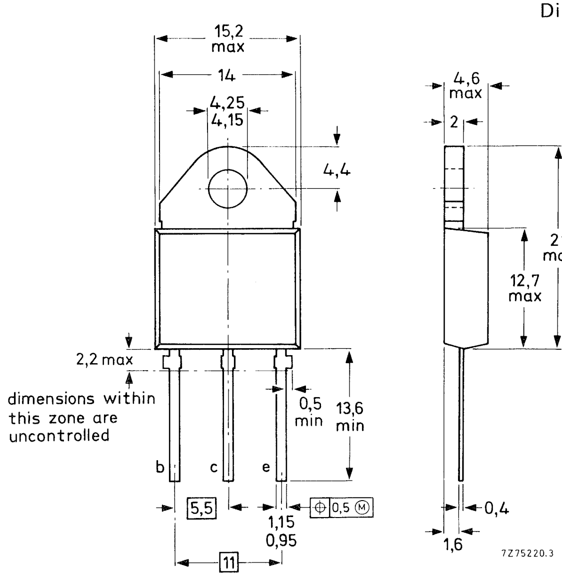
			BUW12	BUW12A	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	8	8	A
Collector current (peak value) $t_p \leqslant 2$ ms	I_{CM}	max.	20	20	A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	125	125	W
Collector-emitter saturation voltage					
I_C = 6 A; I_B = 1,2 A	V_{CEsat}	<	1,5	–	V
I_C = 5 A; I_B = 1 A	V_{CEsat}	<	–	1,5	V
Fall time (resistive load)					
I_{Con} = 6 A; I_{Bon} = $-I_{Boff}$ = 1,2 A	t_f	<	0,8	–	μs
I_{Con} = 5 A; I_{Bon} = $-I_{Boff}$ = 1 A	t_f	<	–	0,8	μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-93.

Collector connected to mounting base.



* See also chapters Mounting instructions and Accessories.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BUW12	BUW12A	
Collector-emitter voltage (peak value; $V_{BE} = 0$)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	8		A
Collector current (peak value); $t_p < 2$ ms	I_{CM}	max.	20		A
Base current (d.c.)	I_B	max.	4		A
Base current (peak value); $t_p \leq 2$ ms	I_{BM}	max.	6		A
Total power dissipation up to $T_{mb} = 25\ ^oC$	P_{tot}	max.	125		W
Storage temperature	T_{stg}		−65 to + 150		^oC
Junction temperature	T_j	max.	150		^oC

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1,0	K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Collector cut-off current*				
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$	I_{CES}	<	1	mA
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$; $T_j = 125\ ^oC$	I_{CES}	<	3	mA
Emitter cut-off current				
$I_C = 0$; $V_{EB} = 9$ V	I_{EBO}	<	10	mA

			BUW12	BUW12A	
Saturation voltages					
$I_C = 6$ A; $I_B = 1,2$ A	V_{CEsat}	<	1,5	–	V
	V_{BEsat}	<	1,5	–	V
$I_C = 5$ A; $I_B = 1,0$ A	V_{CEsat}	<	–	1,5	V
	V_{BEsat}	<	–	1,5	V
Collector-emitter sustaining voltage					
$I_C = 100$ mA; $I_{Boff} = 0$; $L = 25$ mH	$V_{CEOsust}$	>	400	450	V

* Measured with a half sine-wave voltage (curve tracer).

CHARACTERISTICS (continued)

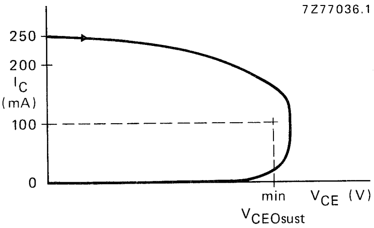


Fig. 2 Oscilloscope display for sustaining voltage.

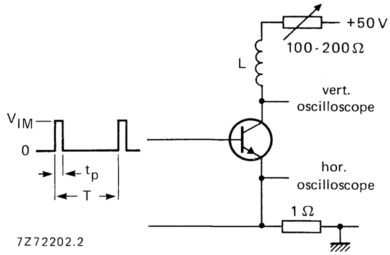
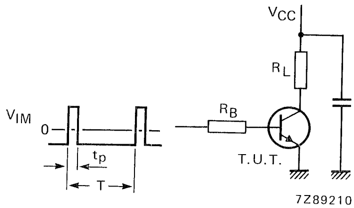


Fig. 3 Test circuit for $V_{CEOsust}$.

DEVELOPMENT SAMPLE DATA

			BUW12	BUW12A	
Switching times resistive load (Figs 4 and 5)					
I_{Con} = 6 A; I_{Bon} = $-I_{Boff}$ = 1,2 A					
Turn-on time	t_{on}	<	1	–	µs
Turn-off: Storage time	t_s	<	4	–	µs
Fall time	t_f	<	0,8	–	µs
I_{Con} = 5 A; I_{Bon} = $-I_{Boff}$ = 1 A					
Turn-on time	t_{on}	<	–	1	µs
Turn-off: Storage time	t_s	<	–	4	µs
Fall time	t_f	<	–	0,8	µs
Switching times inductive load (Figs 6 and 7)					
I_{Con} = 6 A; I_B = 1,2 A					
Turn-off: Storage time	t_s	typ.	1,6	–	µs
		<	2,1	–	µs
Fall time	t_f	typ.	80	–	ns
		<	150	–	ns
I_{Con} = 6 A; I_B = 1,2 A; T_j = 100 °C					
Turn-off: Storage time	t_s	typ.	1,8	–	µs
		<	2,3	–	µs
Fall time	t_f	typ.	140	–	ns
		<	300	–	ns
Switching times inductive load (Figs 6 and 7)					
I_{Con} = 5 A; I_B = 1 A					
Turn-off: Storage time	t_s	typ.	–	1,6	µs
		<	–	2,1	µs
Fall time	t_f	typ.	–	80	ns
		<	–	150	ns
I_{Con} = 5 A; I_B = 1 A; T_j = 100 °C					
Turn-off: Storage time	t_s	typ.	–	1,8	µs
		<	–	2,3	µs
Fall time	t_f	typ.	–	140	ns
		<	–	300	ns



V_{CC} = 250 V
V_{IM} = −6 to + 8 V
$\frac{t_p}{T}$ = 0,01
t_p = 20 μs
The values of R_B and R_L are selected in accordance with I_{Con} and I_B requirements.

Fig. 4 Test circuit resistive load.

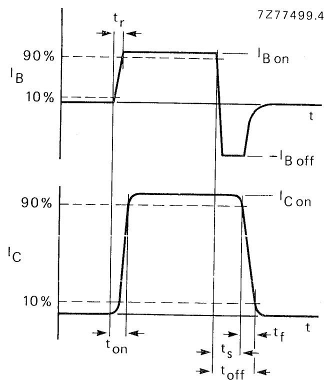


Fig. 5 Switching times waveforms. with resistive load.

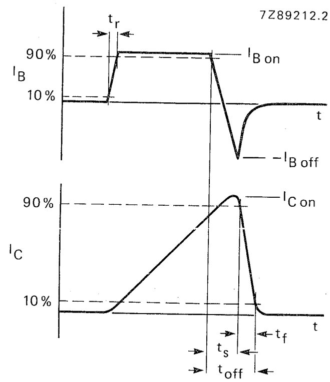
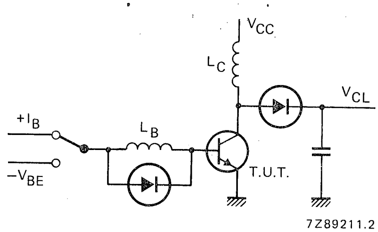


Fig. 6 Switching times waveforms with inductive load.



V_{CL} = 300 V
V_{CC} = 30 V
$-V_{BE}$ = 5 V
L_B = 1 μH
L_C = 200 μH

Fig. 7 Test circuit inductive load.

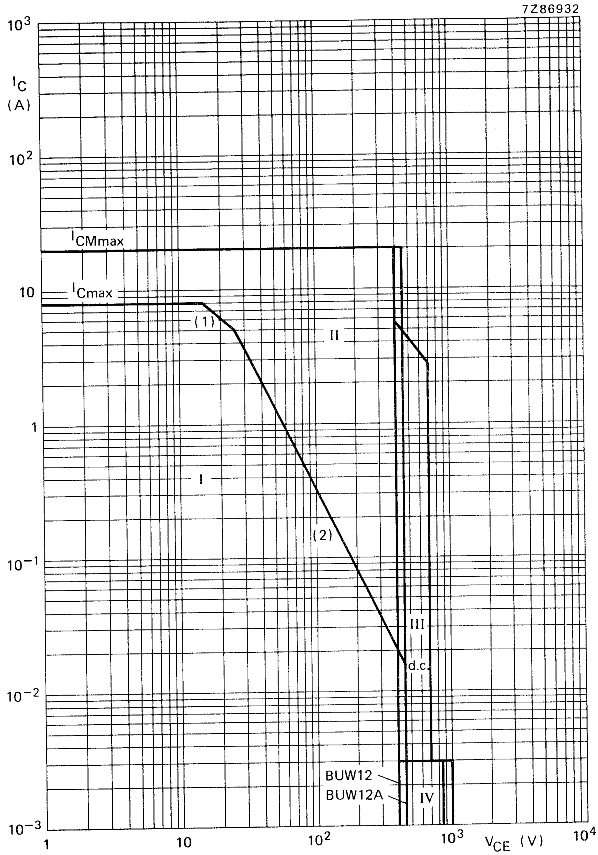


Fig. 8 Safe Operating ARea at $T_{mb} \leq 25\ ^oC$.

(1) $P_{tot\ max}$ line.
(2) Second-breakdown limits (independent of temperature).

I Region of permissible d.c. operation.
II Permissible extension for repetitive pulse operation.
III Area of permissible operation during turn-on in single transistor converters, provided $R_{BE} \leq 100\ \Omega$ and $t_p \leq 0{,}6\ \mu s$.
IV Repetitive pulse operation in this region is permissible provided $V_{BE} \leq 0$ and $t_p \leq 2$ ms.

DEVELOPMENT SAMPLE DATA

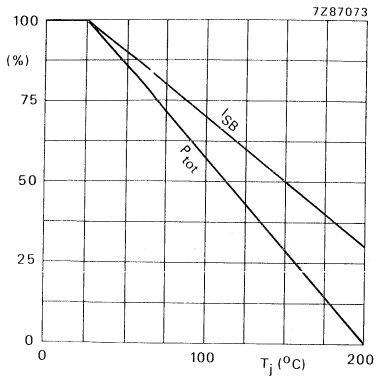


Fig. 9 Total power dissipation and second-breakdown current derating curve.

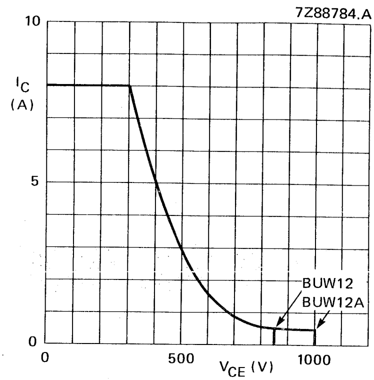


Fig. 10 Reverse bias SOAR.

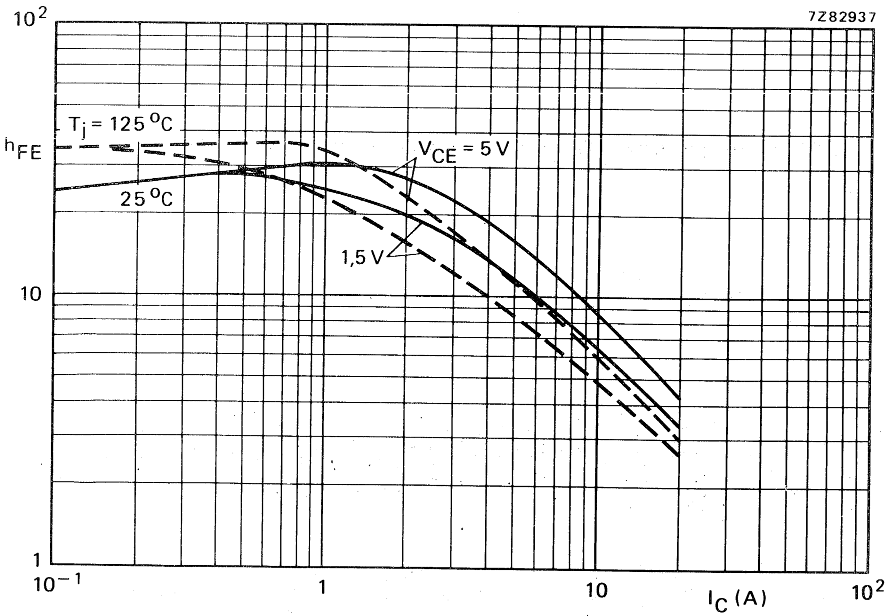


Fig. 11 Typical values d.c. current gain.

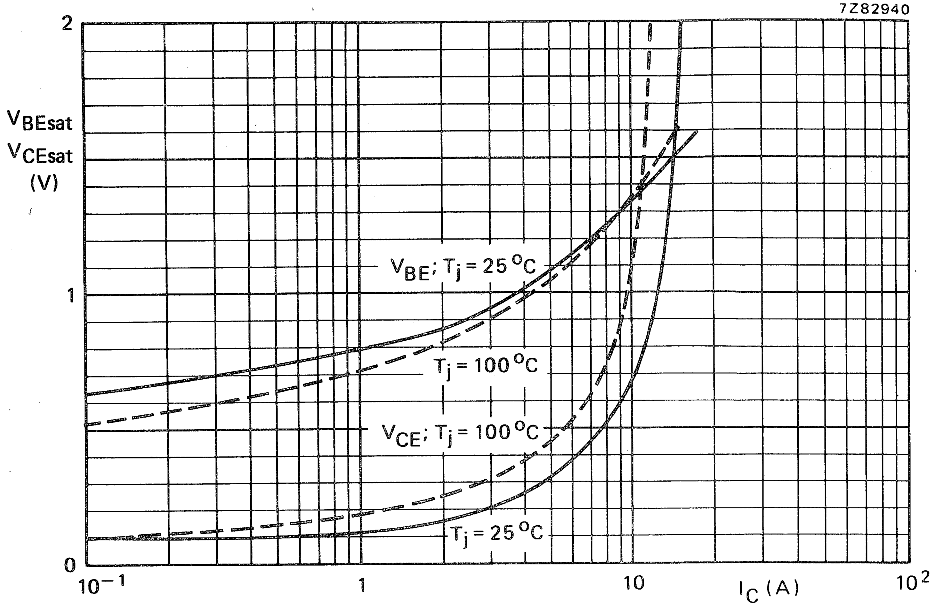


Fig. 12 Typical values base and collector voltage at $I_C/I_B = 5$.

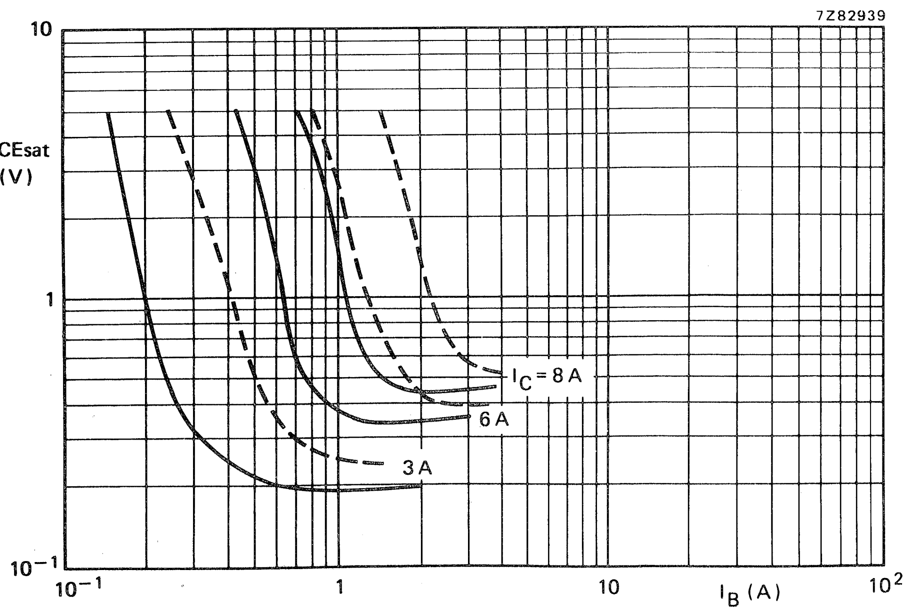


Fig. 13 Typ. (——) and max. (– – –) values collector-emitter saturation voltage at T_j = 25 °C.

DEVELOPMENT SAMPLE DATA

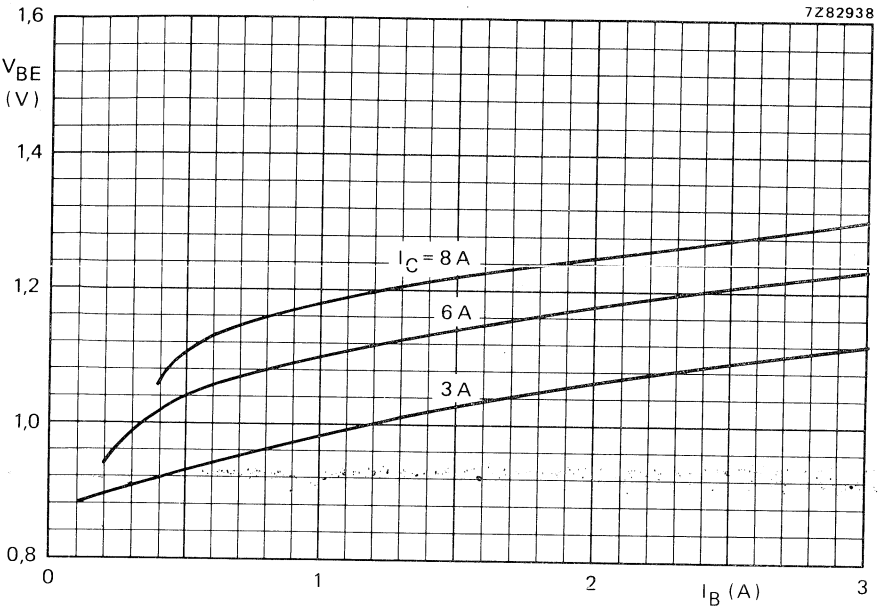


Fig. 14 Typical values base-emitter voltage at T_j = 25 ^oC.

APPLICATION INFORMATION

Important design factors of SMPS circuits are the maximum power losses, heatsink requirements and base drive conditions of the switching transistor. The power losses are very dependent on the operating frequency, the maximum collector current amplitude and shape.

The operating frequency is mostly set between 15 and 50 kHz. The collector current shape varies from rectangular in a forward converter to sawtooth in a flyback converter.

Information on nominal base drive, optimum base inductance and maximum transistor dissipation applied in a forward converter is given in Figs 15, 16 and 17. In these figures I_{CM} represents the maximum repetitive peak collector current, which occurs during overload. The information is derived from limit-case transistors at a mounting base temperature of 100 °C under the following conditions (see also Fig. 15):

- collector current shape I_{C1}/I_{CM} = 0,9
- duty factor t_p/T = 0,45
- rate of rise of I_C during turn-on = 8 A/μs
- rate of rise of V_{CE} during turn-off = 1 kV/μs
- reverse drive voltage during turn-off = 5 V
- base current shape I_{B1}/I_{Be} = 1,5

The required thermal resistance of the heatsink can be calculated from

$$R_{th\ mb\text{-}a} < \frac{100 - T_{amb}}{P_{tot}}\ \text{K/W}.$$

To ensure thermal stability the value of the ambient temperature $T_{amb} > 40$ °C.

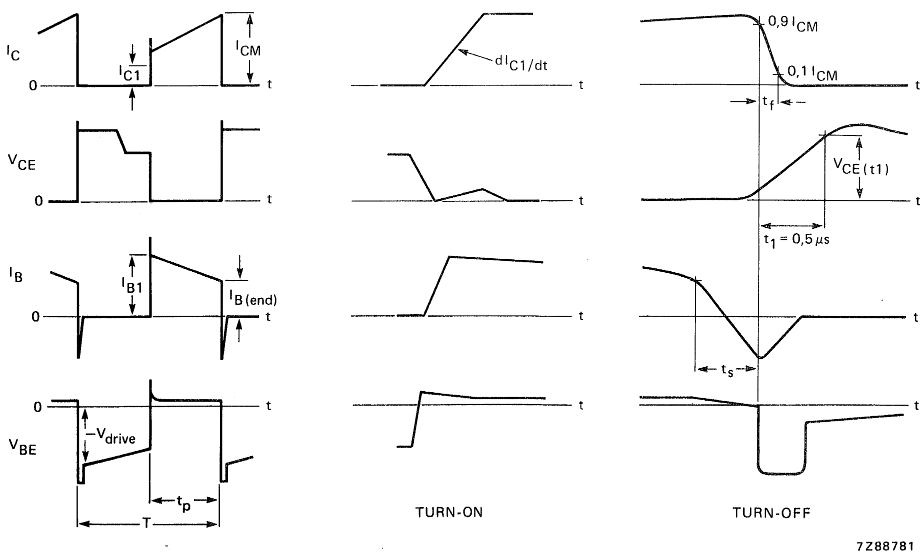


Fig. 15 Relevant waveforms of the switching transistor in a forward SMPS.

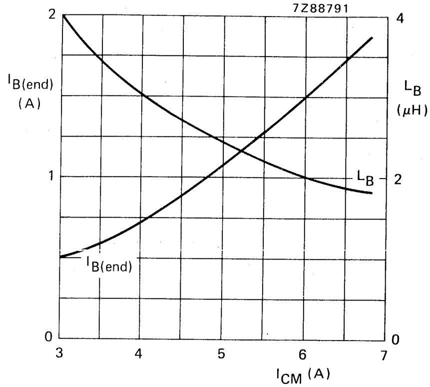


Fig. 16 Recommended nominal "end" value of the base current (I_{Be}) and optimum base inductance (L_B) at $-V_{drive} = 5$ V versus maximum peak collector current. $dI_{B(end)} = \pm 20\%$.

For other values of $-V_{drive}$ (3 V to 7 V) the related L_B is:

$$L_{Bnom} \frac{(-V_{drive}) + 1}{6}$$

L_{Bnom} is the value given in this graph.

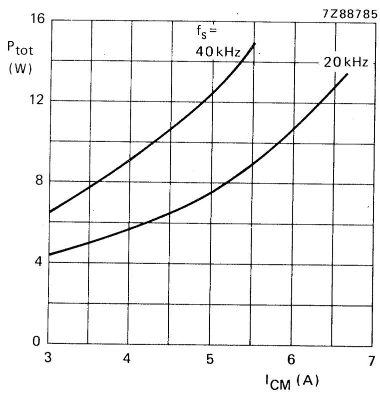


Fig. 17 Maximum transistor dissipation under worse-case operating condition versus maximum peak collector current. $T_{mb} = 100$ °C; $dI_{B(end)} = \pm 20\%$.

SILICON DIFFUSED POWER TRANSISTORS

High-voltage, high-speed, glass-passivated n-p-n power transistors in a SOT-93 envelope, intended for use in converters, inverters, switching regulators, motor control systems etc.

QUICK REFERENCE DATA

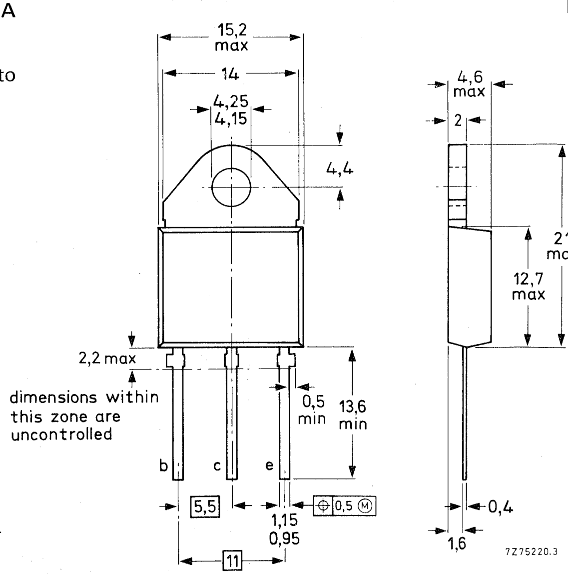
			BUW13	BUW13A	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	15		A
Collector current (peak value) $t_p < 2$ ms	I_{CM}	max.	30		A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	175		W
Collector-emitter saturation voltage					
I_C = 10 A; I_B = 2 A	V_{CEsat}	<	1,5	–	V
I_C = 8 A; I_B = 1,6 A	V_{CEsat}	<	–	1,5	V
Fall time					
I_{Con} = 10 A; I_{Bon} = $-I_{Boff}$ = 2 A	t_f	<	0,8	–	µs
I_{Con} = 8 A; I_{Bon} = $-I_{Boff}$ = 1,6 A	t_f	<	–	0,8	µs

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-93.

Collector connected to mounting base



See also chapters Mounting instructions and Accessories.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BUW13	BUW13A	
Collector-emitter voltage (peak value, $V_{BE} = 0$)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	15		A
Collector current (peak value); $t_p < 2$ ms	I_{CM}	max.	30		A
Base current (d.c.)	I_B	max.	6		A
Base current (peak value); $t_p < 2$ ms	I_{BM}	max.	9		A
Total power dissipation up to $T_{mb} = 25\ ^oC$	P_{tot}	max.	175		W
Storage temperature	T_{stg}		−65 to + 150		^oC
Junction temperature	T_j	max.	150		^oC

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	0,7	K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Collector cut-off current*				
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$	I_{CES}	<	1	mA
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$; $T_j = 125\ ^oC$	I_{CES}	<	4	mA
Emitter cut-off current	I_{EBO}	<	10	mA

			BUW13	BUW13A	
Saturation voltages					
$I_C = 10$ A; $I_B = 2$ A	V_{CEsat}	<	1,5	–	V
	V_{BEsat}	<	1,6	–	V
$I_C = 8$ A; $I_B = 1,6$ A	V_{CEsat}	<	–	1,5	V
	V_{BEsat}	<	–	1,6	V
Collector-emitter sustaining voltage					
$I_C = 100$ mA; $I_{Boff} = 0$; $L = 25$ mH	$V_{CEOsust}$	>	400	450	V

* Measured with a half sine-wave voltage (curve tracer).

CHARACTERISTICS (continued)

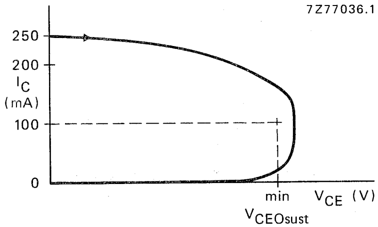


Fig. 2 Oscilloscope display for sustaining voltage.

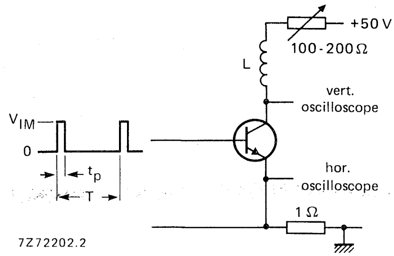
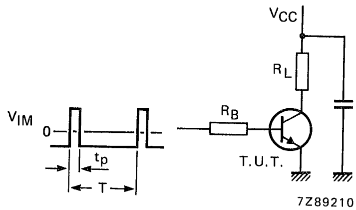


Fig. 3 Test circuit for $V_{CEOsust}$.

DEVELOPMENT SAMPLE DATA

			BUW13	BUW13A	
Switching times resistive load (Figs 4 and 5)					
I_{Con} = 10 A; I_{Bon} = $-I_{Boff}$ = 2 A					
Turn-on time	t_{on}	<	1	–	µs
Turn-off: Storage time	t_s	<	4	–	µs
Fall time	t_f	<	0,8	–	µs
I_{Con} = 8 A; I_{Bon} = $-I_{Boff}$ = 1,6 A					
Turn-on time	t_{on}	<	–	1	µs
Turn-off: Storage time	t_s	<	–	4	µs
Fall time	t_f	<	–	0,8	µs
Switching times inductive load (Figs 6 and 7)					
I_{Con} = 10 A; I_B = 2 A					
Turn-off: Storage time	t_s	typ.	2,3	–	µs
		<	3,0	–	µs
Fall time	t_f	typ.	80	–	ns
		<	150	–	ns
I_{Con} = 10 A; I_B = 2 A; T_j = 100 °C					
Turn-off: Storage time	t_s	typ.	2,5	–	µs
		<	3,2	–	µs
Fall time	t_f	typ.	140	–	ns
		<	300	–	ns
Switching times inductive load (Figs 6 and 7)					
I_{Con} = 8 A; I_B = 1,6 A					
Turn-off: Storage time	t_s	typ.	–	2,3	µs
		<	–	3,0	µs
Fall time	t_f	typ.	–	80	ns
		<	–	150	ns
I_{Con} = 8 A; I_B = 1,6 A; T_j = 100 °C					
Turn-off: Storage time	t_s	typ.	–	2,5	µs
		<	–	3,2	µs
Fall time	t_f	typ.	–	140	ns
		<	–	300	ns



$V_{CC} = 250$ V
$V_{IM} = -6$ to $+8$ V
$t_p = 20$ μs
$\frac{t_p}{T} = 0{,}01$

The values of R_B and R_L are selected in accordance with I_{Con} and I_B requirements.

Fig. 4 Test circuit resistive load.

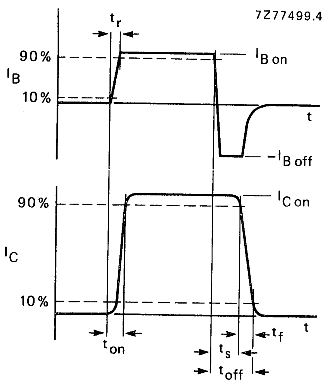


Fig. 5 Switching times waveforms with resistive load.

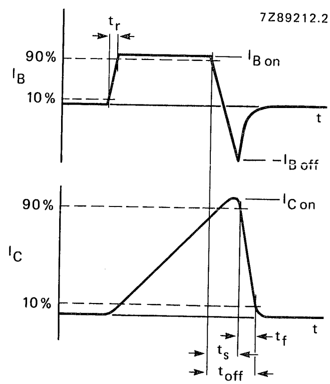
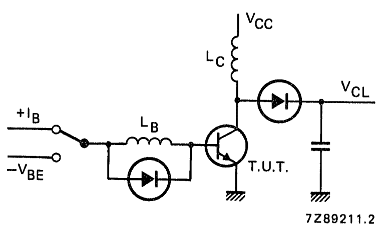


Fig. 6 Switching times waveforms with inductive load.



$V_{CL} = 300$ V
$V_{CC} = 30$ V
$-V_{BE} = 5$ V
$L_B = 1$ μH
$L_C = 200$ μH

Fig. 7 Test circuit inductive load.

DEVELOPMENT SAMPLE DATA

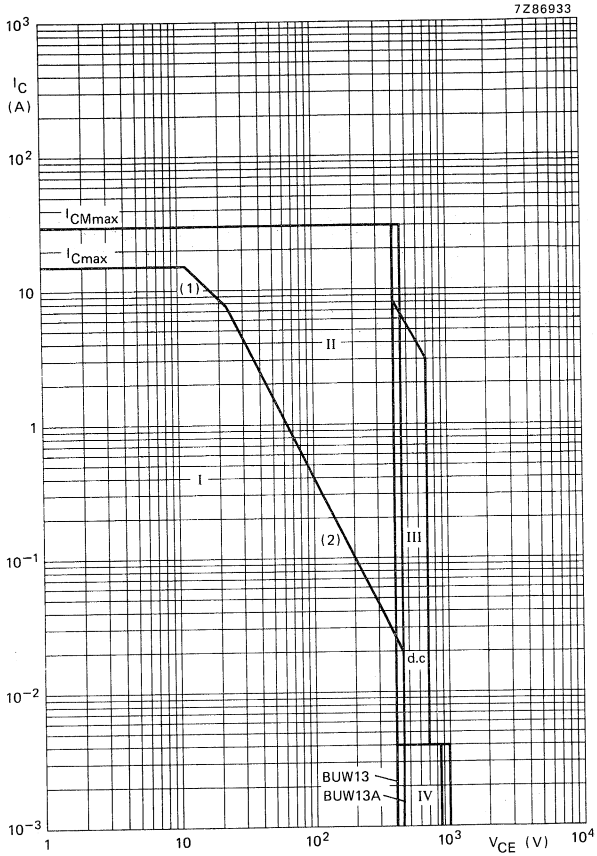


Fig. 8 Safe Operating ARea at $T_{mb} \leqslant 25\ ^oC$.

(1) $P_{tot\ max}$ line.

(2) Second-breakdown limits (independent of temperature).

I Region of permissible d.c. operation.

II Permissible extension for repetitive pulse operation.

III Area of permissible operation during turn-on in single transistor converters, provided $R_{BE} \leqslant 100\ \Omega$ and $t_p \leqslant 0{,}6\ \mu s$.

IV Repetitive pulse operation in this region is permissible provided $V_{BE} \leqslant 0$ and $t_p \leqslant 5$ ms.

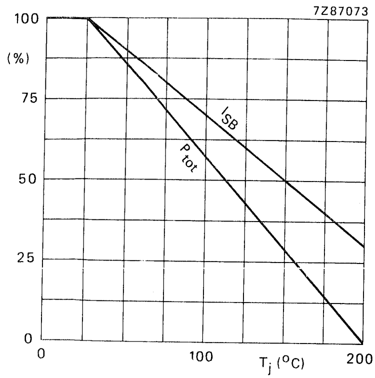


Fig. 9 Total power dissipation and second-breakdown current derating curve.

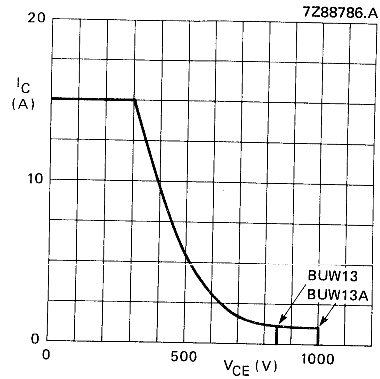


Fig. 10 Reverse bias SOAR.

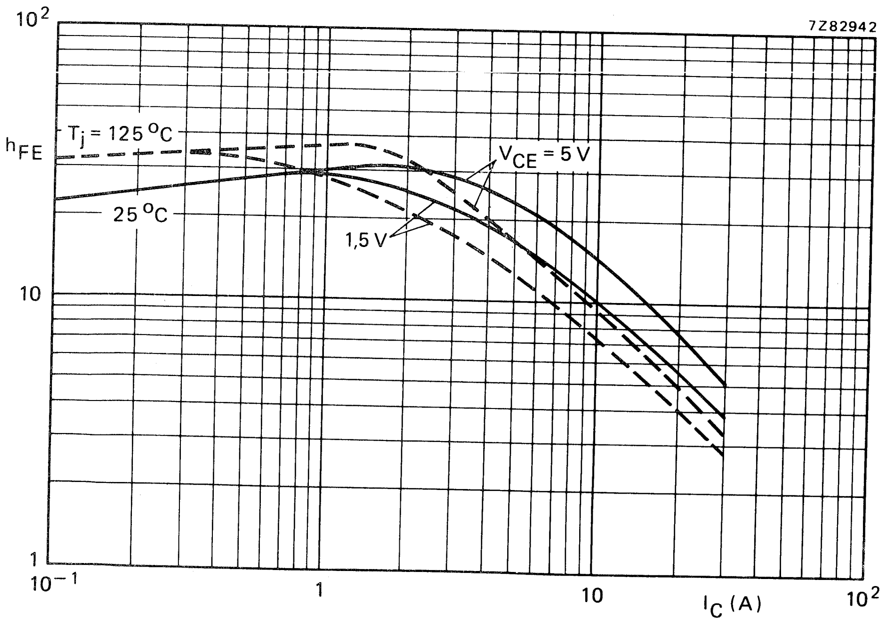


Fig. 11 Typical values d.c. current gain.

DEVELOPMENT SAMPLE DATA

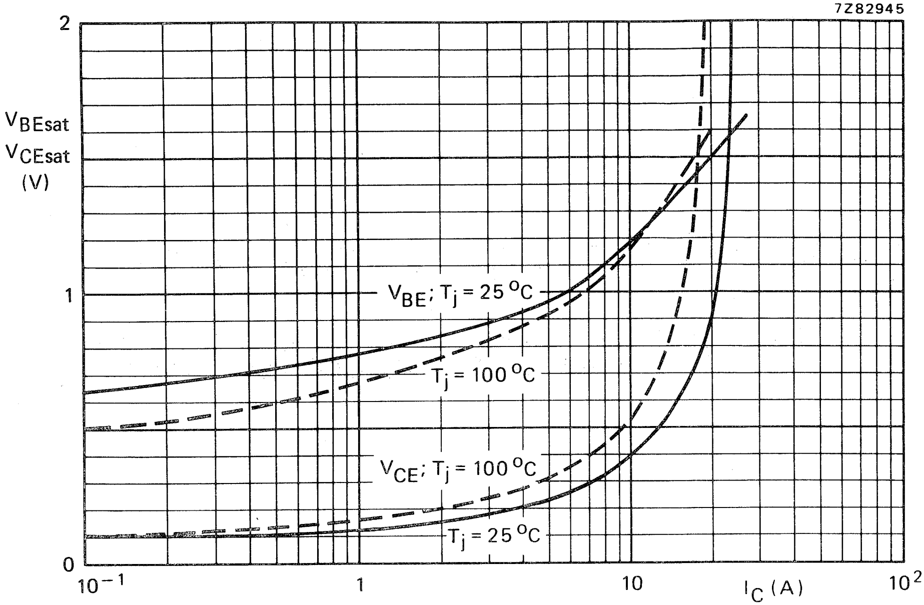


Fig. 12 Typical values base and collector voltage at $I_C/I_B = 5$.

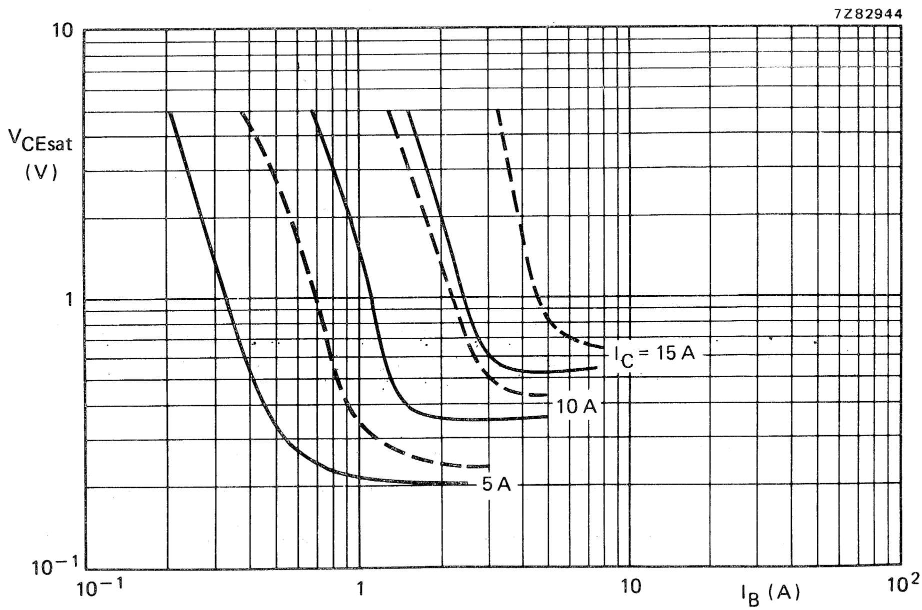


Fig. 13 Typical (——) and maximum (– – –) values saturation voltage. T_j = 25 °C.

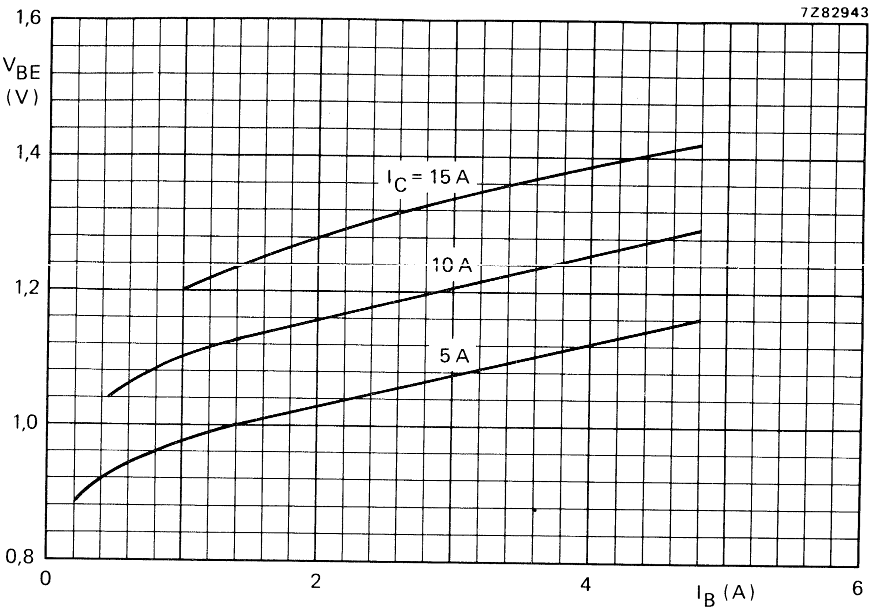


Fig. 14 Typical values base-emitter voltage at T_j = 25 °C.

APPLICATION INFORMATION

Important design factors of SMPS circuits are the maximum power losses, heatsink requirements and base drive conditions of the switching transistor. The power losses are very dependent on the operating frequency, the maximum collector current amplitude and shape.

The operating frequency is mostly set between 15 and 50 kHz. The collector current shape varies from rectangular in a forward converter to sawtooth in a flyback converter.

Information on nominal base drive, optimum base inductance and maximum transistor dissipation applied in a forward converter is given in Figs 15, 16 and 17. In these figures I_{CM} represents the maximum repetitive peak collector current, which occurs during overload. The information is derived from limit-case transistors at a mounting base temperature of 100 °C under the following conditions (see also Fig. 15):

- collector current shape $I_{C1}/I_{CM} = 0,9$
- duty factor $t_p/T = 0,45$
- rate of rise of I_C during turn-on = 10 A/μs
- rate of rise of V_{CE} during turn-off = 1 kV/μs
- reverse drive voltage during turn-off = 5 V
- base current shape $I_{B1}/I_{Be} = 1,5$

The required thermal resistance of the heatsink can be calculated from

$$R_{th\ mb\text{-}a} < \frac{100 - T_{amb}}{P_{tot}}\ \text{K/W}$$

To ensure thermal stability the value of the ambient temperature $T_{amb} > 40$ °C.

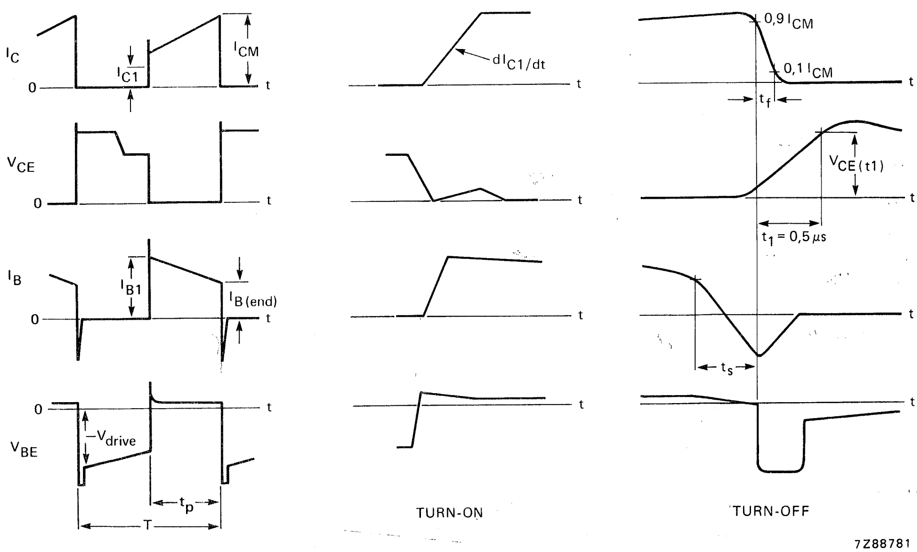


Fig. 15 Relevant waveforms of the switching transistor in a forward SMPS.

DEVELOPMENT SAMPLE DATA

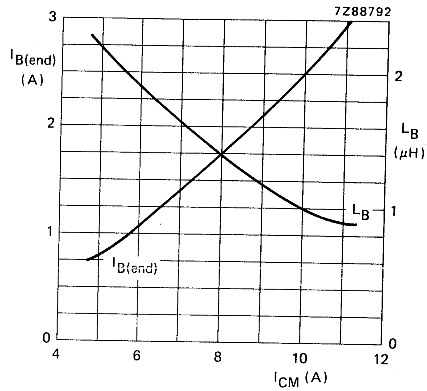


Fig. 16 Recommended nominal "end" value of the base current (I_{Be}) and optimum base inductance (L_B) at $-V_{drive}$ = 5 V versus maximum peak collector current. $dI_{B(end)}$ = ± 20%.

For other values of $-V_{drive}$ (3 V to 7 V) the related L_B is:

$$L_{Bnom} \frac{(-V_{drive}) + 1}{6}$$

L_{Bnom} is the value given in this graph.

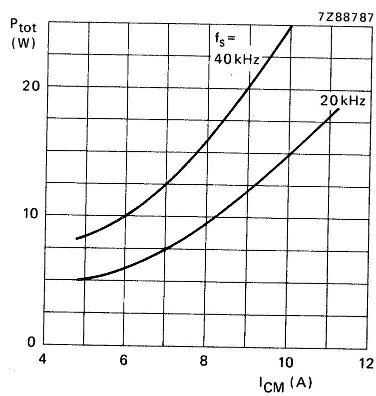


Fig. 17 Maximum transistor dissipation under worse-case operating condition versus maximum peak collector current. T_{mb} = 100 °C; $dI_{B(end)}$ = ± 20%.

SILICON DIFFUSED POWER TRANSISTORS

High-voltage, high-speed, glass-passivated n-p-n power transistors in SOT-82 envelopes, intended for use in converters, inverters, switching regulators, motor control systems and switching applications.

QUICK REFERENCE DATA

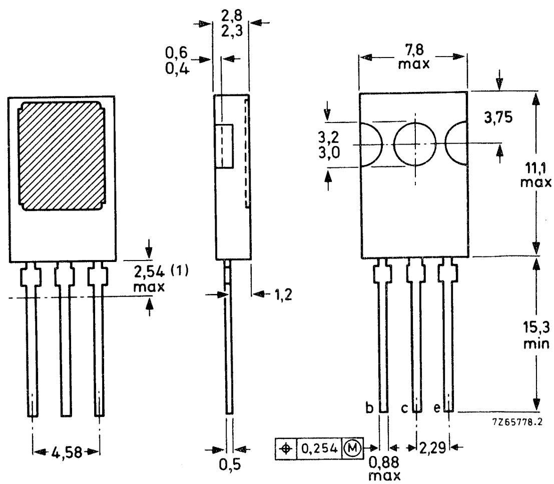
			BUW84	BUW85	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	800	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	2		A
Collector current (peak value) t_p = 2 ms	I_{CM}	max.	3		A
Total power dissipation up to T_{mb} = 45 °C	P_{tot}	max.	50		W
Collector-emitter saturation voltage I_C = 1 A; I_B = 0,2 A	V_{CEsat}	<	1		V
Fall time I_{Con} = 1 A; I_{Bon} = 0,2 A; $-I_{Boff}$ = 0,4 A	t_f	typ.	0,4		μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-82.

Collector connected to mounting base.



(1) Within this region the cross-section of the leads is uncontrolled.

See also chapters Mounting Instructions and Accessories.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BUW84	BUW85	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	800	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
→ Emitter-base voltage (open collector)	V_{EBO}	max.	5	5	V

Collector current (d.c.)	I_C	max.	2	A
Collector current (peak value) t_p = 2 ms	I_{CM}	max.	3	A
Base current (d.c.)	I_B	max.	0,75	A
Base current (peak value)	I_{BM}	max.	1	A
Reverse base current (peak value) *	$-I_{BM}$	max.	1	A
Total power dissipation up to T_{mb} = 45 °C	P_{tot}	max.	50	W
Storage tamperature	T_{stg}		−65 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	2,1	K/W
From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	100	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current **				
$V_{CEM} = V_{CESMmax}$; V_{BE} = 0	I_{CES}	<	200	μA
$V_{CEM} = V_{CESMmax}$; V_{BE} = 0; T_j = 125 °C	I_{CES}	<	1,5	mA
D.C. current gain				
I_C = 0,1 A; V_{CE} = 5 V	h_{FE}	typ.	50	

* Turn-off current.
** Measured with a half sine-wave voltage (curve tracer).

CHARACTERISTICS (continued)

T_j = 25 °C unless otherwise specified

Emitter cut-off current					
I_C = 0; V_{EB} = 5 V	I_{EBO}	<	1		mA
Saturation voltages					
I_C = 0,3 A; I_B = 30 mA	V_{CEsat}	<	0,8		V
I_C = 1 A; I_B = 0,2 A	V_{CEsat}	<	1		V
I_C = 1 A; I_B = 0,2 A	V_{BEsat}	<	1,1		V
Collector-emitter sustaining voltage			BUW84	BUW85	
I_C = 100 mA; I_{Boff} = 0; L = 25 mH	$V_{CEOsust}$	>	400	450	V

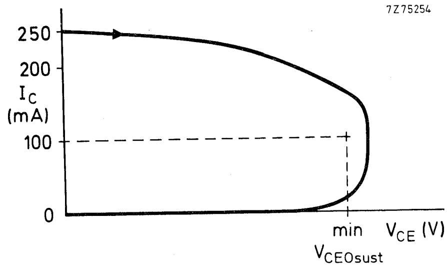


Fig. 2 Oscilloscope display for sustaining voltage.

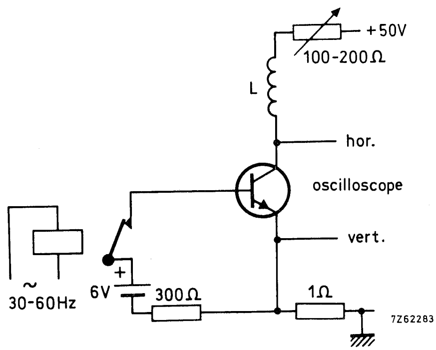


Fig. 3 Test circuit for $V_{CEOsust}$.

CHARACTERISTICS (continued)

T_j = 25 °C unless otherwise specified

Transition frequency at f = 1 MHz; I_C = 0,2 A; V_{CE} = 10 V	f_T	typ.	20 MHz
Switching times: I_{Con} = 1 A; V_{CC} = 250 V; I_{Bon} = 0,2 A; $-I_{Boff}$ = 0,4 A			
Turn-on time	t_{on}	typ.	0,2 µs
		<	0,5 µs
Turn-off: Storage time	t_s	typ.	2 µs
		<	3,5 µs
Fall time	t_f	typ.	0,4 µs
Fall time, T_{mb} = 95 °C	t_f	<	1,4 µs

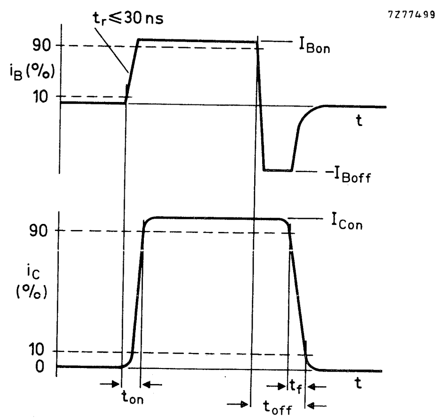


Fig. 4 Waveforms.

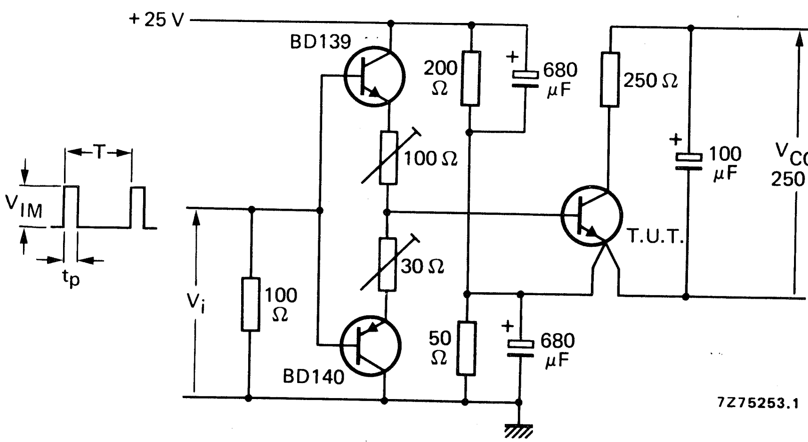


Fig. 5 Test circuit.

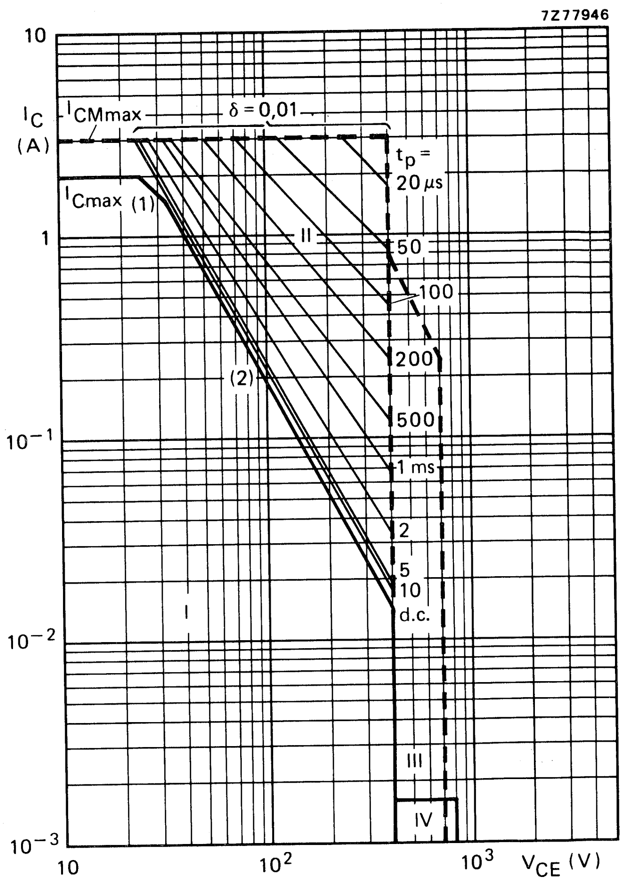


Fig. 6 Safe Operating ARea at $T_{mb} \leqslant 25\ ^oC$ of BUW84.

I Region of permissible d.c. operation
II Permissible extension for repetitive pulse operation
III Area of permissible operation during turn-on in single transistor converters, provided $R_{BE} \leqslant 100\ \Omega$ and $t_p \leqslant 0,6\ \mu s$
IV Repetitive pulse operation in this region is permissible, provided $V_{BE} \leqslant 0$ and $t_p \leqslant 2$ ms

(1) $P_{tot\ max}$ line.
(2) Second-breakdown limits (independent of temperature).

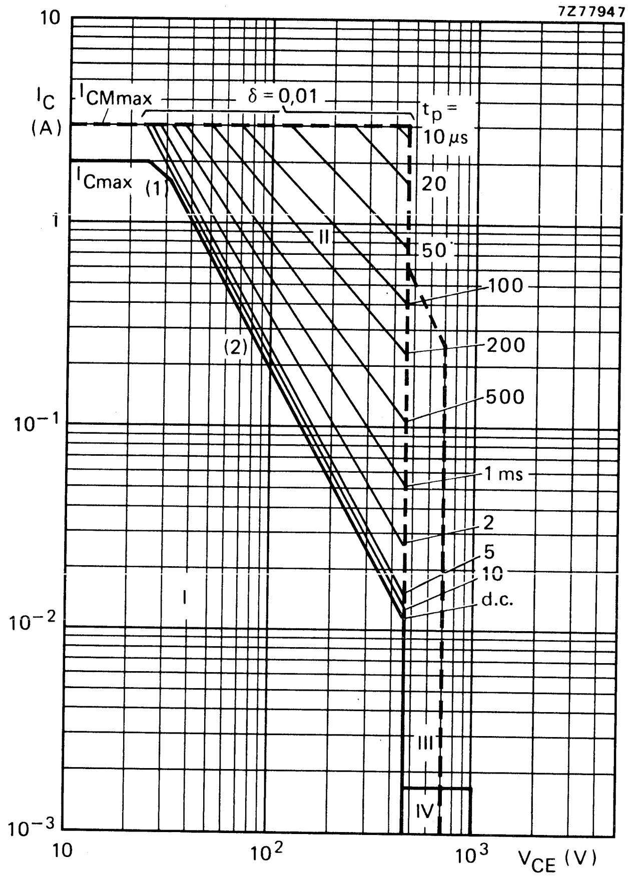


Fig. 7 Safe Operating ARea at $T_{mb} \leqslant 25\ ^oC$ of BUW85.

I Region of permissible d.c. operation

II Permissible extension for repetitive pulse operation

III Area of permissible operation during turn-on in single transistor converters, provided $R_{BE} \leqslant 100\ \Omega$ and $t_p \leqslant 0,6\ \mu s$

IV Repetitive pulse operation in this region is permissible, provided $V_{BE} \leqslant 0$ and $t_p \leqslant 2$ ms

(1) $P_{tot\ max}$ line.

(2) Second-breakdown limits (independent of temperature).

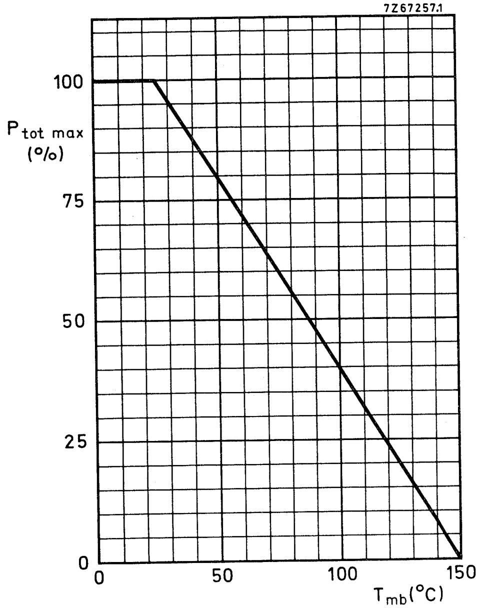

7Z67257.1
100
$P_{tot\ max}$ (%)
75
50
25
0
0
50
100
150
T_{mb} (°C)

Fig. 8.

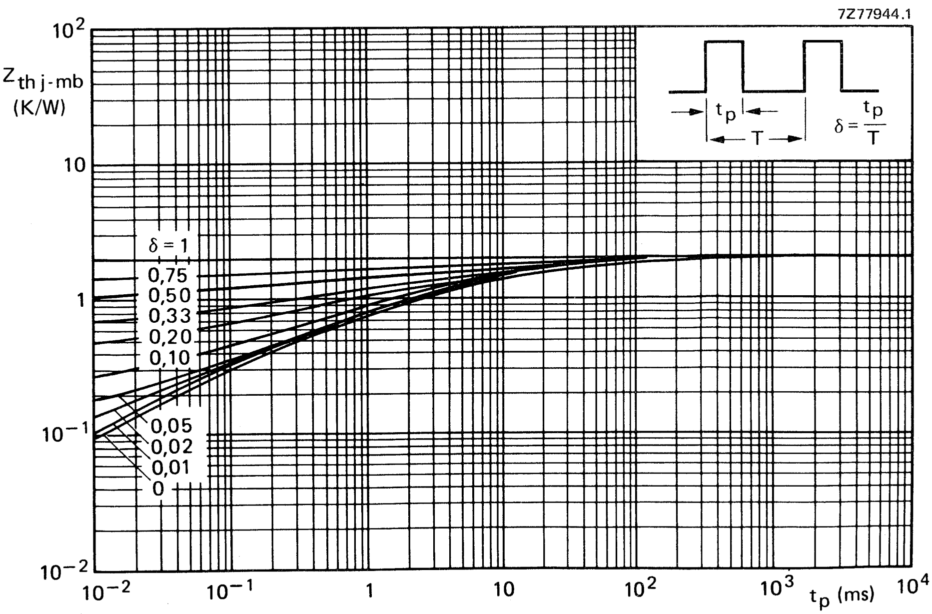

7Z77944.1
10^2
$Z_{th\ j\text{-}mb}$ (K/W)
10
1
10^{-1}
10^{-2}
δ = 1
0,75
0,50
0,33
0,20
0,10
0,05
0,02
0,01
0
t_p
T
$\delta = \frac{t_p}{T}$
10^{-2}
10^{-1}
1
10
10^2
10^3
t_p (ms)
10^4

Fig. 9.

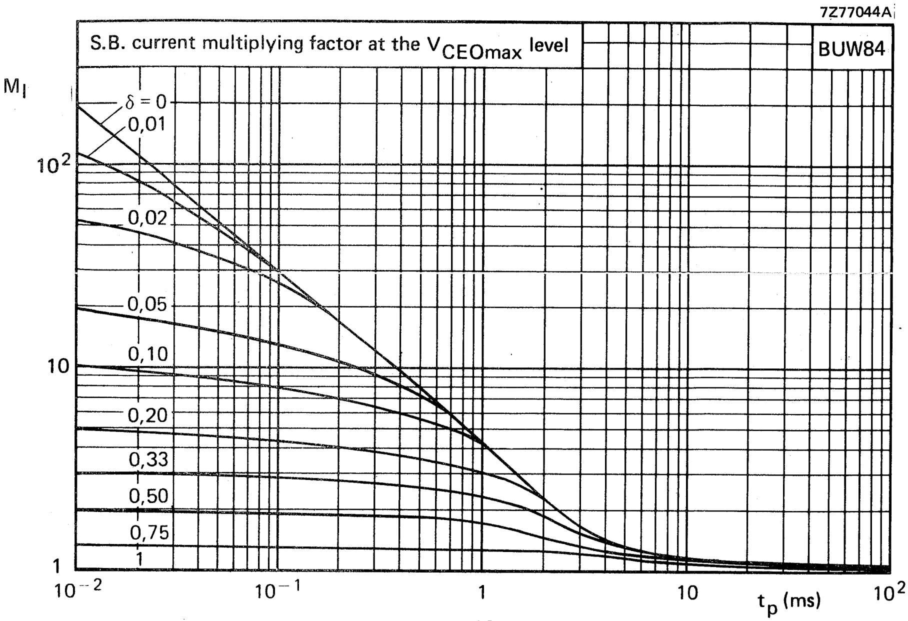

7Z77044A
S.B. current multiplying factor at the V_{CEOmax} level
BUW84
M_I
δ = 0
0,01
0,02
0,05
0,10
0,20
0,33
0,50
0,75
1
10^2
10
1
10^{-2}
10^{-1}
1
10
10^2
t_p (ms)

Fig. 10.

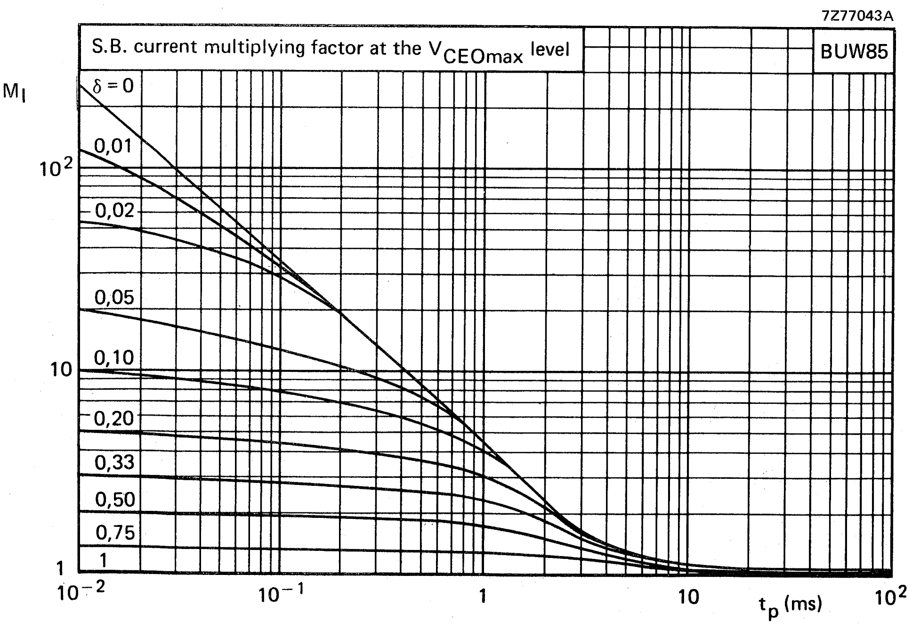

7Z77043A
S.B. current multiplying factor at the V_{CEOmax} level
BUW85
M_I
δ = 0
0,01
0,02
0,05
0,10
0,20
0,33
0,50
0,75
1
10^2
10
1
10^{-2}
10^{-1}
1
10
10^2
t_p (ms)

Fig. 11.

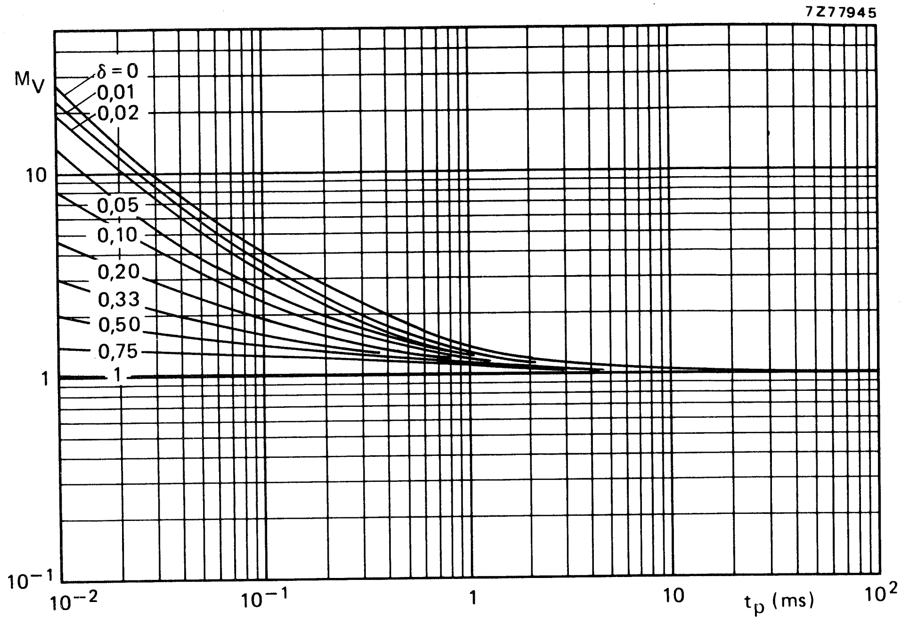


Fig. 12 S.B. voltage multiplying factor at the I_{Cmax} level.

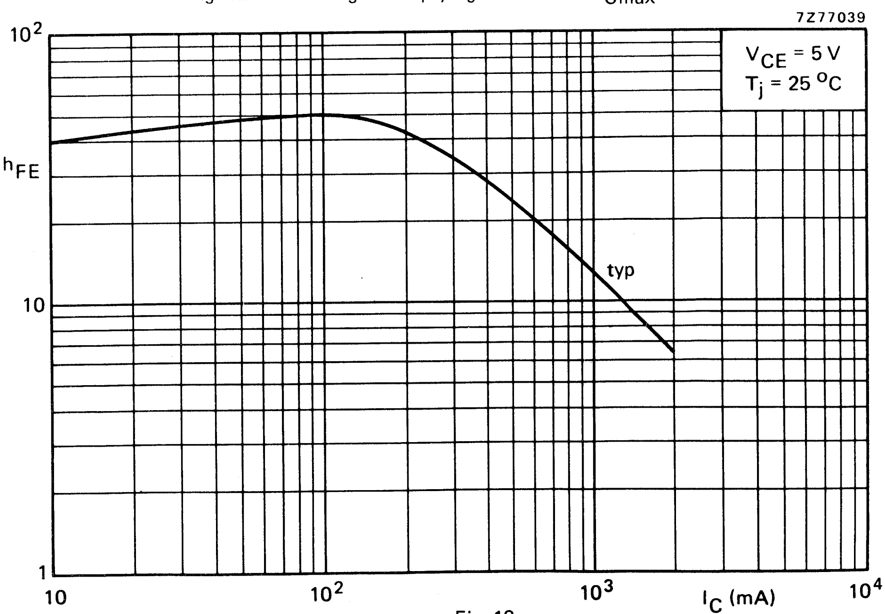


Fig. 13.

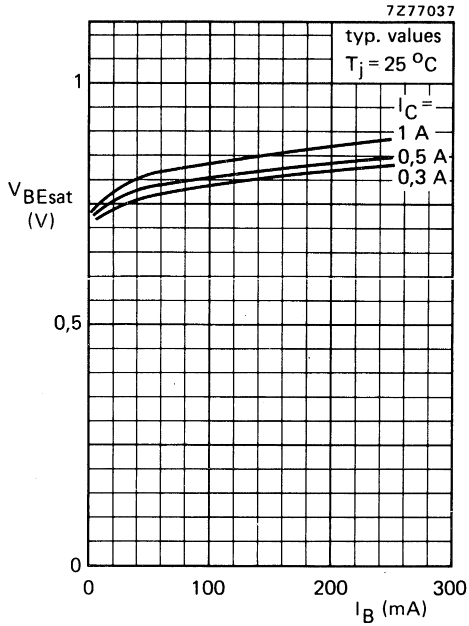


Fig. 14.

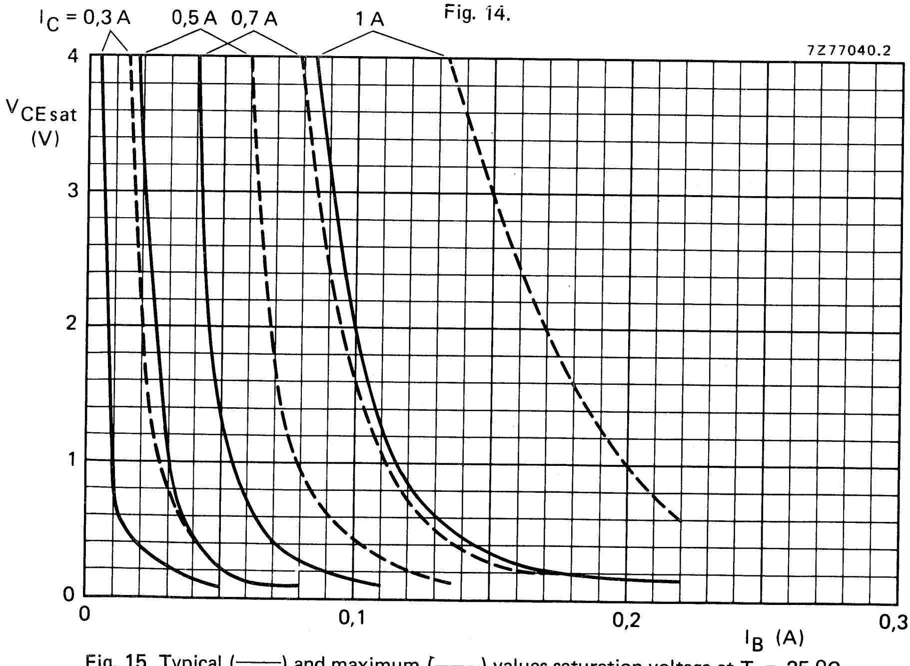


Fig. 15 Typical (——) and maximum (– – –) values saturation voltage at $T_j = 25\ ^oC$.

SILICON DIFFUSED POWER TRANSISTORS

High-voltage, high-speed, glass-passivated n-p-n power transistors in a TO-3 envelope, intended for use in converters, inverters, switching regulators, motor control systems etc.

QUICK REFERENCE DATA

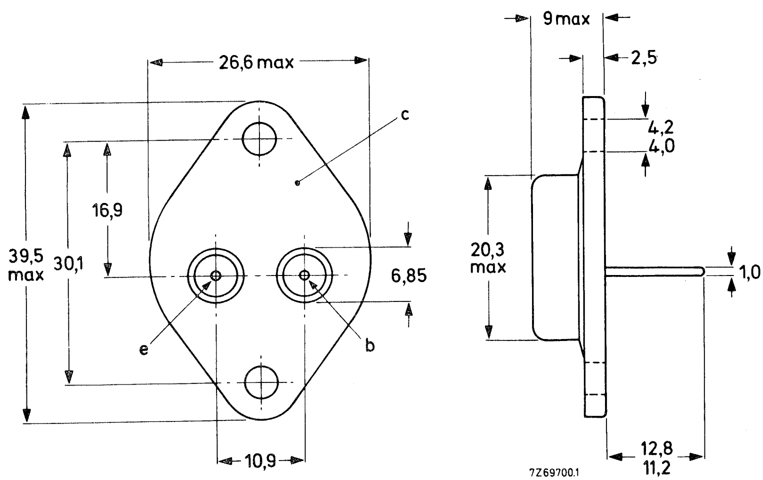
			BUX46	BUX46A	
Collector-emitter voltage (V_{EB} = 2,5 V)	V_{CEX}	max.	850	1000	V
Collector-emitter voltage ($R_{BE} \leqslant 10\ \Omega$)	V_{CER}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	3,5		A
Collector current (peak value) $t_p \leqslant 2$ ms	I_{CM}	max.	5		A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	85		W
Collector-emitter saturation voltage I_C = 2,5 A; I_B = 0,5 A	V_{CEsat}	<	1,5		V
Fall time (resistive load) I_{Con} = 2,5 A; $I_{Bon} = -I_{Boff}$ = 0,5 A	t_f	<	0,8		μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Collector connected to case.



See also chapters Mounting instructions and Accessories.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).

			BUX46	BUX46A	
Collector-emitter voltage (V_{EB} = 2,5 V)	V_{CEX}	max.	850	1000	V
Collector-emitter voltage ($R_{BE} \leqslant 10\ \Omega$)	V_{CER}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	3,5		A
Collector current (peak value) $t_p < 2$ ms	I_{CM}	max.	5		A
Base current (d.c.)	I_B	max.	1,5		A
Base current (peak value); $t_p < 2$ ms	I_{BM}	max.	3		A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	85		W
Storage temperature	T_{stg}		−65 to +175		°C
Junction temperature	T_j	max.	175		°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1,75	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			BUX46	BUX46A	
Collector cut-off current *					
$V_{CE} = V_{CERmax}$; $R_{BE} \leqslant 10\ \Omega$	I_{CER}	<	0,3		mA
$V_{CE} = V_{CERmax}$; $R_{BE} \leqslant 10\ \Omega$; T_j = 125 °C	I_{CER}	<	2		mA
Emitter cut-off current					
I_C = 0; V_{EB} = 5 V	I_{EBO}	<	1		mA
Saturation voltages					
I_C = 3,5 A; I_B = 0,7 A	V_{CEsat}	<	5		V
I_C = 2,5 A; I_B = 0,5 A	V_{CEsat}	<	1,5		V
	V_{BEsat}	<	1,3		V
Collector-emitter sustaining voltage					
I_C = 200 mA; I_B = 0; L = 25 mH	$V_{CEOsust}$	>	400	450	V
Collector-emitter cut-off current					
$V_{CE} = V_{CEXmax}$; V_{BE} = −2,5 V	I_{CEX}	<	0,1		mA
$V_{CE} = V_{CEXmax}$; V_{BE} = −2,5 V; T_j = 125 °C	I_{CEX}	<	1		mA
Emitter-base breakdown voltage					
I_C = 0; I_E = 0,5 A	$V_{(BR)EBO}$	<	30		V
Second breakdown collector current					
V_{CE} = 70 V; t = 1 sec.	$I_{(SB)C}$	>	0,5		A

* Measured with a half sine-wave voltage (curve tracer).

CHARACTERISTICS (continued)

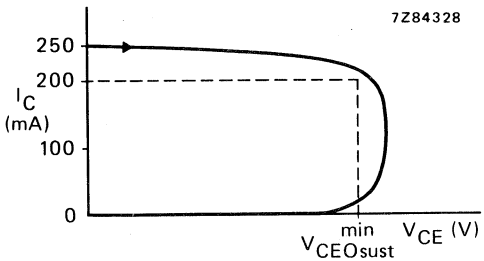


Fig. 2 Oscilloscope display for sustaining voltage.

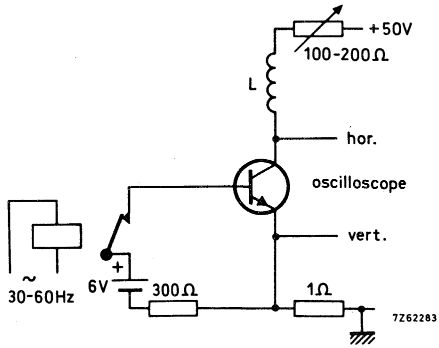


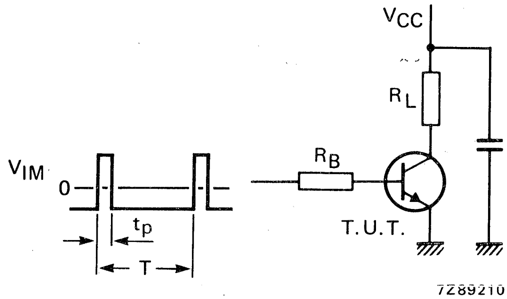
Fig. 3 Test circuit for $V_{CEOsust}$.

Switching times resistive load (Figs 4 and 5)
I_{Con} = 2,5 A; I_{Bon} = $-I_{Boff}$ = 0,5 A

Turn-on time	t_{on}	typ.	0,5 μs
		<	1 μs
Turn-off: Storage time	t_s	typ.	1,5 μs
		<	3 μs
Fall time	t_f	typ.	0,5 μs
		<	0,8 μs

Switching times inductive load (Figs 6 and 7)
I_{Con} = 2,5 A; I_B = 0,5 A

Fall time	t_f	typ.	0,2 μs



$V_{CC} = 250$ V
$V_{IM} = -6$ to $+8$ V
$\frac{t_p}{T} = 0{,}01$
$t_p = 20\ \mu s$

Fig. 4 Test circuit resistive load.
The values of R_B and R_L are selected in accordance with I_{Con} and I_B requirements.

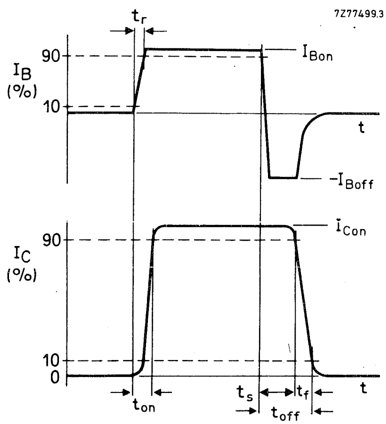


Fig. 5 Switching times waveforms with resistive load.

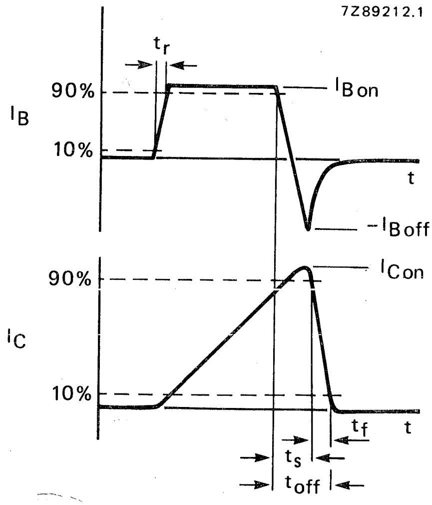
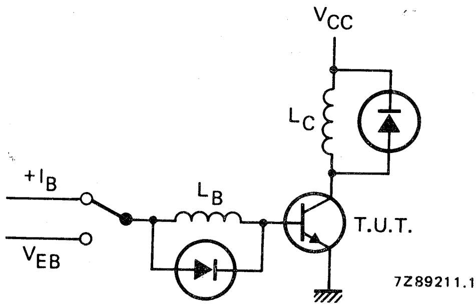


Fig. 6 Switching times waveforms with inductive load.



$V_{CC} = 300$ V
$-V_{EB} = 5$ V

Fig. 7 Test circuit inductive load. $L_C = 1$ mH; $L_B = 3\ \mu H$.

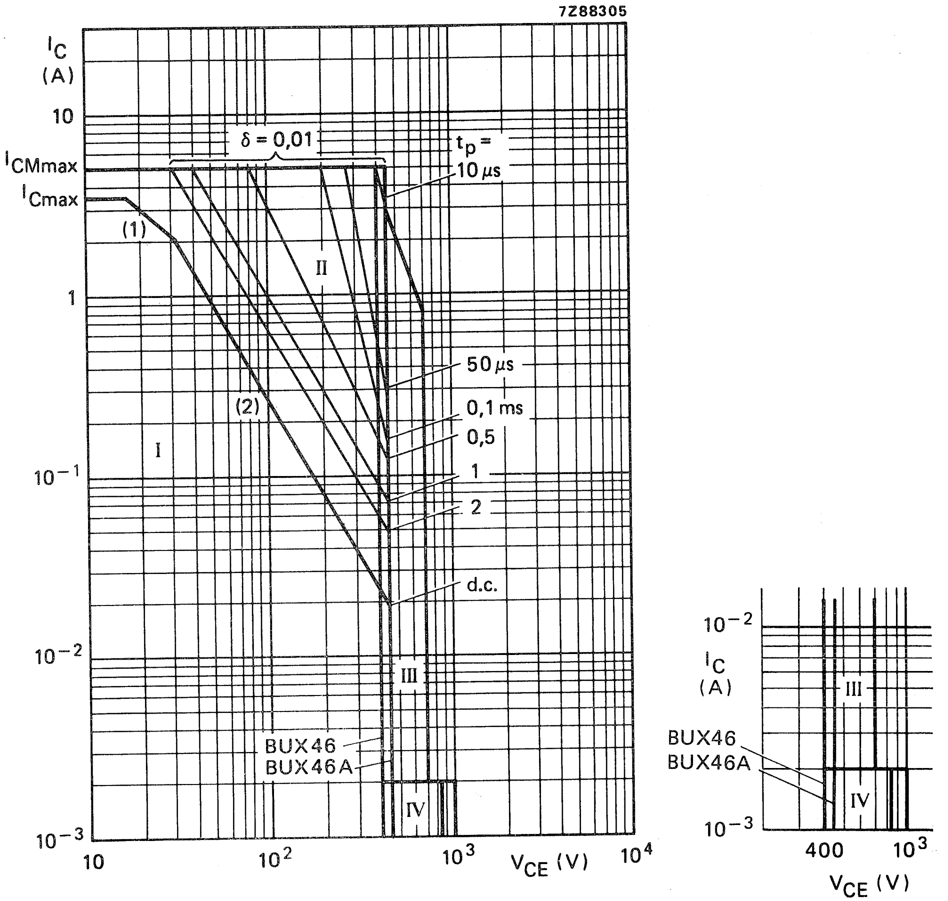


Fig. 8 Safe Operating ARea at $T_{mb} \leqslant 60\ ^{o}C$.

(1) $P_{tot\ max}$ and $P_{tot\ peak}$ max. lines.
(2) Second-breakdown limits (independent of temperature).

I Region of permissible d.c. operation.
II Permissible extension for repetitive pulse operation.
III Area of permissible operation during turn-on in single transistor converters, provided $R_{BE} \leqslant 100\ \Omega$ and $t_p \leqslant 0,6\ \mu s$.
IV Repetitive pulse operation in this region is permissible, provided $V_{BE} \leqslant 0$ and $t_p \leqslant 2$ ms.

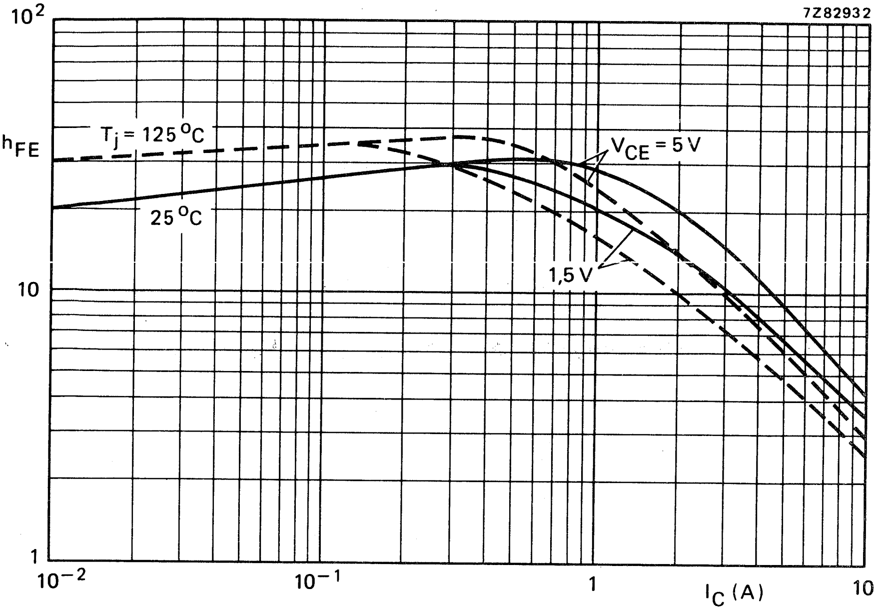


Fig. 9 D.C. current gain.

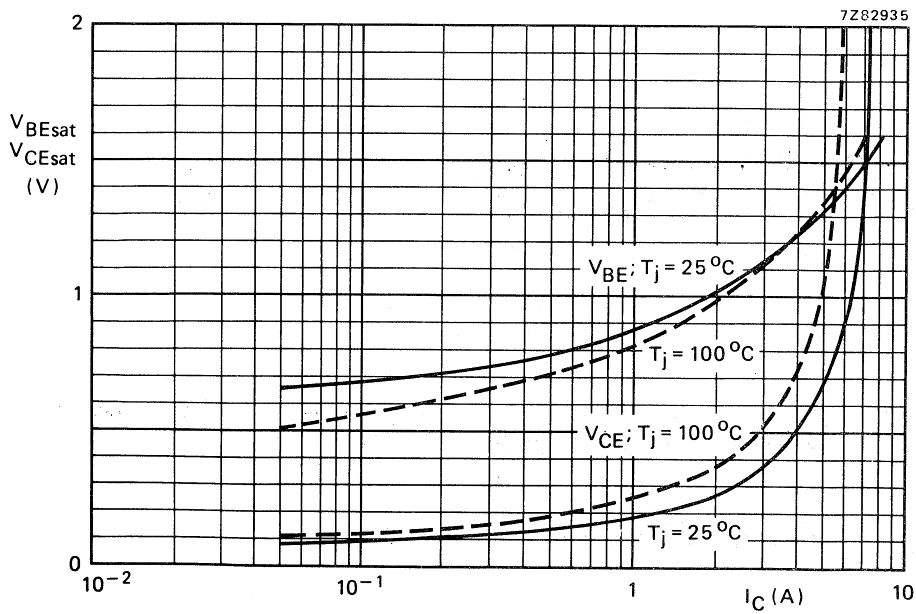


Fig. 10 Typical values base-emitter and collector-emitter voltage, $I_C/I_B = 5$.

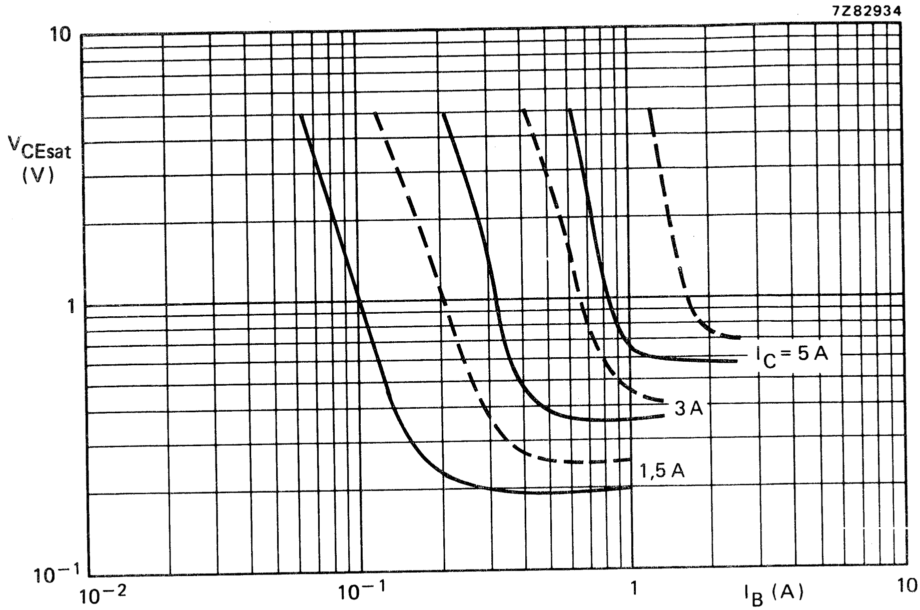


Fig. 11 Typ. (——) and max. (– – –) values collector-emitter saturation voltage at T_j = 25 °C.

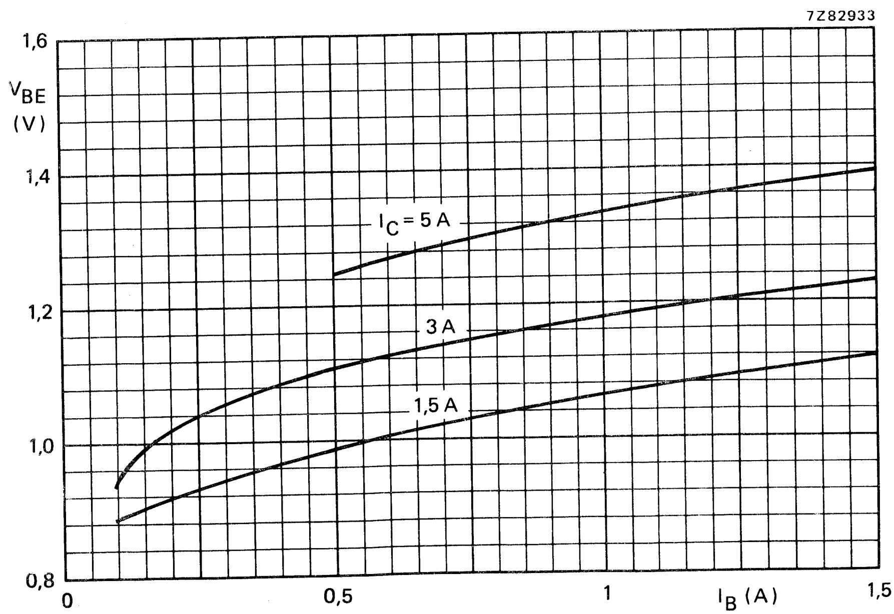


Fig. 12 Typical values at T_j = 25 °C.

SILICON DIFFUSED POWER TRANSISTORS

High-voltage, high-speed, glass-passivated n-p-n power transistors in a TO-3 envelope, intended for use in converters, inverters, switching regulators, motor control systems etc.

QUICK REFERENCE DATA

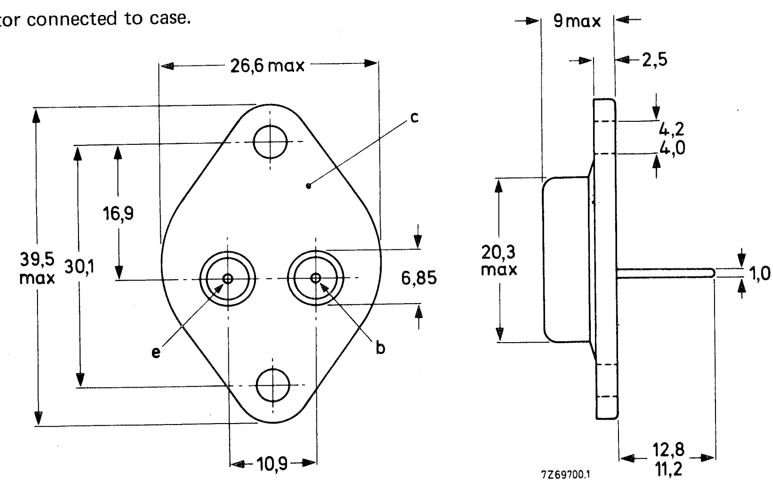
			BUX47	BUX47A	
Collector-emitter voltage (V_{EB} = 2,5 V)	V_{CEX}	max.	850	1000	V
Collector-emitter voltage ($R_{BE} \leqslant 10\ \Omega$)	V_{CER}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	9		A
Collector current (peak value) $t_p \leqslant 5$ ms	I_{CM}	max.	15		A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	125		W
Collector-emitter saturation voltage					
I_C = 6 A; I_B = 1,2 A	V_{CEsat}	<	1,5	—	V
I_C = 5 A; I_B = 1 A	V_{CEsat}	<	—	1,5	V
Fall time (resistive load)					
I_{Con} = 6 A; I_{Bon} = $-I_{Boff}$ = 1,2 A	t_f	<	0,8	—	μs
I_{Con} = 5 A; I_{Bon} = $-I_{Boff}$ = 1 A	t_f	<	—	0,8	μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Collector connected to case.



See also chapters Mounting instructions and Accessories.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BUX47	BUX47A	
Collector-emitter voltage (V_{EB} = 2,5 V)	V_{CEX}	max.	850	1000	V
Collector-emitter voltage ($R_{BE} \leqslant 10\ \Omega$)	V_{CER}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	9		A
Collector current (peak value); $t_p < 5$ ms	I_{CM}	max.	15		A
Base current (d.c.)	I_B	max.	3		A
Base current (peak value); $t_p \leqslant 5$ ms	I_{BM}	max.	6		A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	125		W
Storage temperature	T_{stg}		−65 to + 200		°C
Junction temperature	T_j	max.	200		°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1,4	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			BUX47	BUX47A	
Collector cut-off current*					
$V_{CE} = V_{CERmax}$; $R_{BE} \leqslant 10\ \Omega$	I_{CER}	<	0,4		mA
$V_{CE} = V_{CERmax}$; $R_{BE} \leqslant 10\ \Omega$; T_j = 125 °C	I_{CER}	<	3		mA
Emitter cut-off current					
I_C = 0; V_{EB} = 5 V	I_{EBO}	<	1		mA
Saturation voltages					
I_C = 6 A; I_B = 1,2 A	V_{CEsat}	<	1,5	–	V
I_C = 9 A; I_B = 1,8 A	V_{CEsat}	<	5	–	V
I_C = 5 A; I_B = 1 A	V_{CEsat}	<	–	1,5	V
I_C = 8 A; I_B = 1,6 A	V_{CEsat}	<	–	5	V
I_C = 6 A; I_B = 1,2 A	V_{BEsat}	<	1,6	–	V
I_C = 5 A; I_B = 1 A	V_{BEsat}	<	–	1,6	V
Collector-emitter sustaining voltage					
I_C = 200 mA; I_B = 0; L = 25 mH	$V_{CEOsust}$	>	400	450	V
Emitter-base breakdown voltage					
I_C = 0; I_B = 0,5 A	$V_{(BR)EBO}$		7 to 30		V
Collector cut-off current					
$V_{CE} = V_{CEXmax}$; V_{BE} = −2,5 V	I_{CEX}	<	0,15		mA
$V_{CE} = V_{CEXmax}$; V_{BE} = −2,5 V; T_j = 125 °C	I_{CEX}	<	1,5		mA

* Measured with a half sine-wave voltage (curve tracer).

CHARACTERISTICS (continued)

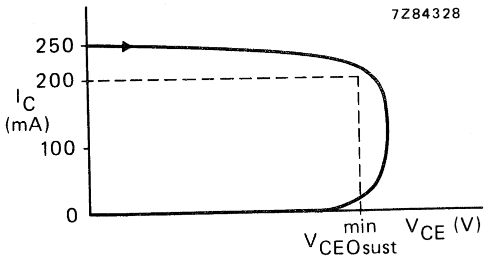


Fig. 2 Oscilloscope display for sustaining voltage.

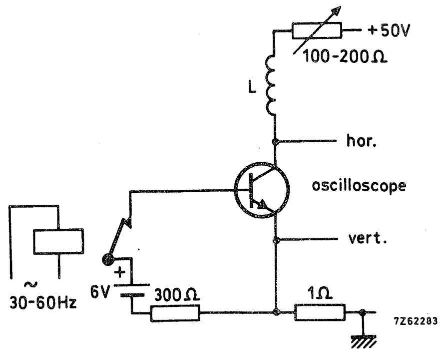


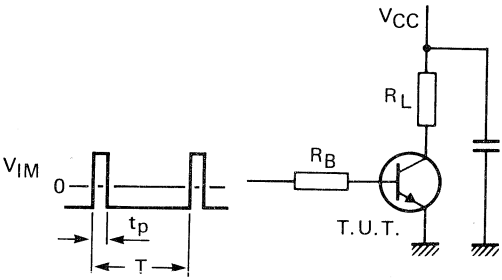
Fig. 3 Test circuit for $V_{CEOsust}$.

Switching times resistive load (Figs 4 and 5)
BUX47: I_{Con} = 6 A; I_{Bon} = $-I_{Boff}$ = 1,2 A
BUX47A: I_{Con} = 5 A; I_{Bon} = $-I_{Boff}$ = 1 A

Turn-on time	t_{on}	typ.	0,6 µs
		<	1,0 µs
Turn-off: Storage time	t_s	typ.	2,8 µs
		<	3,0 µs
Fall time	t_f	typ.	0,45 µs
		<	0,8 µs

Switching times inductive load (Figs 6 and 7)
BUX47: I_{Con} = 6 A; I_B = 1,2 A
BUX47A; I_{Con} = 5 A; I_B = 1 A

Turn-off: Storage time	t_s	typ.	2,5 µs
Storage time; T_j = 100 °C	t_s	<	4 µs
Fall time	t_f	typ.	80 ns
Fall time; T_j = 100 °C	t_f	<	400 ns



V_{CC} = 250 V
V_{IM} = −6 to + 8 V
$\frac{t_p}{T}$ = 0,01
t_p = 20 μs

Fig. 4 Test circuit resistive load.
The values of R_B and R_L are selected in accordance with I_{Con} and I_B requirements.

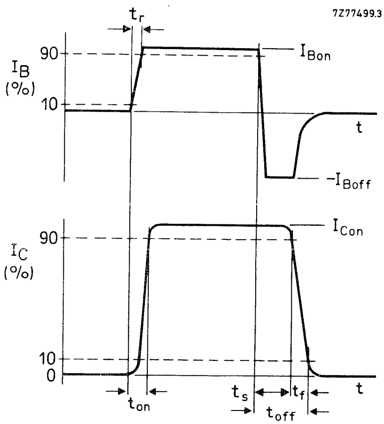


Fig. 5 Switching times waveforms with resistive load.

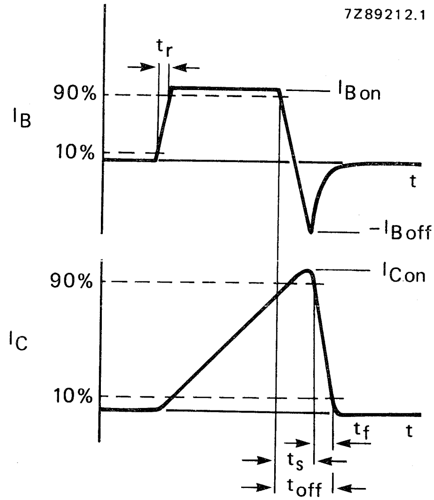
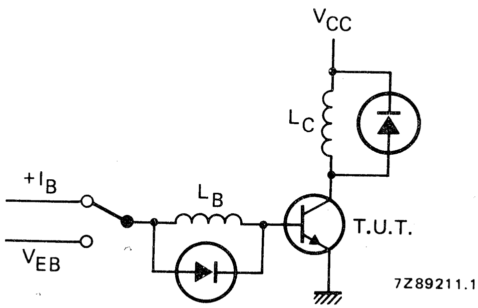
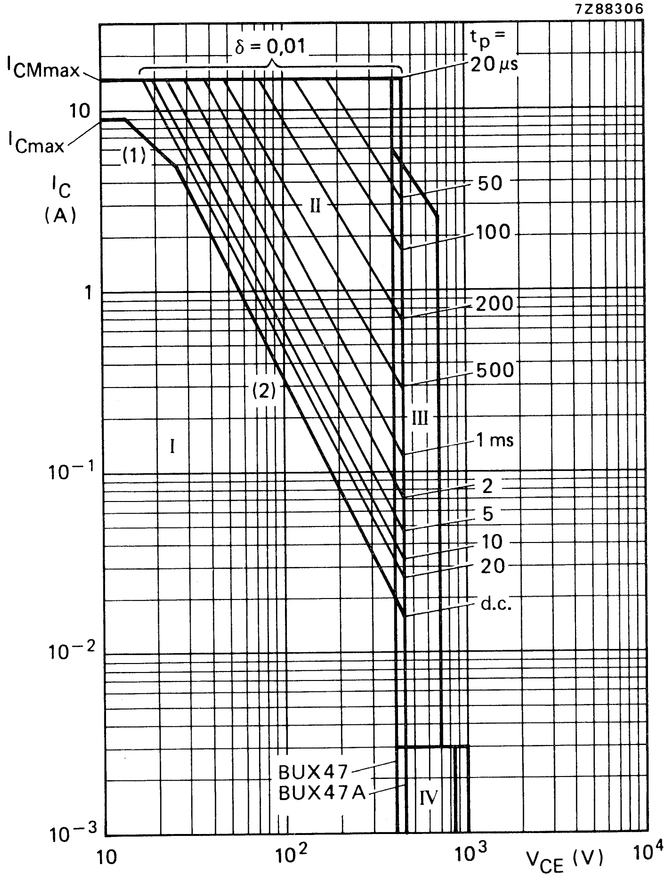


Fig. 6 Switching times waveforms with inductive load.



V_{CC} = 300 V
V_{EB} = 5 V

Fig. 7 Test circuit inductive load. L_C = 1,5 mH; L_B = 3 μH.



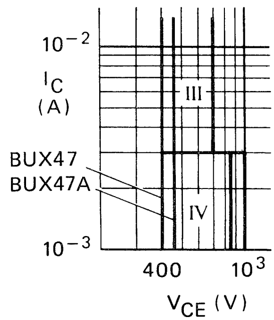


Fig. 8 Safe Operating ARea at $T_{mb} \leqslant 25\ ^oC$.

(1) $P_{tot\ max}$ and $P_{tot\ peak\ max}$ lines.
(2) Second-breakdown limits (independent of temperature).

I Region of permissible d.c. operation.
II Permissible extension for repetitive pulse operation.
III Area of permissible operation during turn-on in single transistor converters, provided $R_{BE} \leqslant 100\ \Omega$ and $t_p \leqslant 0{,}6\ \mu s$.
IV Repetitive pulse operation in this region is permissible, provided $V_{BE} \leqslant 0$ and $t_p \leqslant 2$ ms.

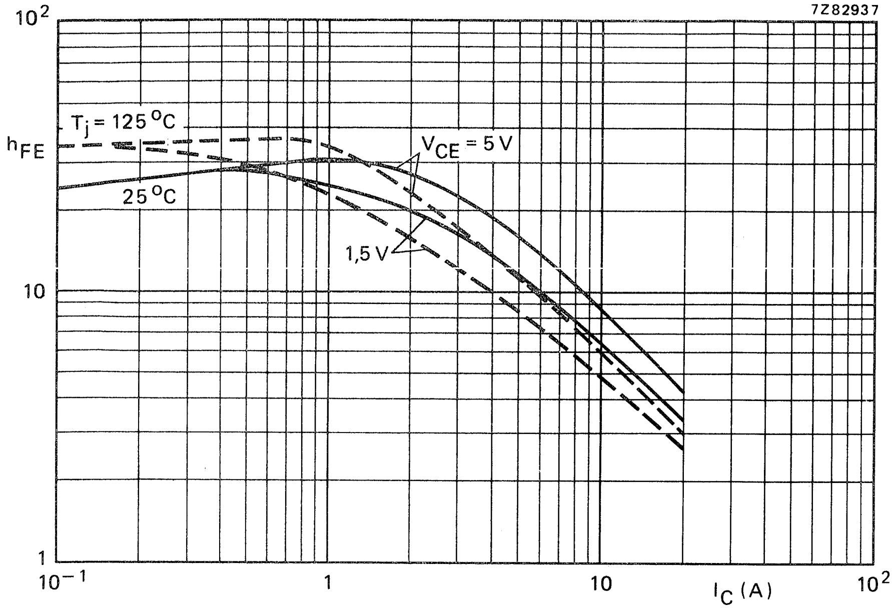


Fig. 9 Typical values d.c. current gain.

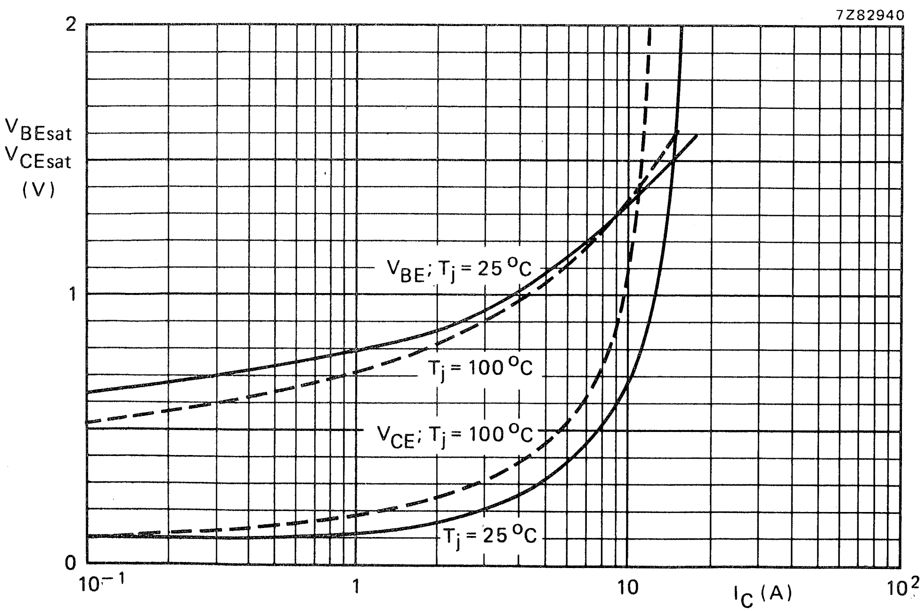


Fig. 10 Typical values base and collector voltage at I_C/I_B = 5.

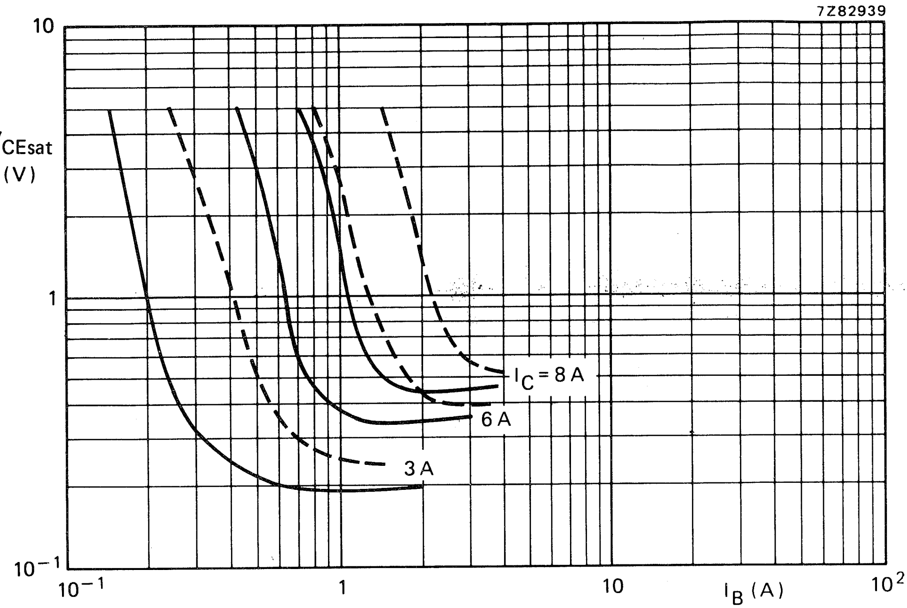


Fig. 11 Typ. (——) and max. (– – –) values collector-emitter saturation voltage at T_j = 25 °C.

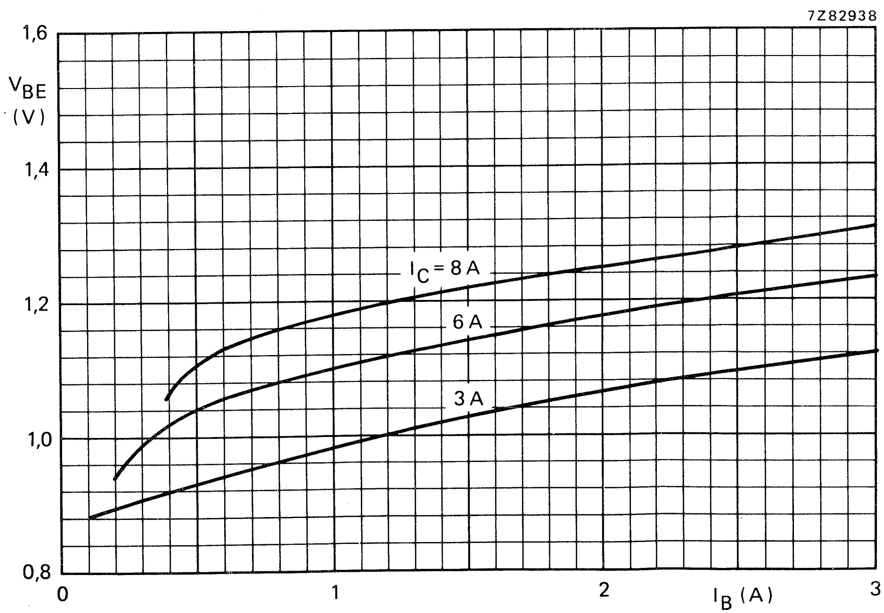


Fig. 12 Typical values base-emitter voltage at T_j = 25 °C.

SILICON DIFFUSED POWER TRANSISTORS

High-voltage, high-speed, glass-passivated n-p-n power transistors in a TO-3 envelope, intended for use in converters, inverters, switching regulators, motor control systems etc.

QUICK REFERENCE DATA

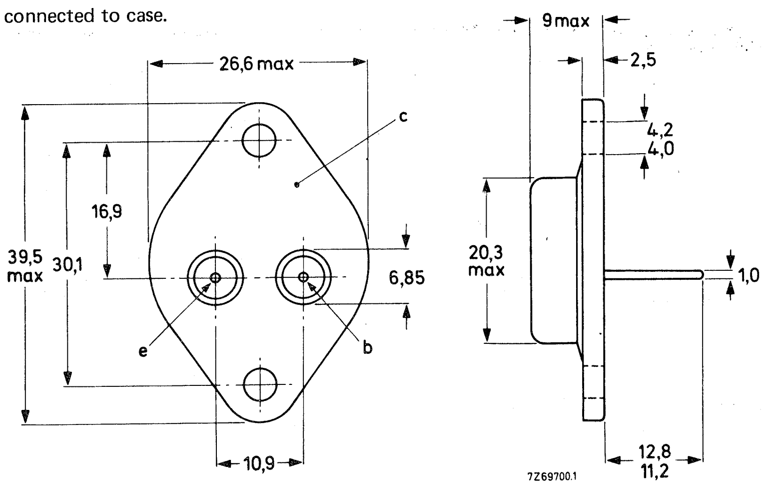
			BUX48	BUX48A	
Collector-emitter voltage (peak value; $V_{BE} = 0$)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	15	15	A
Collector current (peak value; $t_p < 2$ ms)	I_{CM}	max.	30	30	A
Total power dissipation up to $T_{mb} = 25\,^oC$	P_{tot}	max.	175	175	W
Collector-emitter saturation voltage					
$I_C = 10$ A; $I_B = 2$ A	V_{CEsat}	<	1,5	—	V
$I_C = 8$ A; $I_B = 1{,}6$ A	V_{CEsat}	<	—	1,5	V
Fall time (resistive load)					
$I_{Con} = 10$ A; $I_{Bon} = -I_{Boff} = 2$ A	t_f	<	800	—	ns
$I_{Con} = 8$ A; $I_{Bon} = -I_{Boff} = 1{,}6$ A	t_f	<	—	800	ns

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Collector connected to case.



See also chapters Mounting instructions and Accessories.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BUX48	BUX48A	
Collector-emitter voltage (peak value; $V_{BE} = 0$)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (peak value; $V_{BE} = -2,5$ V)	V_{CEX}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	15		A
Collector current (peak value)	I_{CM}	max.	30		A
Base current (d.c.)	I_B	max.	4		A
Base current (peak value)	I_{BM}	max.	20		A
Total power dissipation up to $T_{mb} = 25$ °C	P_{tot}	max.	175		W
Storage temperature	T_{stg}		−65 to +200		°C
Junction temperature	T_j	max.	200		°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\,j\text{-}mb}$	=	1,0	K/W

CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified

			BUX48	BUX48A	
Collector-emitter current					
$V_{CE} = V_{CEX}$; $R_{BE} \leq 10\ \Omega$;	I_{CER}	<	0,5		mA
$V_{CE} = V_{CEX}$; $R_{BE} \leq 10\ \Omega$; $T_j = 125$ °C	I_{CER}	<	4		mA
Collector-emitter current					
$V_{CE} = V_{CEX}$; $V_{BE} = -2,5$ V	I_{CEX}	<	0,2		mA
$V_{CE} = V_{CEX}$; $V_{BE} = -2,5$ V; $T_j = 125$ °C	I_{CEX}	<	2		mA
Emitter cut-off current					
$I_C = 0$; $V_{EB} = 5$ V	I_{EBO}	<	1		mA
Saturation voltages					
$I_C = 10$ A; $I_B = 2$ A	V_{CEsat}	<	1,5	−	V
	V_{BEsat}	<	1,6	−	V
$I_C = 8$ A; $I_B = 1,6$ A	V_{CEsat}	<	−	1,5	V
	V_{BEsat}	<	−	1,6	V
$I_C = 15$ A; $I_B = 3$ A	V_{CEsat}	<	5	−	V
$I_C = 12$ A; $I_B = 2,4$ A	V_{CEsat}	<	−	5	V
Collector-emitter sustaining voltage					
$I_C = 200$ mA; $I_{Boff} = 0$; L = 25 mH	$V_{CEOsust}$	>	400	450	V
Emitter-base breakdown voltage					
$I_C = 0$; $I_B = 50$ mA;	$V_{(BR)EBO}$		7 to 30		V

* Measured with a half sine-wave voltage (curve tracer).

CHARACTERISTICS (continued)

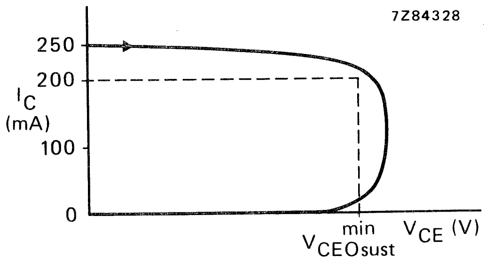


Fig. 2 Oscilloscope display for sustaining voltage.

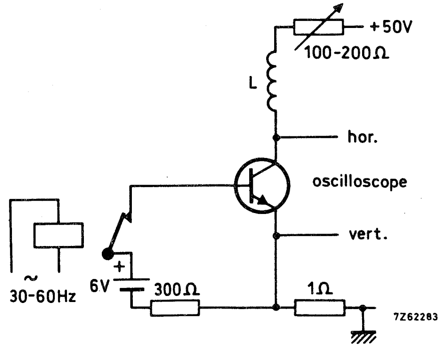


Fig. 3 Test circuit for $V_{CEOsust}$.

			BUX48	BUX48A	
Switching times resistive load (Fig. 4 and 5)					
I_{Con} = 10 A; I_{Bon} = $-I_{Boff}$ = 2 A					
Turn-on time	t_{on}	<	1	–	μs
Turn-off: Storage time	t_s	<	3	–	μs
Fall time	t_f	<	0,8	–	μs
I_{Con} = 8 A; I_{Bon} = $-I_{Boff}$ = 1,6 A					
Turn-on time	t_{on}	<	–	1	μs
Turn-off: Storage time	t_s	<	–	3	μs
Fall time	t_f	<	–	0,8	μs
Switching times inductive load (Fig. 6 and 7)					
I_{Con} = 10 A; I_{Bon} = 2 A; T_{mb} = 25 °C					
Turn-off: Storage time	t_s	typ.	3	–	μs
Fall time	t_f	typ.	80	–	ns
I_{Con} = 10 A; I_{Bon} = 2 A; T_{mb} = 100 °C					
Turn-off: Storage time	t_s	<	5	–	μs
Fall time	t_f	<	0,4	–	μs
I_{Con} = 8 A; I_{Bon} = 1,6 A; T_{mb} = 25 °C					
Turn-off: Storage time	t_s	typ.	–	3	μs
Fall time	t_f	typ.	–	80	ns
I_{Con} = 8 A; I_{Bon} = 1,6 A; T_{mb} = 100 °C					
Turn-off: Storage time	t_s	<	–	5	μs
Fall time	t_f	<	–	0,4	μs

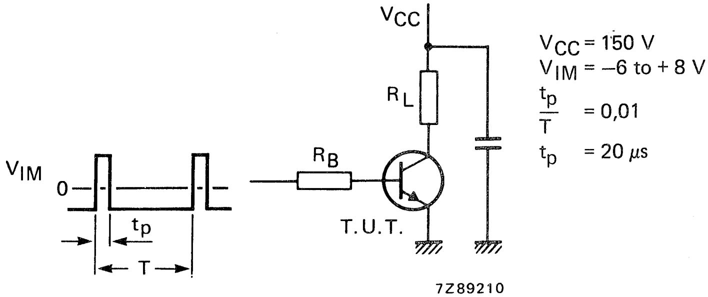


Fig. 4 Test circuit resistive load.
The values of R_B and R_L are selected in accordance with I_{Con} and I_B requirements.

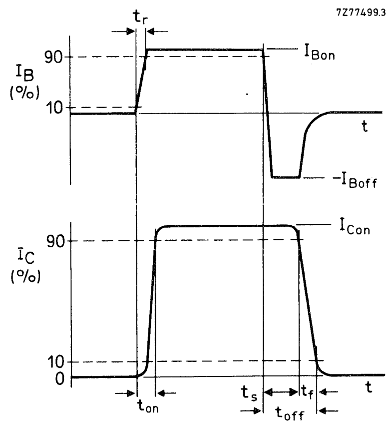


Fig. 5 Switching times waveforms with resistive load.

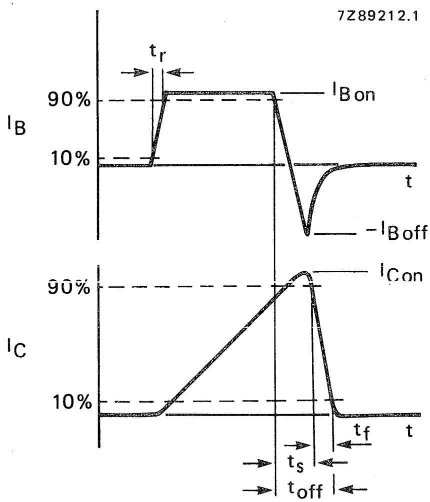


Fig. 6 Switching times waveforms with inductive load.

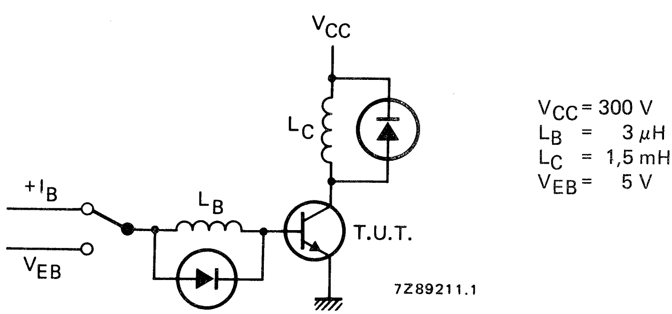


Fig. 7 Test circuit inductive load.

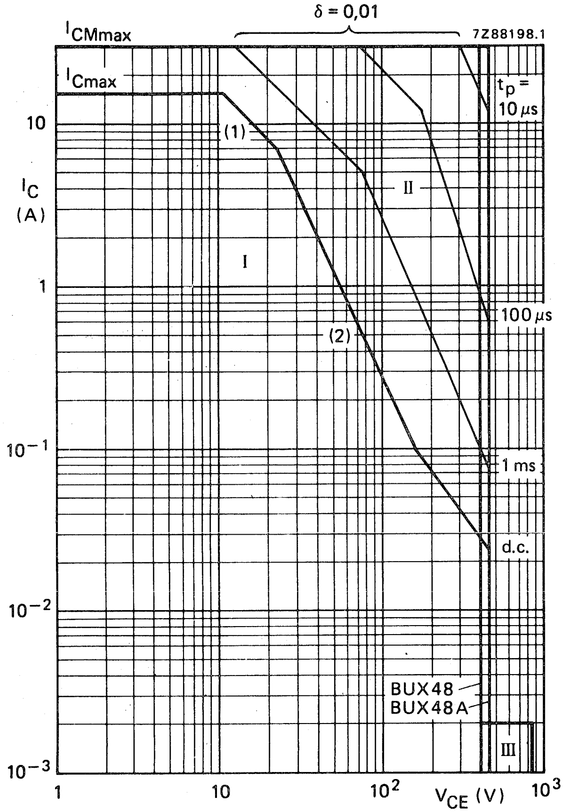


Fig. 8 Safe Operating ARea at $T_{mb} \leqslant 25\ ^{o}C$.
(1) $P_{tot\,max}$ and $P_{tot\,peak\,max}$ lines.
(2) Second-breakdown limits (independent of temperature).
I Region of permissible d.c. operation.
II Permissible extension for repetitive pulse operation.
III Repetitive pulse operation in this region is permissible, provided $V_{BE} \leqslant 0$ and $t_p \leqslant 5$ ms.

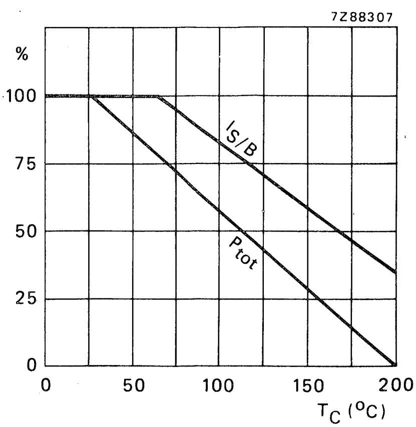


Fig. 8a Derating curve.

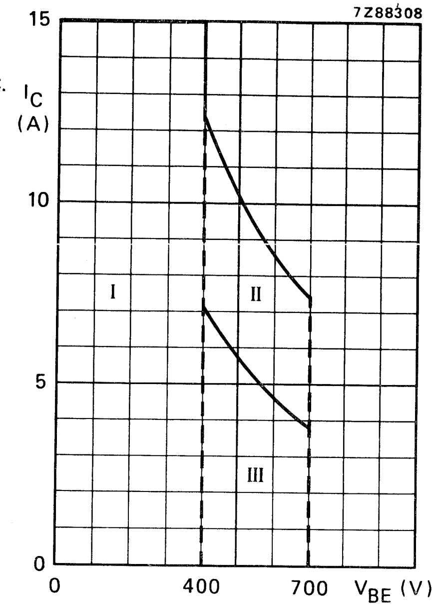


Fig. 9 Forward bias safe operation area, $T_j \leqslant 125\ ^oC$.

I Safe operation area during turn-off and during turn-on.
For BUX48A the right-hand limit is 450 V.

II Safe operation are during turn-on only provided $t_r < 0,2\ \mu s$.

III Safe operation area during turn-on only provided $t_r < 0,5\ \mu s$ and $R_{BE} < 100\ \Omega$.

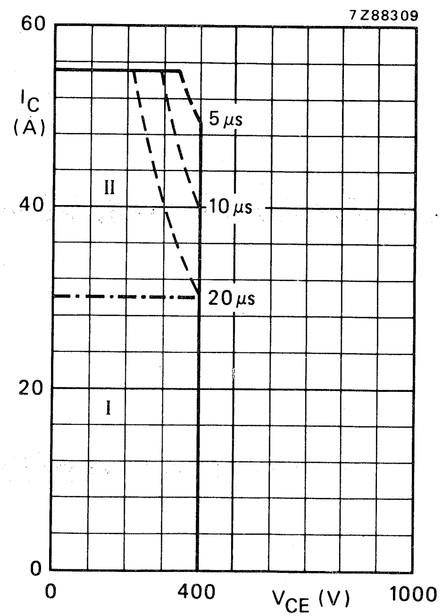


Fig. 10 Forward bias accidental overload area, $T_j \leqslant 125\ ^oC$.

I Safe operation provided normal forward bias conditions are respected ($I_{S/B}$, $T_{j\,max}$).

II Safe operation area for non-repetitive pulses. During component life the number of pulses in area II should not exceed 3000 times.

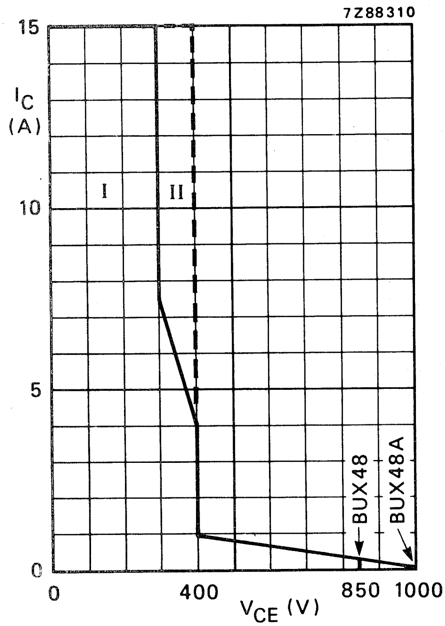


Fig. 11 Reverse bias safe operation area, $I_{Cend}/I_{Bend} \geq 5$; $-V_{BE} = 3$ V.

I Normal reverse bias safe operation area, $V_{BE} < 0$ V.

II Extension of the reverse bias safe operation area provided a desaturation network (Baker clamp) is used.

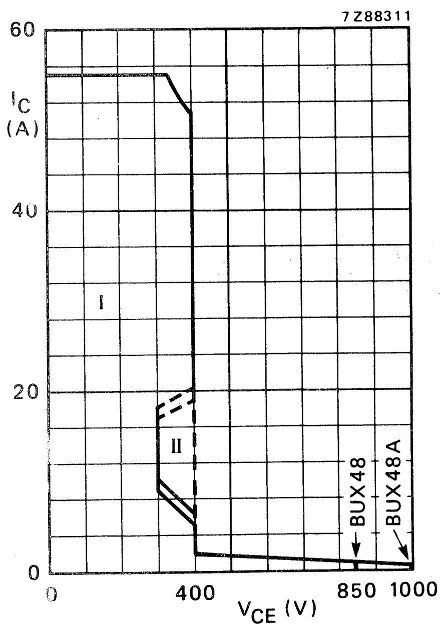


Fig. 12 Reverse bias accidental overload area, $-V_{BE} = 3$ V; $T_j \leq 125$ °C.

I Operation at high currents ($I_C > I_{CM}$) is permitted, provided the pulses are non repetitive and $V_{BE} < 0$.

II This area may be entered only through the broken line. Crossing the continuous line is not permitted.

During component life the number of surge pulses in area I and II should not exceed 3000 times.

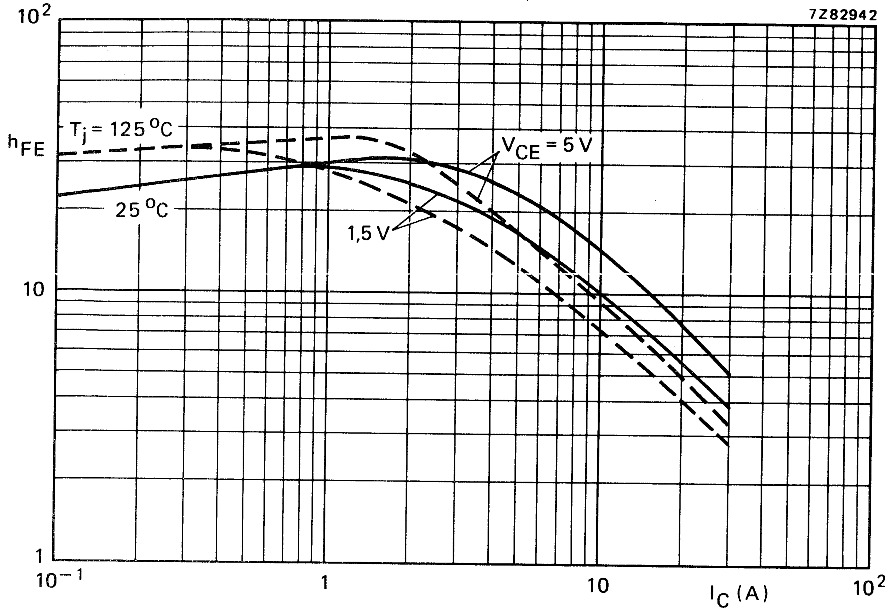


Fig. 13 Typical values d.c. current gain.

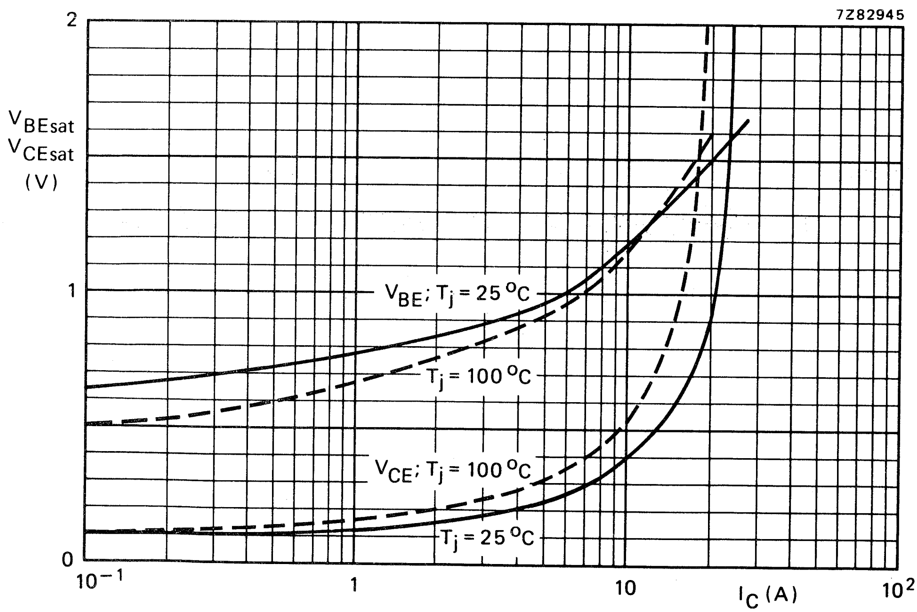


Fig. 14 Typical values base and collector voltage at $I_C/I_B = 5$.

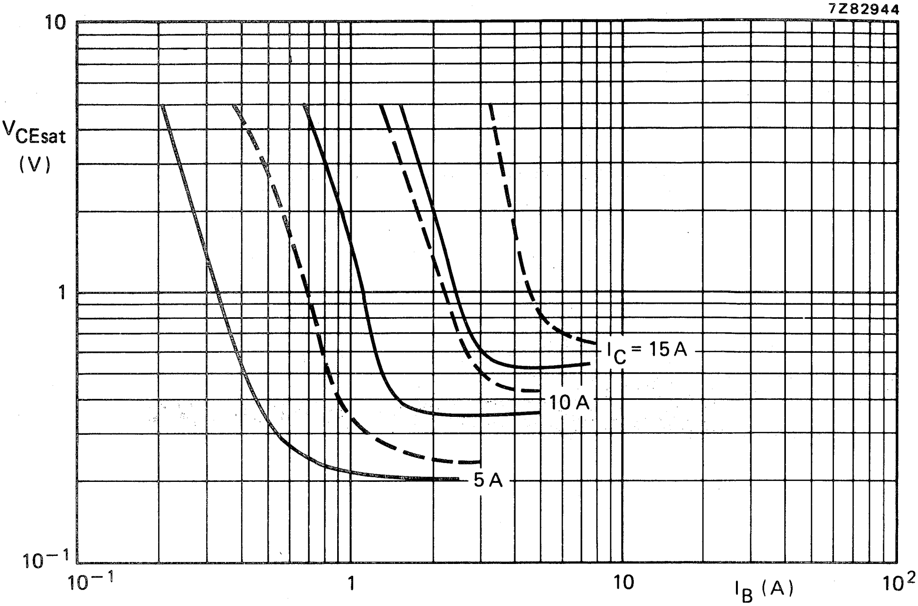


Fig. 15 Typical (——) and maximum (– – –) values saturation voltage. T_j = 25 °C.

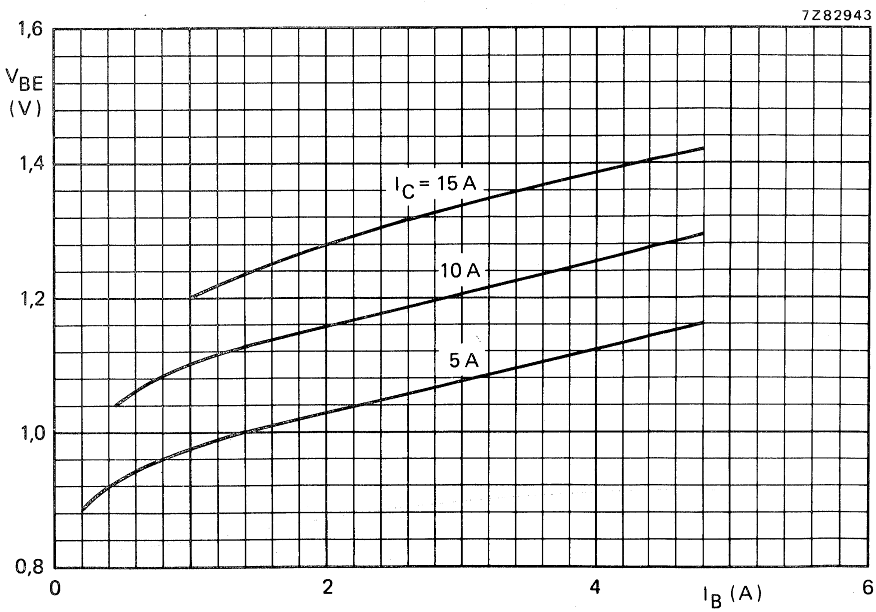


Fig. 16 Typical values base-emitter voltage at T_j = 25 °C.

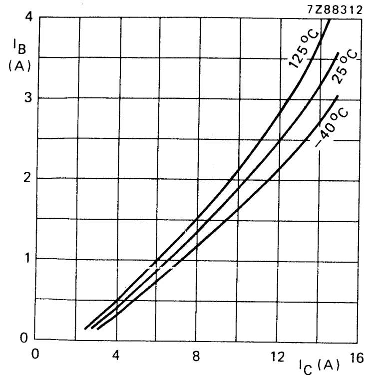


Fig. 17 Minimum base current to saturate the transistor as a function of the collector current.

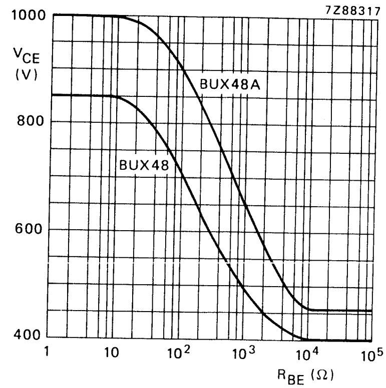


Fig. 18 Typical values collector-emitter voltage as a function of the base-emitter resistance.

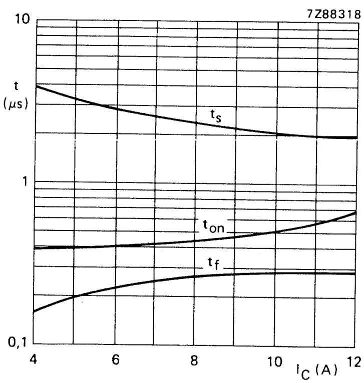


Fig. 19 Typical values switching times resistive circuits as a function of collector current.

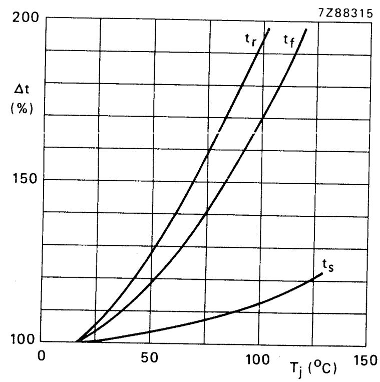


Fig. 20 Increase of switching times as a function of temperature. To read in connection with Fig. 19.

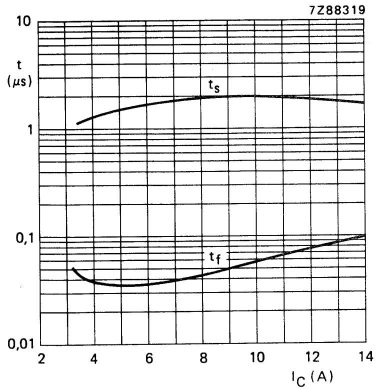


Fig. 21 Typical values switching times inductive circuits as a function of collector current.

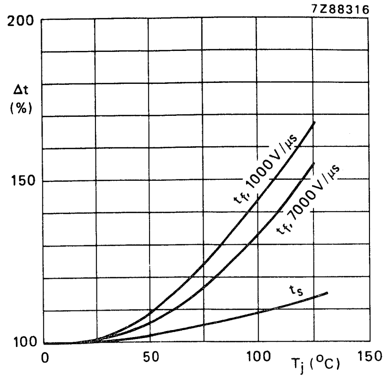


Fig. 22 Increase of storage and fall times to read in connection with Fig. 21 as a function of junction temperature.

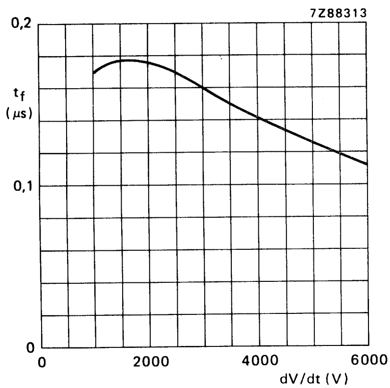


Fig. 23 Typical values fall time as a function of dV_{CE}/dt at T_{mb} = 25 °C and I_C = 10 A.

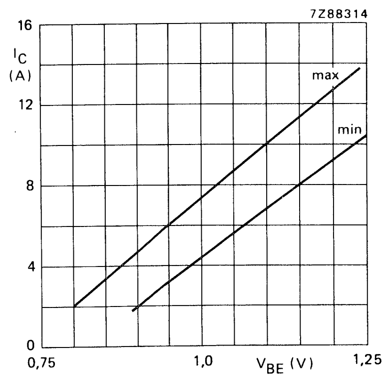


Fig. 24 Base-emitter voltage as a function of collector current at V_{CE} = 1,5 V; T_{mb} = 25 °C and 90% confidence.

SILICON DIFFUSED POWER TRANSISTORS

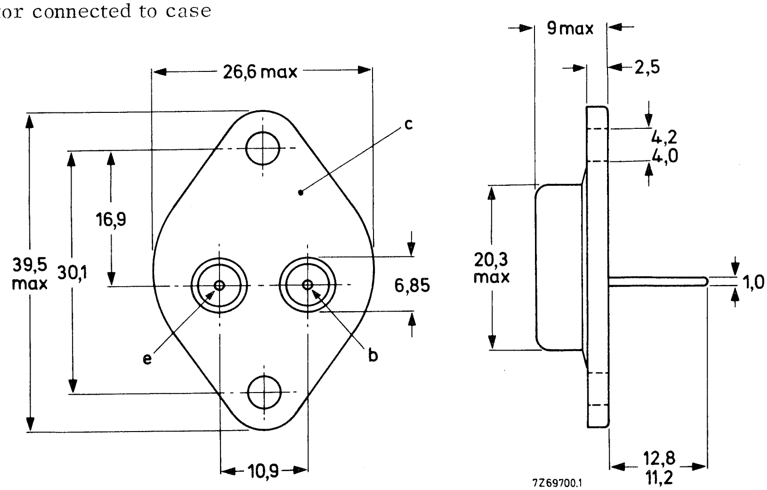
High-voltage, high-speed switching n-p-n power transistors in TO-3 envelopes, intended for use in converters, inverters, switching regulators and motor control systems.

QUICK REFERENCE DATA

			BUX80	BUX81	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	800	1000	V
Collector-emitter voltage (R_{BE} = 50 Ω)	V_{CER}	max.	500	500	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	10		A
Collector current (peak value) t_p = 2 ms	I_{CM}	max.	15		A
Total power dissipation up to T_{mb} = 40 °C	P_{tot}	max.	100		W
Collector-emitter saturation voltage I_C = 5 A; I_B = 1 A	V_{CEsat}	<	1,5		V
Fall time I_{Con} = 5 A; I_{Bon} = 1 A; $-I_{Boff}$ = 2 A	t_f	typ.	0,3		µs

MECHANICAL DATA Dimensions in mm

TO-3
Collector connected to case



See also chapters Mounting instructions and Accessories.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

			BUX80	BUX81	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	800	1000	V
Collector-emitter voltage (R_{BE} = 50 Ω)	V_{CER}	max.	500	500	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V

Currents

Collector current (d.c.)	I_C	max.	10	A
Collector current (peak value) t_p = 2 ms	I_{CM}	max.	15	A
Base current (d.c.)	I_B	max.	4	A
Base current (peak value)	I_{BM}	max.	6	A
Reverse base current (d.c. or average over any 20 ms period)	$-I_{B(AV)}$	max.	100	mA
Reverse base current (peak value) [1]	$-I_{BM}$	max.	6	A

Power dissipation

Total power dissipation up to T_{mb} = 40 °C	P_{tot}	max.	100	W

Temperatures

Storage temperature	T_{stg}		−65 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j-mb}$	=	1,1	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current [2]

$V_{CEM} = V_{CESMmax}$; $V_{BE} = 0$	I_{CES}	<	1	mA
$V_{CEM} = V_{CESMmax}$; $V_{BE} = 0$; $T_j = 125$ °C	I_{CES}	<	3	mA

D.C. current gain

I_C = 1,2 A; V_{CE} = 5 V	h_{FE}	typ.	30	

1) Turn-off current.

2) Measured with a half sine wave voltage (curve tracer).

CHARACTERISTICS (continued) T_j = 25 °C unless otherwise specified

Emitter cut-off current

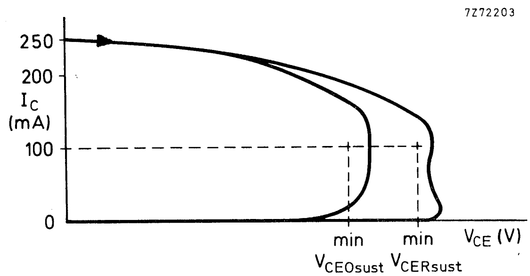
I_C = 0; V_{EB} = 10 V	I_{EBO}	<	10	mA

Saturation voltages

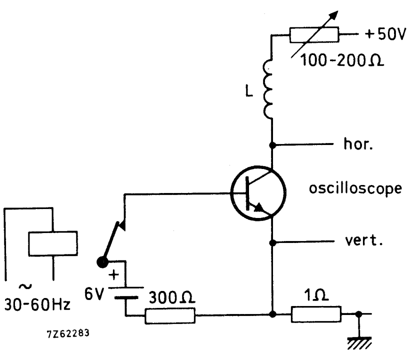
I_C = 5 A; I_B = 1 A	V_{CEsat}	<	1,5	V
	$V_{BE\,sat}$	<	1,4	V
I_C = 8 A; I_B = 2,5 A	V_{CEsat}	<	3	V
	$V_{BE\,sat}$	<	1,8	V

Collector-emitter sustaining voltages

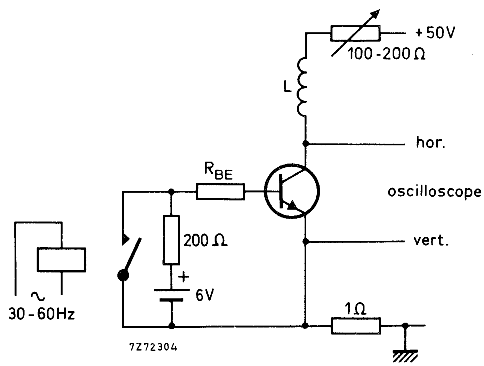
			BUX80	BUX81	
I_C = 100 mA; I_{Boff} = 0; L = 25 mH	$V_{CEOsust}$	>	400	450	V
I_C = 100 mA; R_{BE} = 50 Ω; L = 15 mH	$V_{CERsust}$	>	500	500	V



Oscilloscope display for sustaining voltages



Test circuit for $V_{CEOsust}$

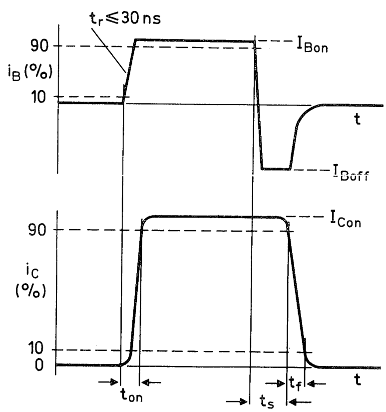


Test circuit for $V_{CERsust}$

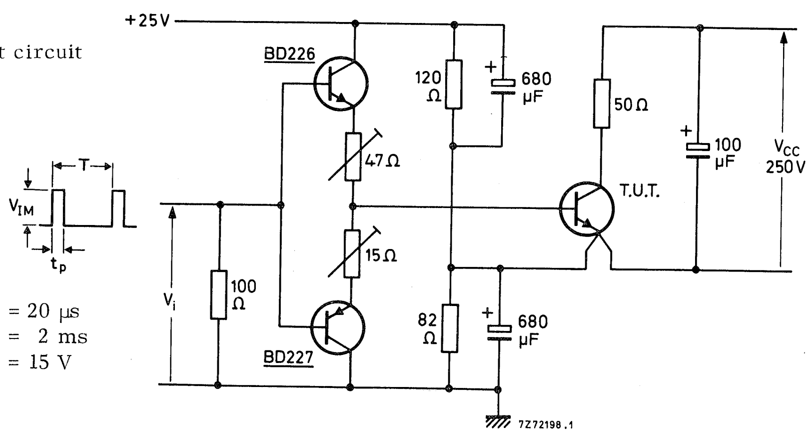
CHARACTERISTICS (continued) T_j = 25 °C unless otherwise specified

Transition frequency at f = 1 MHz				
I_C = 0,2 A; V_{CE} = 10 V	f_T	typ.	6	MHz
Switching times				
I_{Con} = 5 A; V_{CC} = 250 V I_{Bon} = 1 A; $-I_{Boff}$ = 2 A				
Turn-on time	t_{on}	typ. <	0,35 0,5	μs μs
Turn-off: Storage time	t_s	typ. <	2,5 3,5	μs μs
Fall time	t_f	typ.	0,3	μs
Fall time, T_{mb} = 95 °C	t_f	<	0,8	μs

Waveform

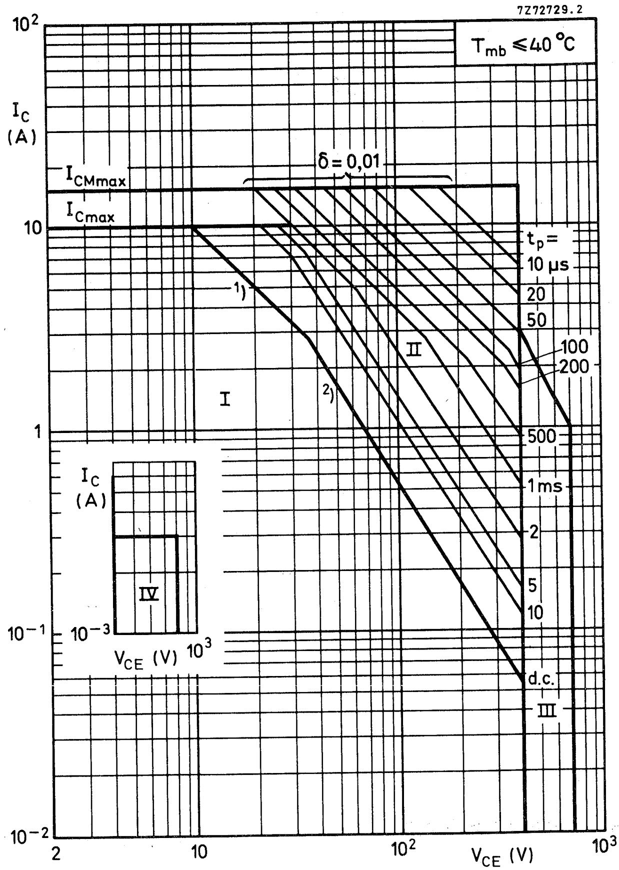


Test circuit



t_p = 20 μs
T = 2 ms
V_{IM} = 15 V

BUX80



Safe Operating ARea

I Region of permissible d.c. operation

II Permissible extension for repetitive pulse operation

III Area of permissible operation during turn-on in single-transistor converters, provided $R_{BE} \leq 100\ \Omega$ and $t_p \leq 0,6\ \mu s$

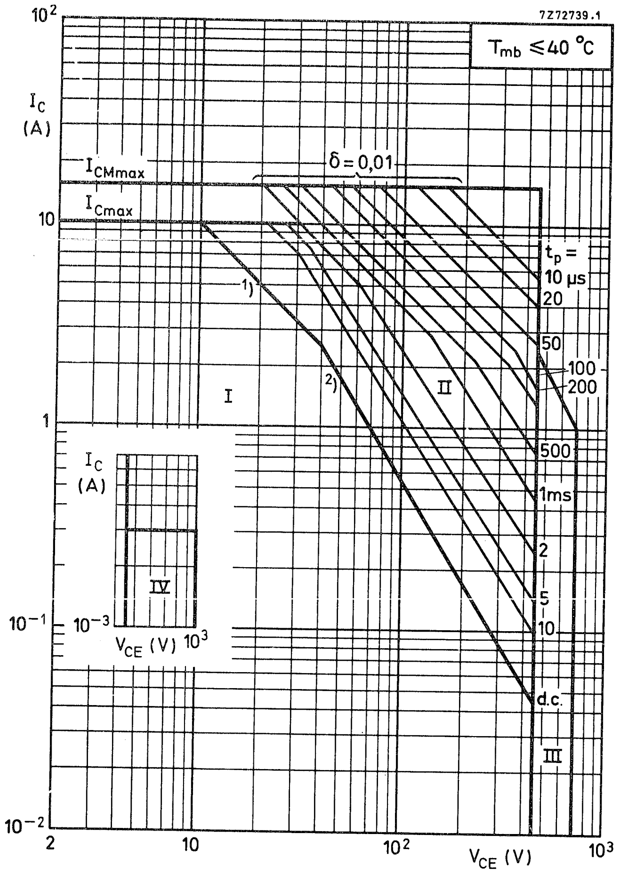
IV Repetitive pulse operation in this region is permissible, provided $V_{BE} \leq 0$ and $t_p \leq 2$ ms

---

1) $P_{tot\ max}$ and $P_{peak\ max}$ lines.

2) Second-breakdown limits (independent of temperature).

BUX81



Safe Operating ARea

I Region of permissible d.c. operation

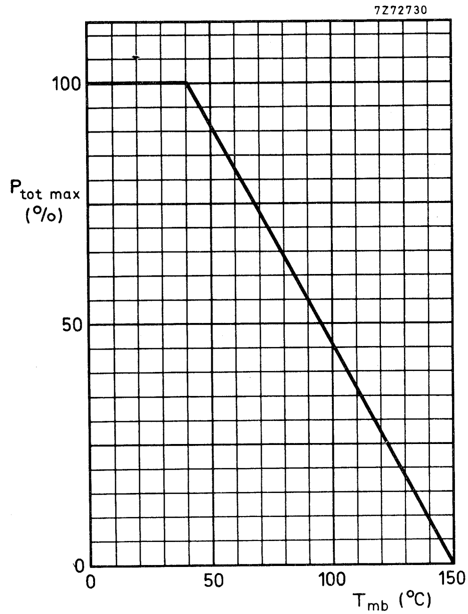
II Permissible extension for repetitive pulse operation

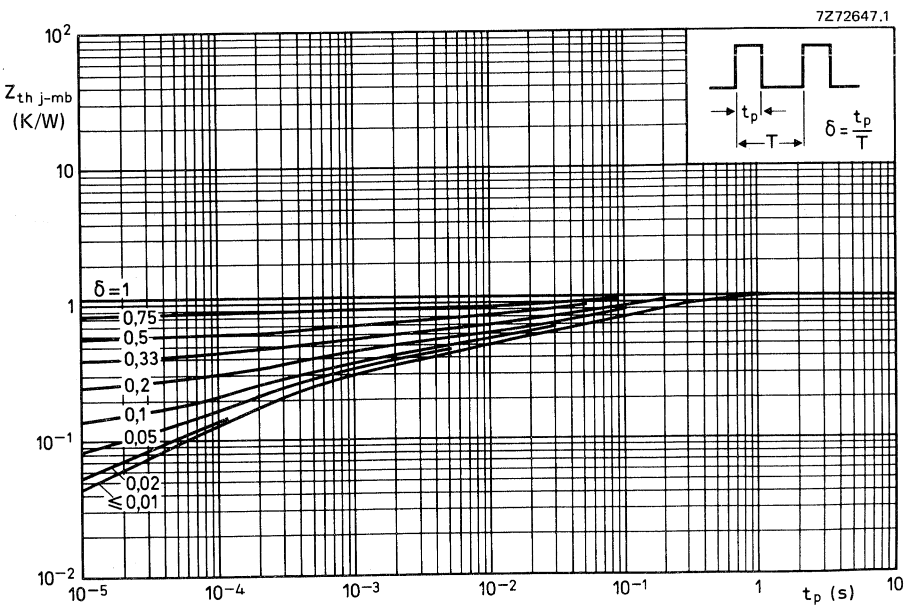
III Area of permissible operation during turn-on in single-transistor converters, provided $R_{BE} \leq 100\ \Omega$ and $t_p \leq 0,6$ μs

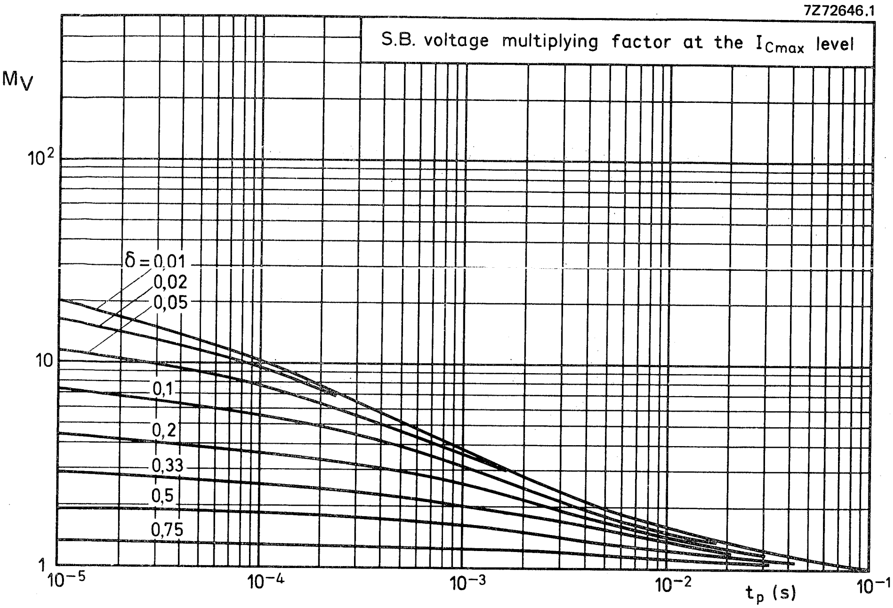
IV Repetitive pulse operation in this region is permissible, provided $V_{BE} \leq 0$ and $t_p \leq 2$ ms

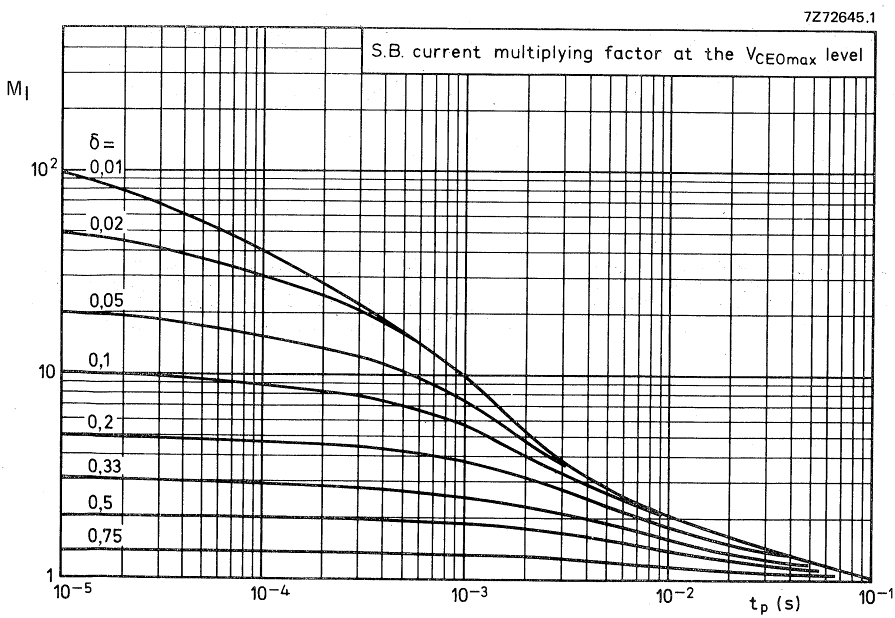
1) $P_{tot\ max}$ and $P_{peak\ max}$ lines.

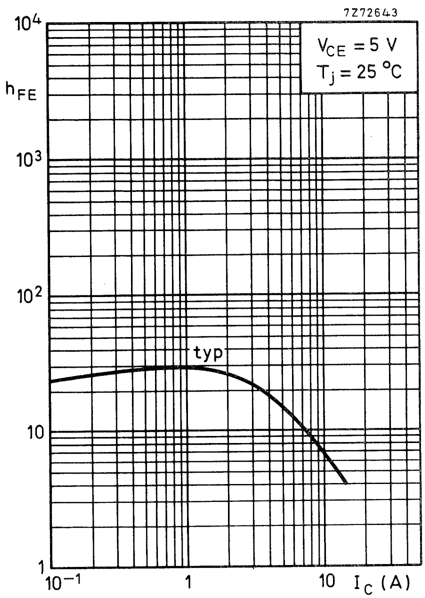
2) Second-breakdown limits (independent of temperature).

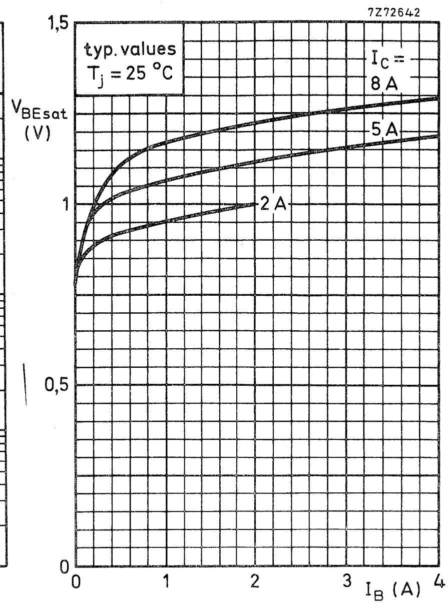

7Z72730
100
$P_{tot\ max}$
(%)
50
0
0
50
100
150
T_{mb} (°C)

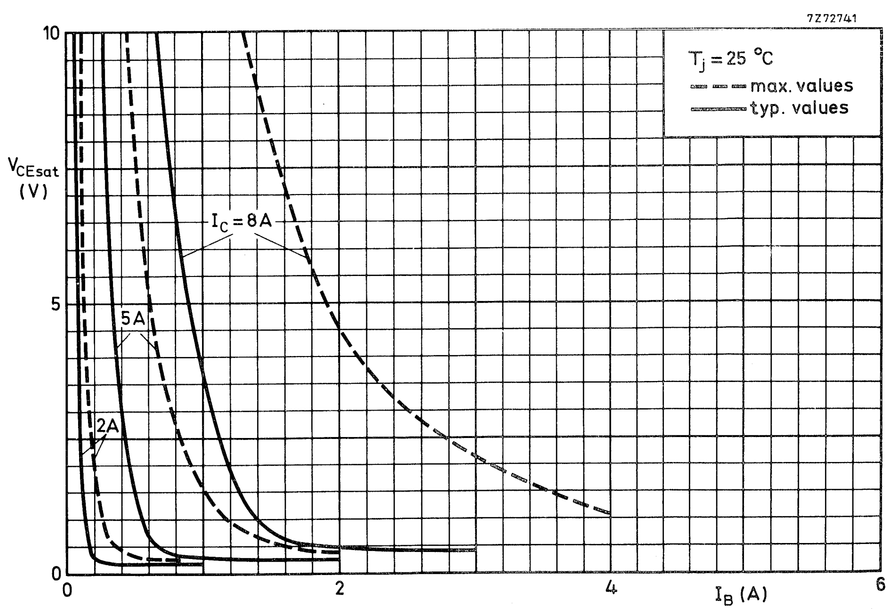

7Z72647.1
10^2
$Z_{th\ j\text{-}mb}$
(K/W)
10
1
10^{-1}
10^{-2}
δ=1
0,75
0,5
0,33
0,2
0,1
0,05
0,02
≤0,01
t_p
T
$\delta = \frac{t_p}{T}$
10^{-5}
10^{-4}
10^{-3}
10^{-2}
10^{-1}
1
t_p (s)
10


7Z72646.1
S.B. voltage multiplying factor at the I_{Cmax} level
M_V
10^2
10
1
δ = 0,01
0,02
0,05
0,1
0,2
0,33
0,5
0,75
10^{-5}
10^{-4}
10^{-3}
10^{-2}
t_p (s)
10^{-1}


7Z72645.1
S.B. current multiplying factor at the V_{CEOmax} level
M_I
δ =
0,01
0,02
0,05
0,1
0,2
0,33
0,5
0,75
10^2
10
1
10^{-5}
10^{-4}
10^{-3}
10^{-2}
t_p (s)
10^{-1}


7Z72643
$V_{CE} = 5$ V
$T_j = 25$ °C
h_{FE}
typ
I_C (A)


7Z72642
typ. values
$T_j = 25$ °C
$I_C =$
8 A
5 A
2 A
V_{BEsat} (V)
I_B (A)


7Z72741
$T_j = 25$ °C
max. values
typ. values
V_{CEsat} (V)
$I_C = 8$ A
5A
2A
I_B (A)

APPLICATION INFORMATION ON BUX80 (detailed information on request)

Important factors in the design of SMPS circuits are the power losses and heatsink requirements of the supply output transistor and the base drive conditions during turn-off. In SMPS circuits with mains isolation the duty factor of the collector current generally varies between 0,25 and 0,5.

The operating frequency lies between 15 kHz and 50 kHz and the shape of the collector current varies from rectangular in a forward converter to a sawtooth in a flyback circuit.

As the BUX80 will mainly be used in forward or push-pull converters the information on optimum base drive and device dissipation given in the graphs on page 12 is concentrated on this application.
In these figures I_{CM} represents the highest repetitive peak collector current that can occur in the given circuit, e.g. during overload.

The total power dissipation for a limit-case transistor is given in Fig. 5 which applies for a mounting base temperature of 100 °C. The required thermal resistance for the heatsink can be calculated from

$$R_{th\ mb\text{-}a} = \frac{100 - T_{amb\ max}}{P_{tot}}.$$

To ensure thermal stability the minimum value of T_{amb} in the above equation is 40 °C.

A practical SMPS output circuit for an output power in the order of 400 W is given in Fig. 2.

At a collector current of 5 A and a base current of 1 A in this circuit the following turn-off times can be expected.

			T_{mb} = 25 °C	100 °C	
Storage time	t_s	typ	2	2,7	µs
Fall time	t_f	typ	0,18	0,5	µs

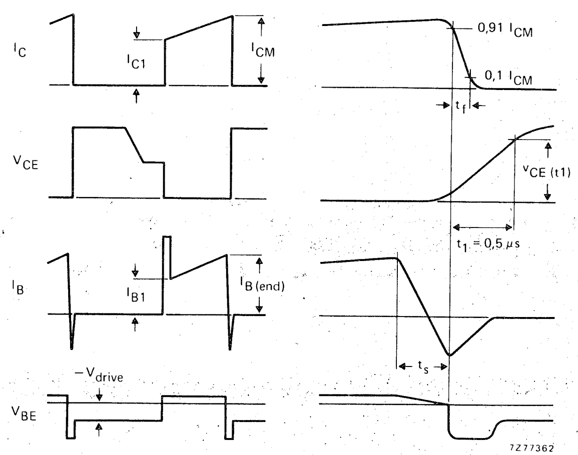


Fig. 1 Relevant waveforms of switching transistor.

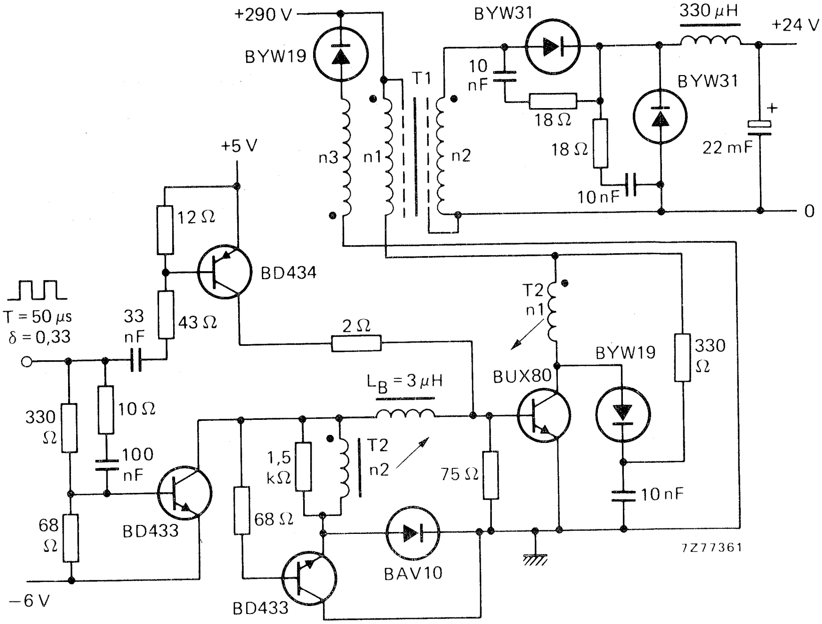


Fig. 2 Practical SMPS output circuit.

T1 (output transformer): Core U64; n1 = n3 = 56 turns; n2 = 17 turns

T2 (base current transformer): Core U20; n1 = 5 turns; n2 = 25 turns

$V_{CE(t1)} < 300$ V (see Fig. 1)

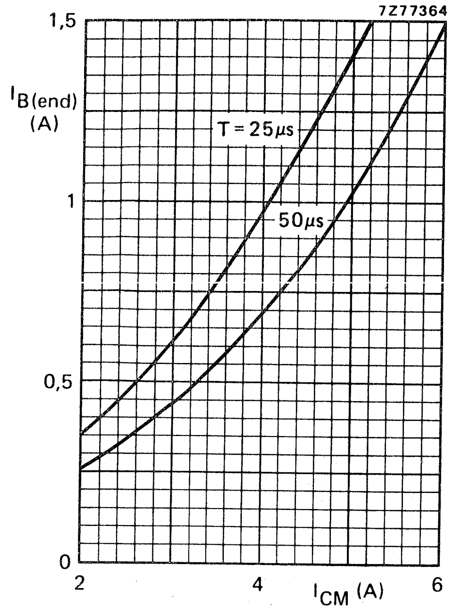


Fig. 3.

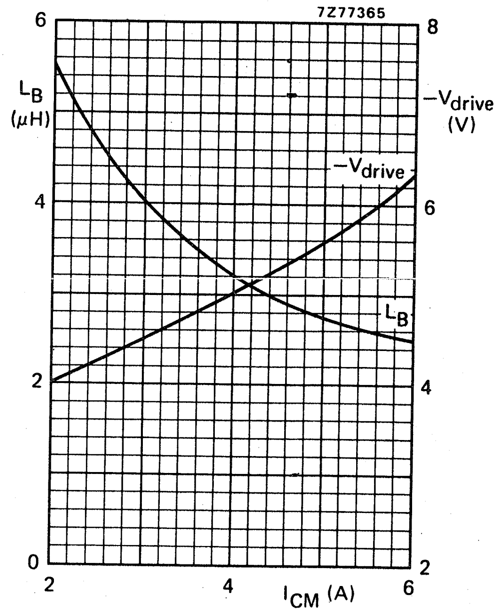


Fig. 4.

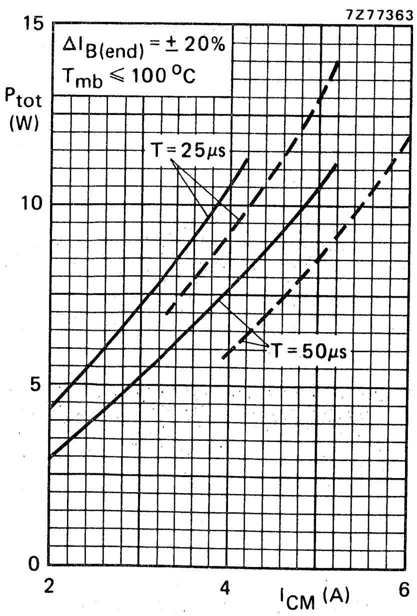


Fig. 5.

Fig. 3 Recommended nominal "end" value of the base current versus maximum peak collector current.

Fig. 4 Minimum required base inductance and recommended negative drive voltage versus maximum peak collector current.

Fig. 5 Maximum total power dissipation of a limit-case transistor if the base current is chosen in accordance with Fig. 3. Solid lines for transformer drive and dotted lines for collector-coupled current drive.

SILICON DIFFUSED POWER TRANSISTORS

High-voltage, high-speed switching n-p-n power transistors in TO-3 envelopes, intended for use in converters, inverters, switching regulators and motor control systems.

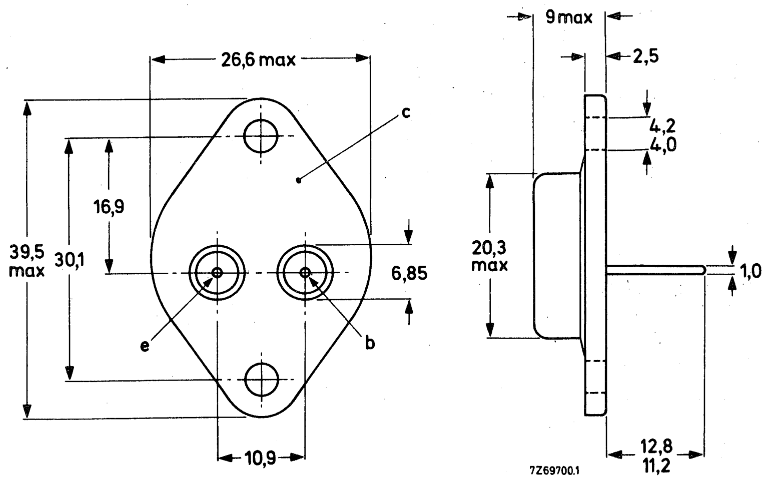
QUICK REFERENCE DATA

			BUX82	BUX83	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	800	1000	V
Collector-emitter voltage (R_{BE} = 100 Ω)	V_{CER}	max.	500	500	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	6		A
Collector current (peak value) t_p = 2 ms	I_{CM}	max.	8		A
Total power dissipation up to T_{mb} = 50 °C	P_{tot}	max.	60		W
Collector-emitter saturation voltage I_C = 2,5 A; I_B = 0,5 A	V_{CEsat}	<	1,5		V
Fall time I_{Con} = 2,5 A; I_{Bon} = 0,5 A; $-I_{Boff}$ = 1 A	t_f	typ.	0,3		μs

MECHANICAL DATA

Dimensions in mm

TO-3
Collector connected to case



See also chapters Mounting instructions and Accessories.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

			BUX82	BUX83	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	800	1000	V
Collector-emitter voltage (R_{BE} = 100 Ω)	V_{CER}	max.	500	500	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V

Currents

Collector current (d.c.)	I_C	max.	6	A
Collector current (peak value) t_p = 2 ms	I_{CM}	max.	8	A
Base current (d.c.)	I_B	max.	2	A
Base current (peak value)	I_{BM}	max.	3	A
Reverse base current (d.c. or average over any 20 ms period)	$-I_{B(AV)}$	max.	100	mA
Reverse base current (peak value) 1)	$-I_{BM}$	max.	3	A

Power dissipation

Total power dissipation up to T_{mb} = 50 °C	P_{tot}	max.	60	W

Temperatures

Storage temperature	T_{stg}		−65 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1,65	K/W

CHARACTERISTICS T_j = 25 °C unless otherwise specified

Collector cut-off current 2)

$V_{CEM} = V_{CESMmax}$; $V_{BE} = 0$	I_{CES}	<	1	mA
$V_{CEM} = V_{CESMmax}$; $V_{BE} = 0$; T_j = 125 °C	I_{CES}	<	2	mA

D.C. current gain

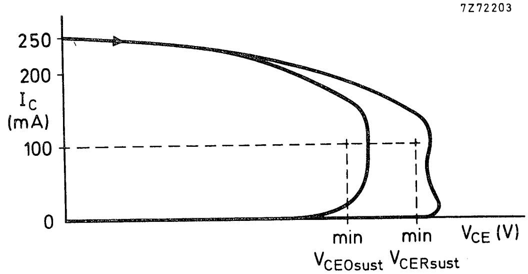
I_C = 0,6 A; V_{CE} = 5 V	h_{FE}	typ.	30

1) Turn-off current.

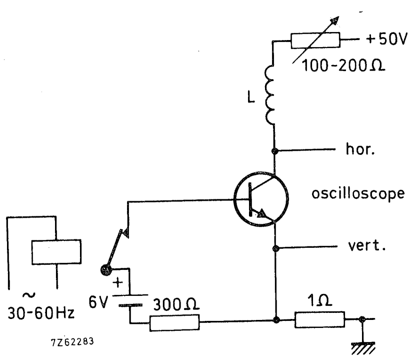
2) Measured with a half sine wave voltage (curve tracer).

CHARACTERISTICS (continued) — T_j = 25 °C unless otherwise specified

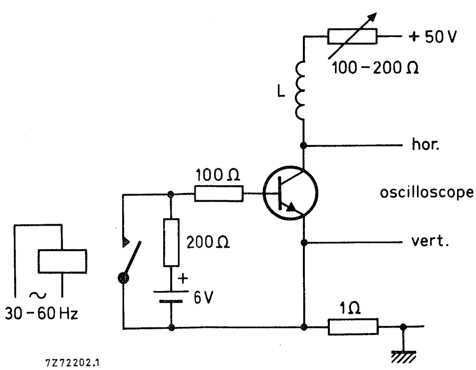
Emitter cut-off current					
I_C = 0; V_{EB} = 10 V	I_{EBO}	<	10		mA
Saturation voltages					
I_C = 2,5 A; I_B = 0,5 A	V_{CEsat}	<	1,5		V
	$V_{BE\,sat}$	<	1,4		V
I_C = 4 A; I_B = 1,25 A	V_{CEsat}	<	3		V
	$V_{BE\,sat}$	<	1,6		V
Collector-emitter sustaining voltages			BUX82	BUX83	
I_C = 100 mA; I_{Boff} = 0; L = 25 mH	$V_{CEOsust}$	>	400	450	V
I_C = 100 mA; R_{BE} = 100 Ω; L = 15 mH	$V_{CERsust}$	>	500	500	V



Oscilloscope display for sustaining voltages



Test circuit for $V_{CEOsust}$

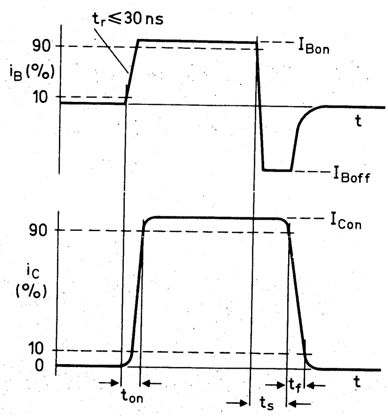


Test circuit for V_{ERsust}

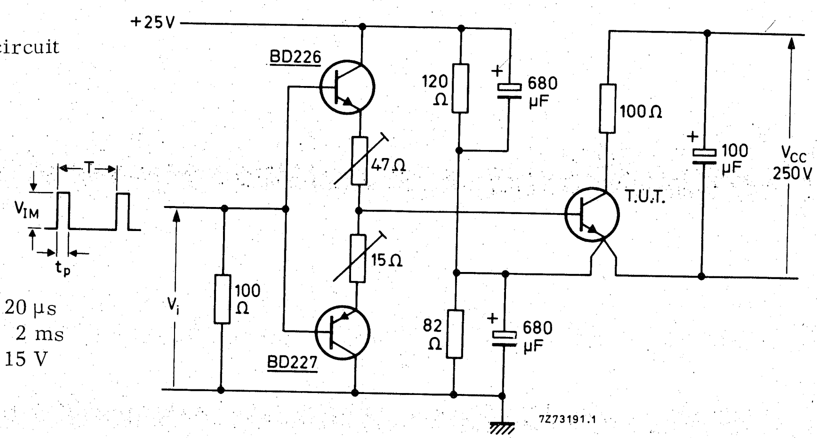
CHARACTERISTICS (continued) T_j = 25 °C unless otherwise specified

Transition frequency at f = 1 MHz				
I_C = 0,2 A; V_{CE} = 10 V	f_T	typ.	6	MHz
Switching times				
I_{Con} = 2,5 A; V_{CC} = 250 V				
I_{Bon} = 0,5 A; $-I_{Boff}$ = 1 A				
Turn-on time	t_{on}	typ.	0,3	μs
		<	0,5	μs
Turn-off: Storage time	t_s	typ.	2	μs
		<	3,5	μs
Fall time	t_f	typ.	0,3	μs
Fall time, T_{mb} = 95 °C	t_f	<	1	μs

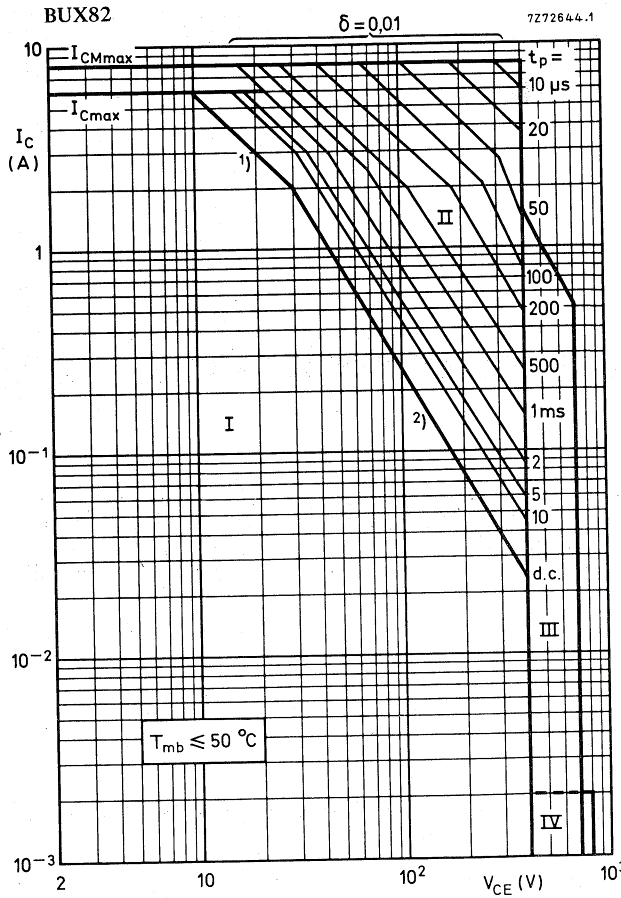
Waveform



Test circuit



t_p = 20 μs
T = 2 ms
V_{IM} = 15 V



Safe Operating ARea

I Region of permissible d.c. operation

II Permissible extension for repetitive pulse operation

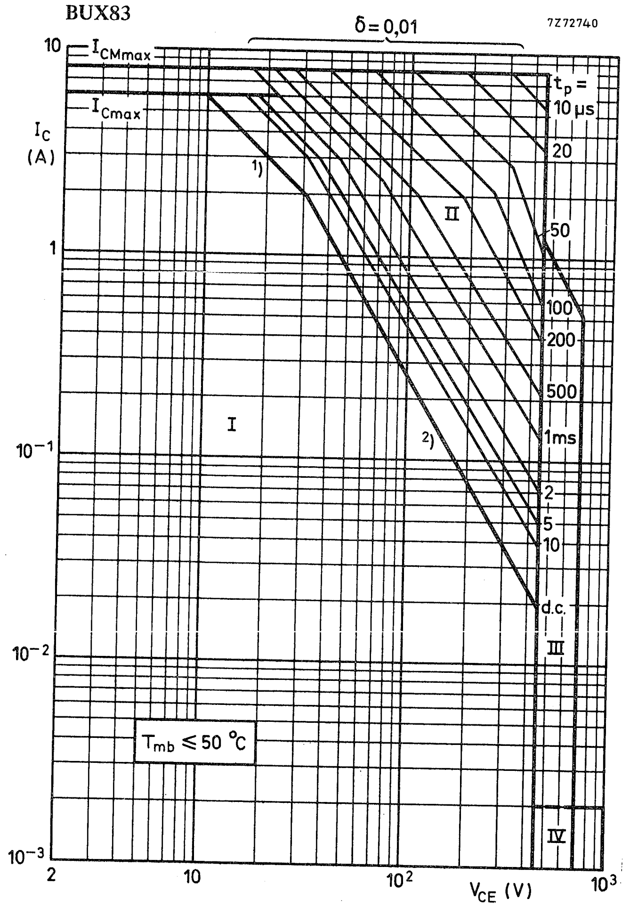
III Area of permissible operation during turn-on in single-transistor converters, provided $R_{BE} \leq 100\ \Omega$ and $t_p \leq 0,6\ \mu s$

IV Repetitive pulse operation in this region is permissible, provided $V_{BE} \leq 0$ and $t_p \leq 2$ ms

---

1) $P_{tot\,max}$ and $P_{peak\,max}$ lines.

2) Second-breakdown limits (independent of temperature).



Safe Operating ARea

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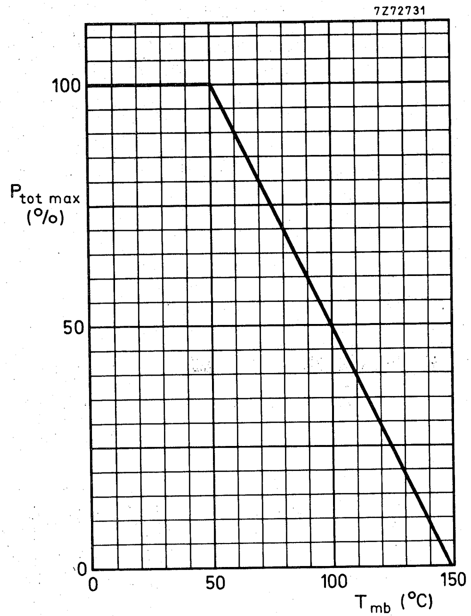
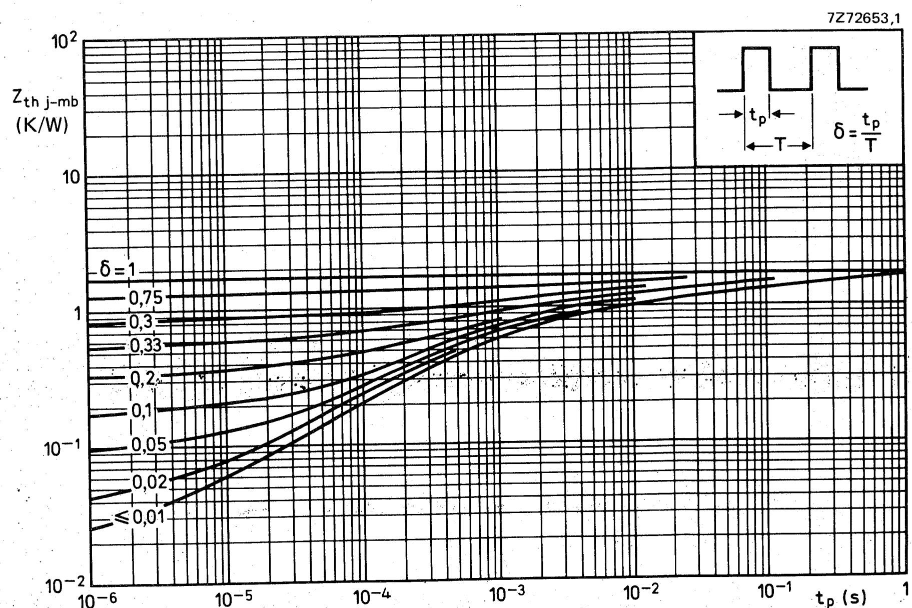
IV Repetitive pulse operation in this region is permissible, provided $V_{BE} \leq 0$ and $t_p \leq 2$ ms

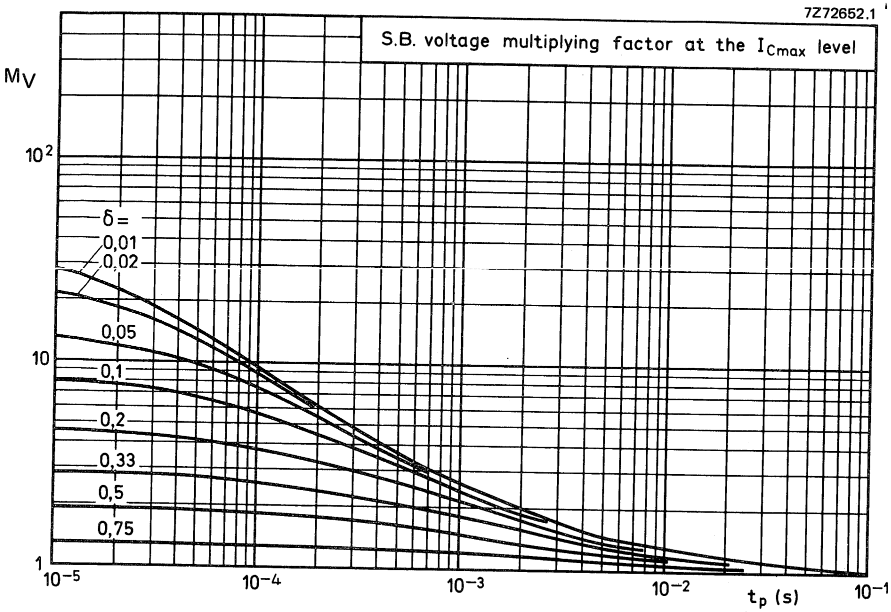
---

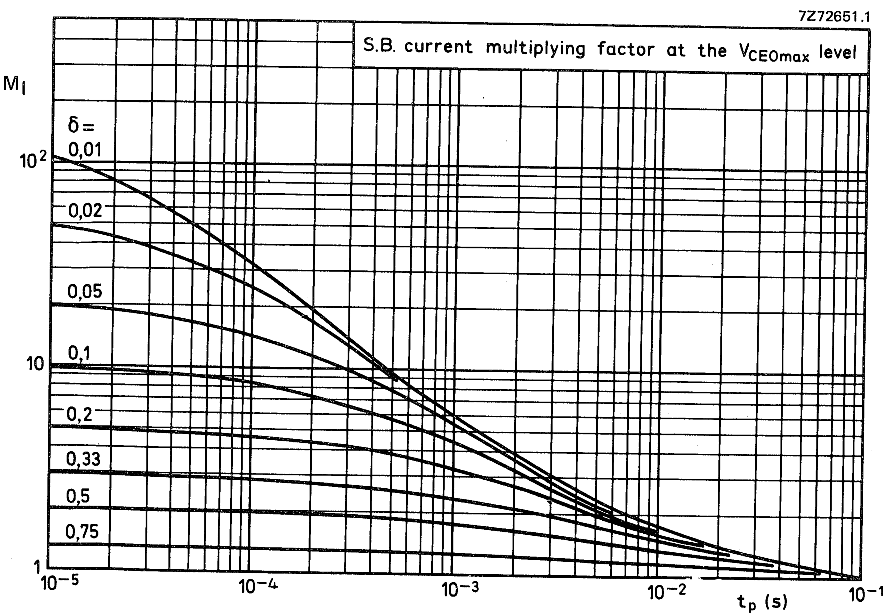
1) $P_{tot\ max}$ and $P_{peak\ max}$ lines.

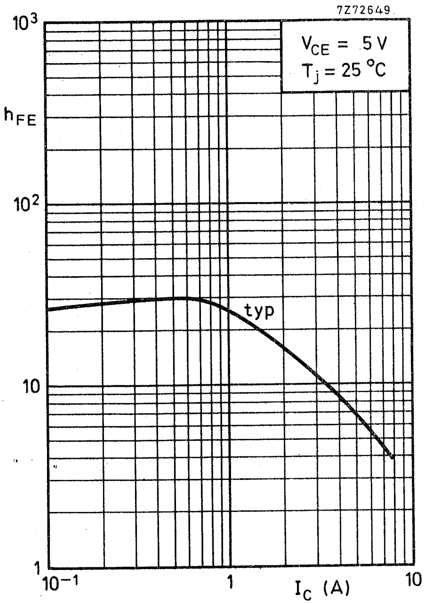
2) Second-breakdown limits (independent of temperature).

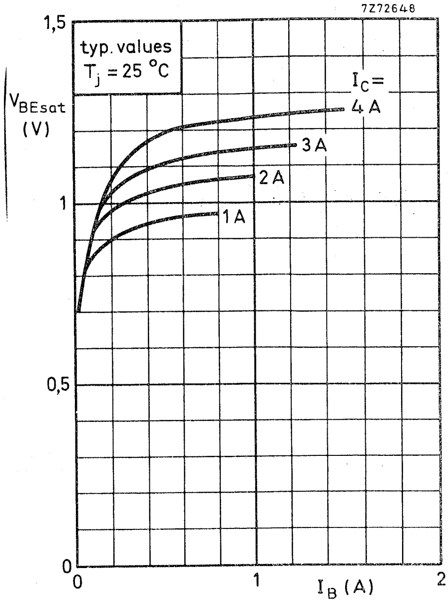

7Z72731
100
$P_{tot\ max}$ (%)
50
0
0
50
100
150
T_{mb} (°C)

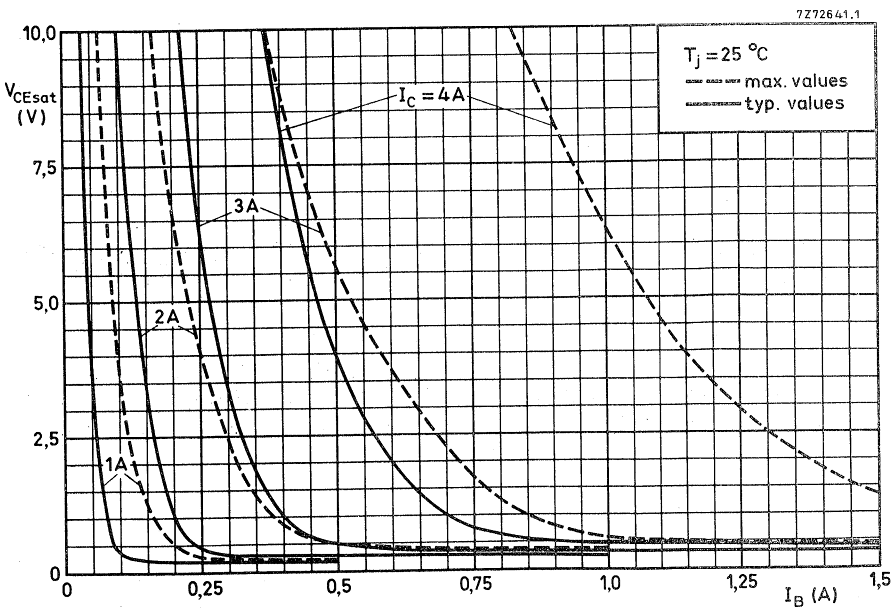

7Z72653.1
10^2
$Z_{th\ j\text{-}mb}$ (K/W)
10
1
10^{-1}
10^{-2}
$\delta = 1$
0,75
0,5
0,33
0,2
0,1
0,05
0,02
≤ 0,01
t_p
T
$\delta = \frac{t_p}{T}$
10^{-6}
10^{-5}
10^{-4}
10^{-3}
10^{-2}
10^{-1}
1
t_p (s)


7Z72652.1
S.B. voltage multiplying factor at the I_{Cmax} level
M_V
10^2
10
1
δ =
0,01
0,02
0,05
0,1
0,2
0,33
0,5
0,75
10^{-5}
10^{-4}
10^{-3}
10^{-2}
t_p (s)
10^{-1}


7Z72651.1
S.B. current multiplying factor at the V_{CEOmax} level
M_I
10^2
10
1
δ =
0,01
0,02
0,05
0,1
0,2
0,33
0,5
0,75
10^{-5}
10^{-4}
10^{-3}
10^{-2}
t_p (s)
10^{-1}


7Z72649
V_{CE} = 5 V
T_j = 25 °C
h_{FE}
10^3
10^2
10
1
typ
10^{-1}
1
10
I_C (A)


7Z72648
typ. values
T_j = 25 °C
V_{BEsat}
(V)
1,5
1
0,5
0
I_C =
4 A
3 A
2 A
1 A
0
1
2
I_B (A)


7Z72641.1
T_j = 25 °C
max. values
typ. values
V_{CEsat}
(V)
10,0
7,5
5,0
2,5
0
I_C = 4 A
3 A
2 A
1 A
0
0,25
0,5
0,75
1,0
1,25
1,5
I_B (A)

APPLICATION INFORMATION ON BUX82 (detailed information on request)

Important factors in the design of SMPS circuits are the power losses and heatsink requirements of the supply output transistor and the base drive conditions during turn-off. In SMPS circuits with mains isolation the duty factor of the collector current generally varies between 0,25 and 0,5.

The operating frequency lies between 15 kHz and 50 kHz and the shape of the collector current varies from rectangular in a forward converter to a sawtooth in a flyback circuit.

Information on optimum base drive and device dissipation of the BUX82 in a flyback converter is given in Figs 3 to 5. Figs 6 to 8 apply to a forward converter. In these figures I_{CM} represents the highest repetitive peak collector current that can occur in the given circuit, e.g. during overload.

The total power dissipation for a limit-case transistor is given in Figs 5 and 8 which applies for a mounting base temperature of 100 °C. The required thermal resistance for the heatsink can be calculated from

$$R_{th\ mb\text{-}a} = \frac{100 - T_{amb\ max}}{P_{tot}}.$$

To ensure thermal stability the minimum value of T_{amb} in the above equation is 40 °C.

A practical forward converter output circuit for an output power in the order of 200 W is given in Fig. 2.

At a collector current of 2,5 A and a base current of 0,5 A in this circuit the following turn-off times can be expected.

			T_{mb} = 25 °C	100 °C	
Storage time	t_s	typ	1,9	2,7	μs
Fall time	t_f	typ	0,17	0,7	μs

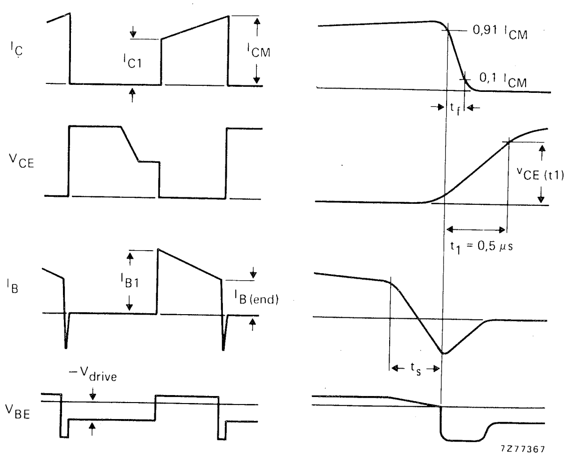


Fig. 1 Relevant waveforms of switching transistor.

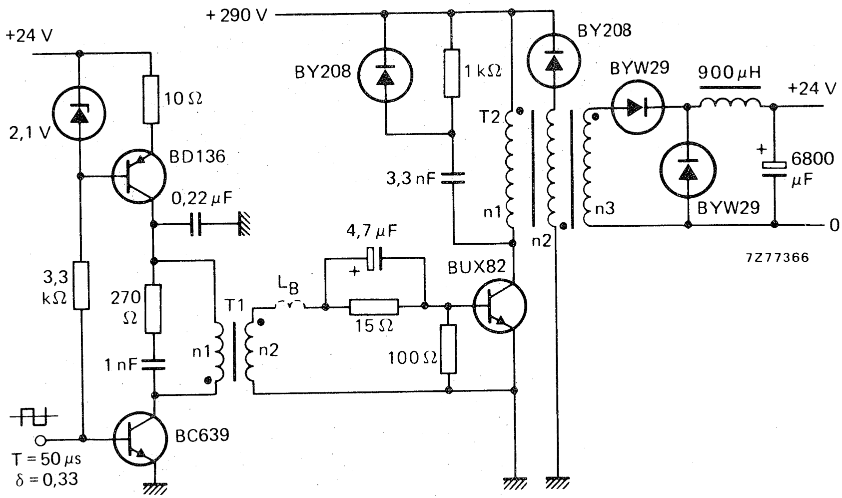


Fig. 2 Practical forward converter SMPS output circuit.

T1 (driver transformer): Core U20; n1 = 75 turns; n2 = 20 turns

T2 (output transformer): Core E55; n1 = n2 = 72 turns; n3 = 19 turns

$V_{CE(t1)} < 300$ V (see Fig. 1)

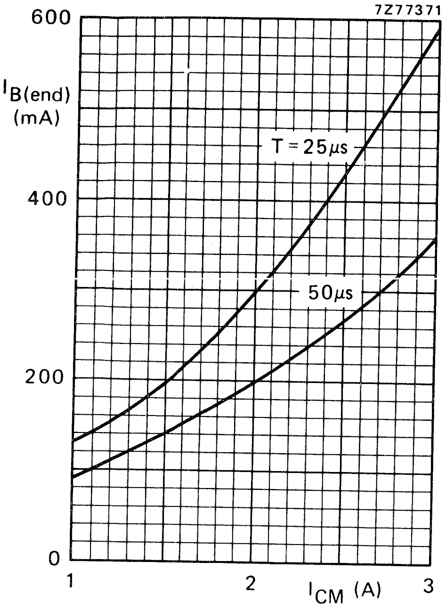


Fig. 3.

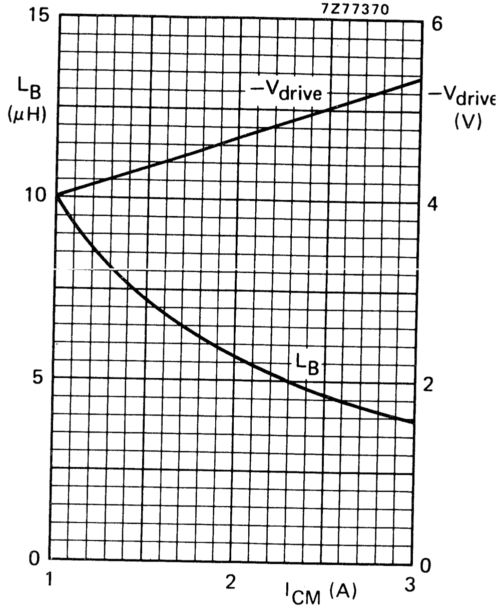


Fig. 4.

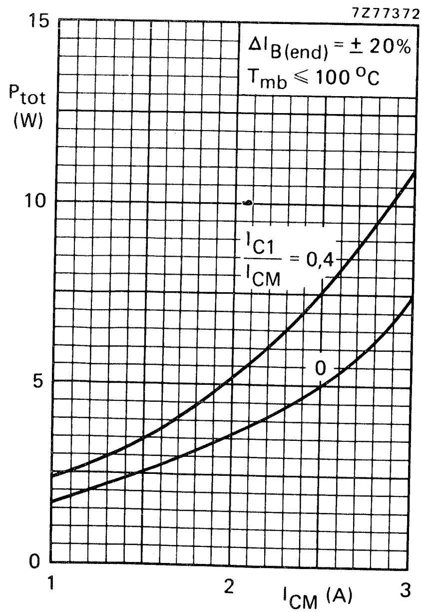


Fig. 5.

Fig. 3 Recommended nominal "end" value of the base current versus maximum peak collector current in a **flyback** converter.

Fig. 4 Minimum required base inductance and recommended negative drive voltage versus maximum peak collector current.

Fig. 5 Maximum total power dissipation of a limit-case transistor if the base current is chosen in accordance with Fig. 3.

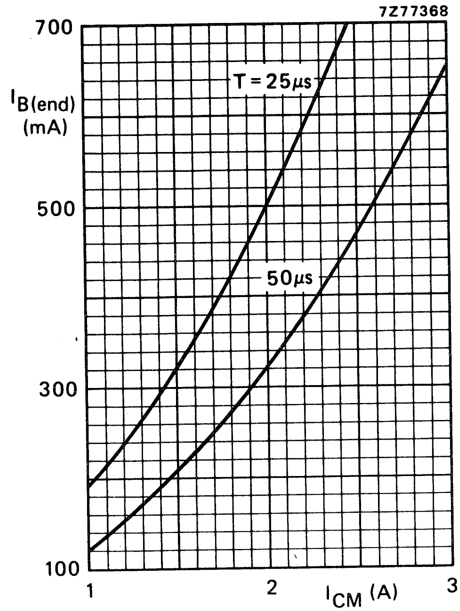


Fig. 6.

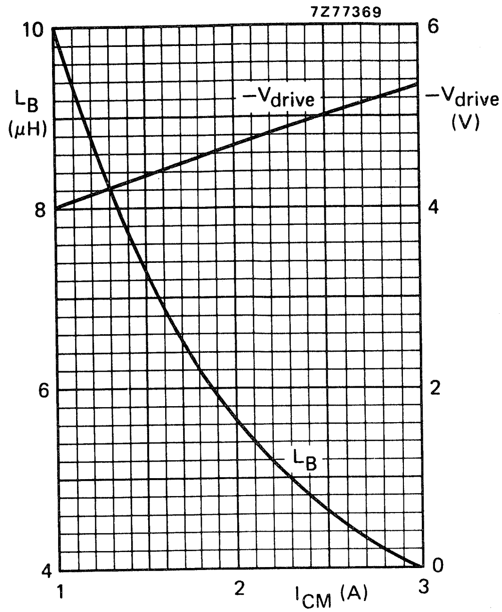


Fig. 7.

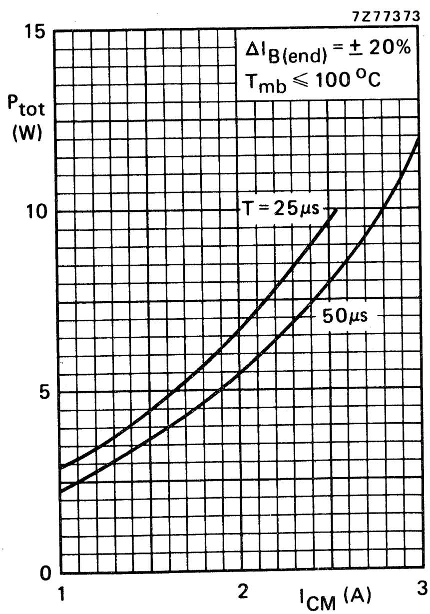


Fig. 8.

Fig. 6 Recommended nominal "end" value of the base current versus maximum peak collector current in a **forward** converter.

Fig. 7 Minimum required base inductance and recommended negative drive voltage versus maximum peak collector current.

Fig. 8 Maximum total power dissipation of a limit-case transistor if the base current is chosen in accordance with Fig. 6.

SILICON DIFFUSED POWER TRANSISTORS

High-voltage, high-speed, glass-passivated n-p-n power transistors in TO-220 envelopes, intended for use in converters, inverters, switching regulators, motor control systems and switching applications.

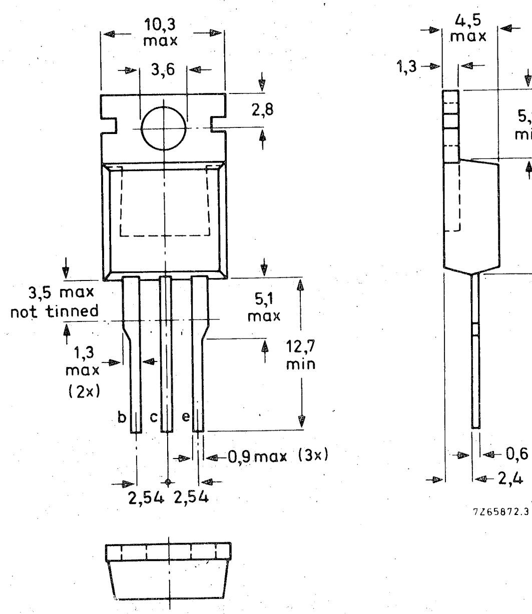
QUICK REFERENCE DATA

			BUX84	BUX85	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max	800	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max	400	450	V
Collector current (d.c.)	I_C	max	2		A
Collector current (peak value) t_p = 2 ms	I_{CM}	max	3		A
Total power dissipation up to T_{mb} = 50 °C	P_{tot}	max	40		W
Collector-emitter saturation voltage I_C = 1 A; I_B = 0,2 A	V_{CEsat}	<	1		V
Fall time I_{Con} = 1 A; I_{Bon} = 0,2 A; $-I_{Boff}$ = 0,4 A	t_f	typ	0,4		μs

MECHANICAL DATA

Dimensions in mm

TO-220
Collector connected to mounting base



See also chapters Mounting Instructions and Accessories.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

			BUX84	BUX85	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max	800	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max	400	450	V

Currents

Collector current (d.c.)	I_C	max	2	A
Collector current (peak value) t_p = 2 ms	I_{CM}	max	3	A
Base current (d.c.)	I_B	max	0,75	A
Base current (peak value)	I_{BM}	max	1	A
Reverse base current (peak value) *	$-I_{BM}$	max	1	A

Power dissipation

Total power dissipation up to T_{mb} = 50 °C	P_{tot}	max	40	W

Temperatures

Storage temperature	T_{stg}		−65 to +150	°C
Junction temperature	T_j	max	150	°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	2,5	K/W
From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	70	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current **

$V_{CEM} = V_{CESMmax}$; $V_{BE} = 0$	I_{CES}	<	200	μA
$V_{CEM} = V_{CESMmax}$; $V_{BE} = 0$; T_j = 125 °C	I_{CES}	<	1,5	mA

D.C. current gain

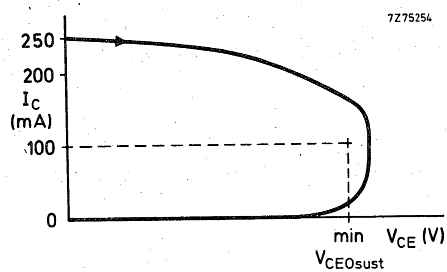
I_C = 0,1 A; V_{CE} = 5 V	h_{FE}	typ	50	

* Turn-off current.
** Measured with a half sine-wave voltage (curve tracer).

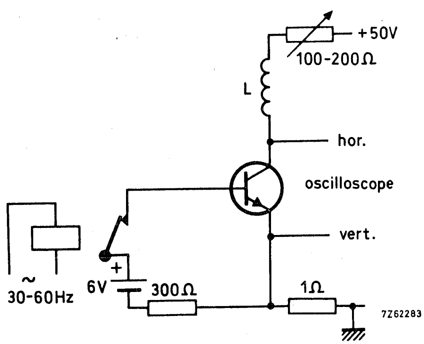
CHARACTERISTICS (continued)

T_j = 25 °C unless otherwise specified

Emitter cut-off current					
$I_C = 0$; $V_{EB} = 5$ V	I_{EBO}	<	1		mA
Saturation voltages					
$I_C = 0,3$ A; $I_B = 30$ mA	V_{CEsat}	<	0,8		V
$I_C = 1$ A; $I_B = 0,2$ A	V_{CEsat}	<	1,0		V
$I_C = 1$ A; $I_B = 0,2$ A	V_{BEsat}	<	1,1		V
Collector-emitter sustaining voltage			BUX84	BUX85	
$I_C = 100$ mA; $I_{Boff} = 0$; L = 25 mH	$V_{CEOsust}$	>	400	450	V



Oscilloscope display for sustaining voltage.



Test circuit for $V_{CEOsust}$.

CHARACTERISTICS (continued) $T_j = 25\ ^oC$ unless otherwise specified

Transition frequency at f = 1 MHz

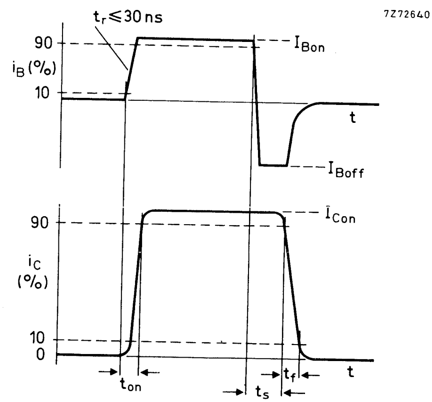
$I_C = 0{,}2$ A; $V_{CE} = 10$ V	f_T	typ	20	MHz

Switching times

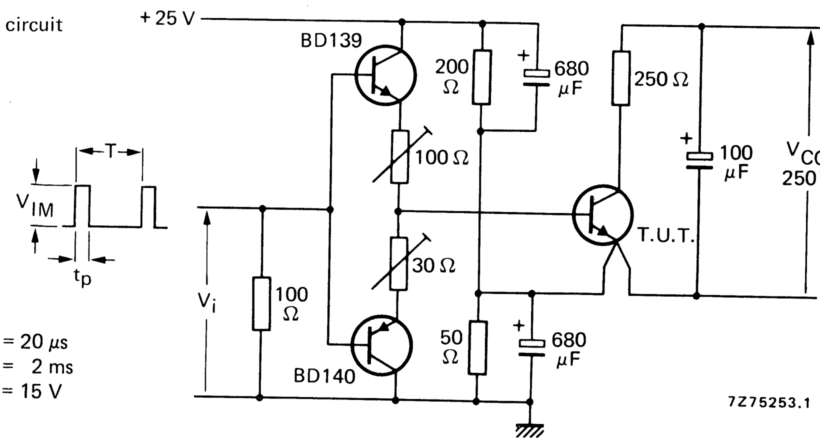
$I_{Con} = 1$ A; $V_{CC} = 250$ V
$I_{Bon} = 0{,}2$ A; $-I_{Boff} = 0{,}4$ A

Turn-on time	t_{on}	typ	0,2	μs
		<	0,5	μs
Turn-off: Storage time	t_s	typ	2	μs
		<	3,5	μs
Fall time	t_f	typ	0,4	μs
Fall time, $T_{mb} = 95\ ^oC$	t_f	<	1,4	μs

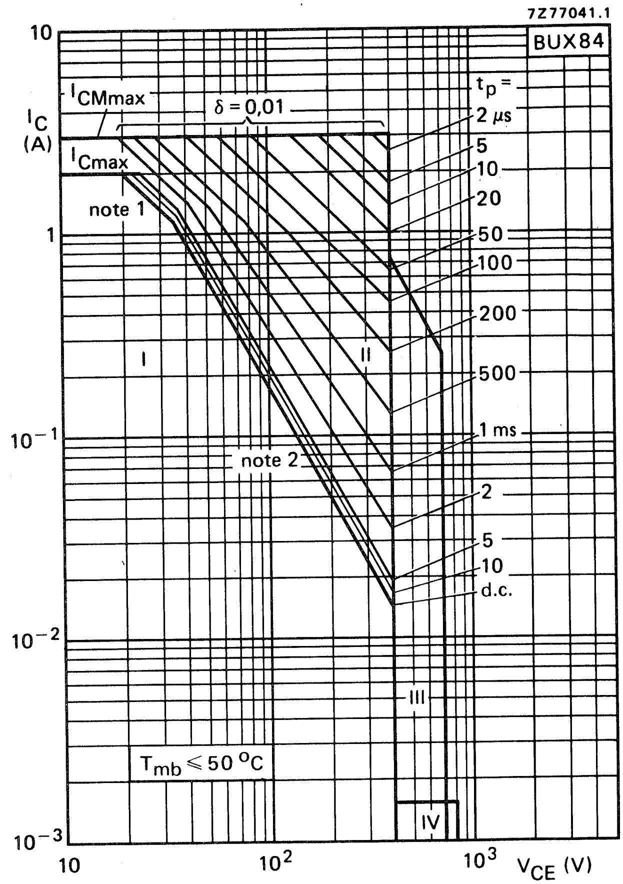
Waveform



Test circuit



$t_p = 20\ \mu s$
$T = 2$ ms
$V_{IM} = 15$ V



Safe Operating ARea

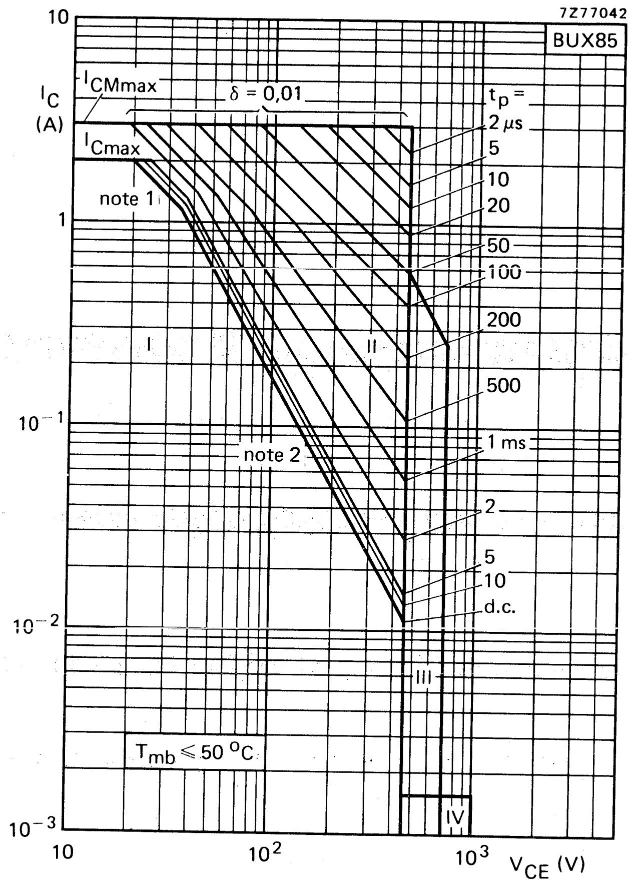
I Region of permissible d.c. operation

II Permissible extension for repetitive pulse operation

III Area of permissible operation during turn-on in single transistor converters, provided $R_{BE} \leqslant 100\ \Omega$ and $t_p \leqslant 0,6\ \mu s$

IV Repetitive pulse operation in this region is permissible, provided $V_{BE} \leqslant 0$ and $t_p \leqslant 2$ ms

Notes
1. $P_{tot\ max}$ and $P_{peak\ max}$ lines.
2. Second-breakdown limits (independent of temperature).



Safe Operating ARea

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Notes
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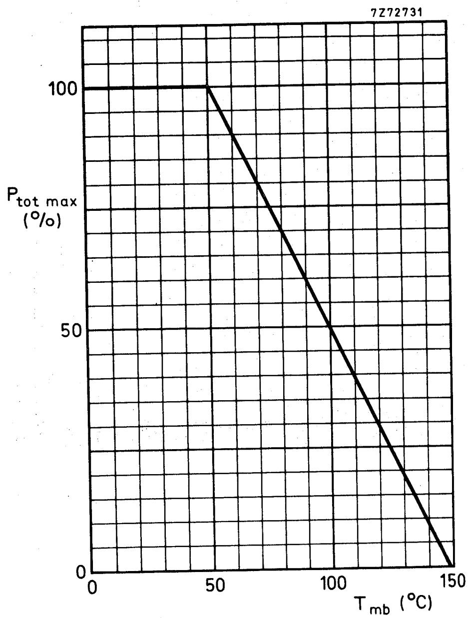
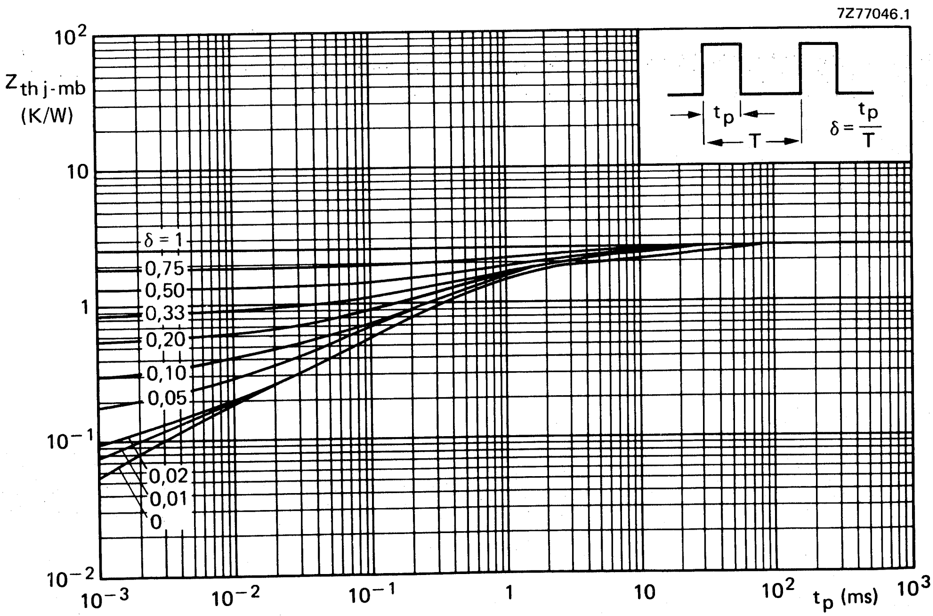
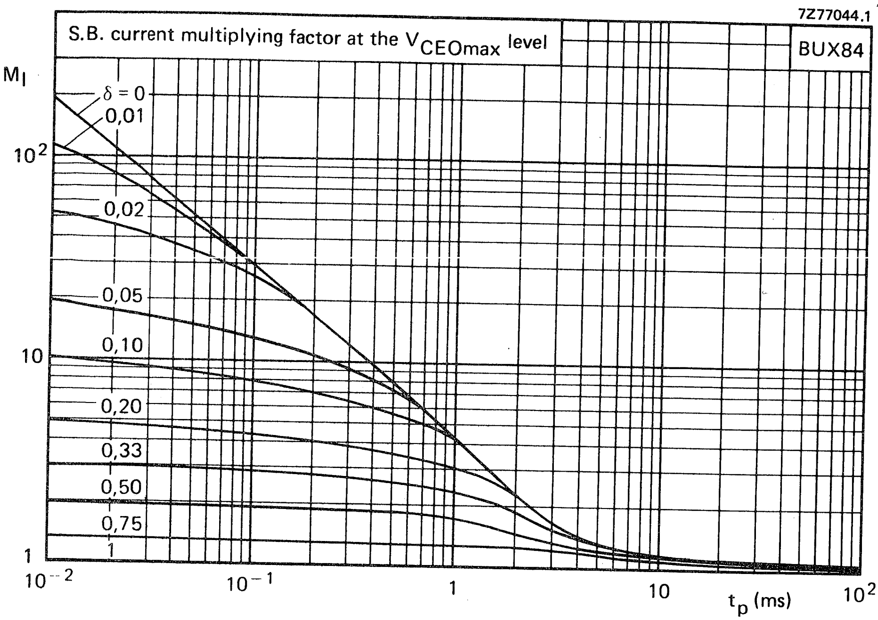
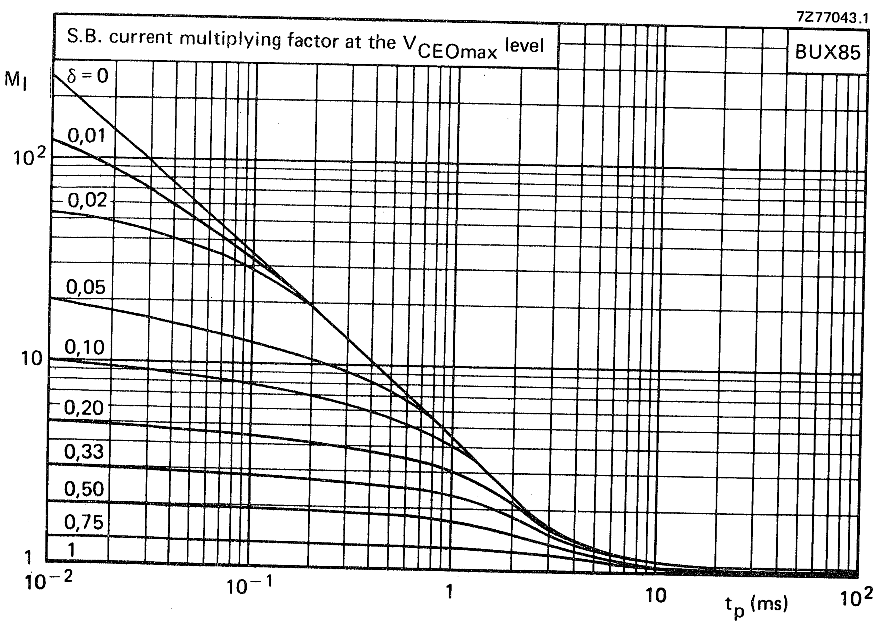
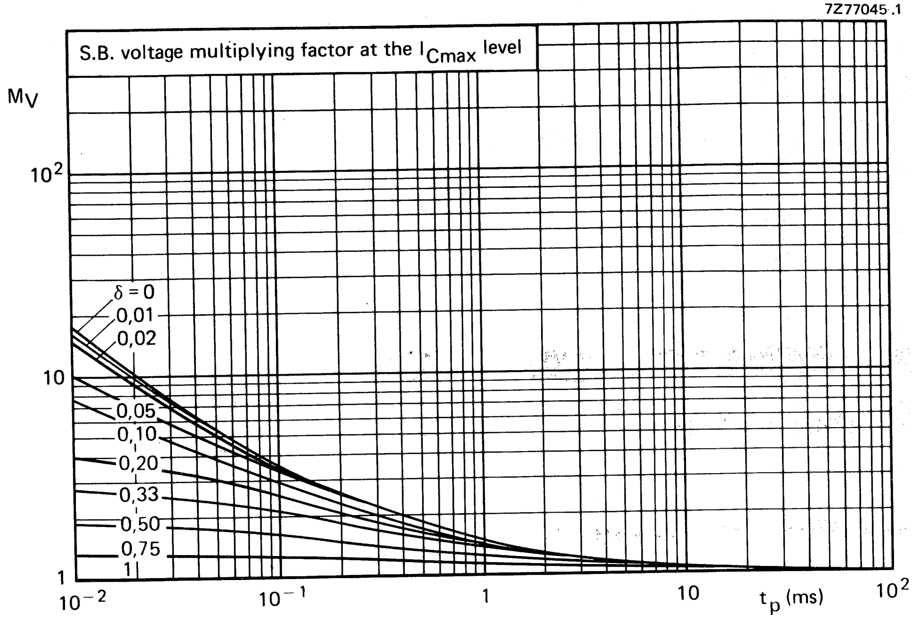
2. Second-breakdown limits (independent of temperature).

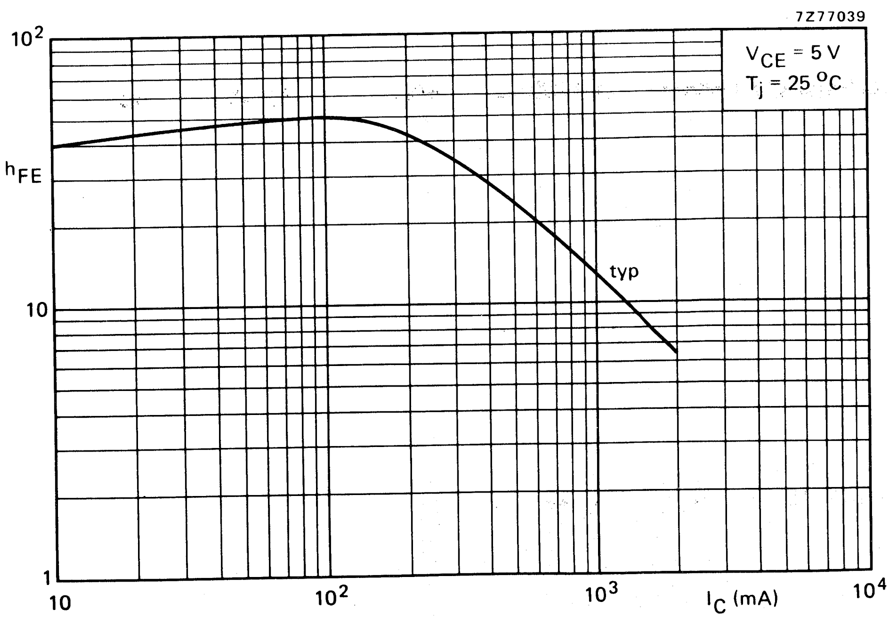

7Z72731
$P_{tot\ max}$ (%)
100
50
0
0
50
100
150
T_{mb} (°C)


7Z77046.1
$Z_{th\ j\text{-}mb}$ (K/W)
10^2
10
1
10^{-1}
10^{-2}
δ = 1
0,75
0,50
0,33
0,20
0,10
0,05
0,02
0,01
0
t_p
T
$\delta = \frac{t_p}{T}$
10^{-3}
10^{-2}
10^{-1}
1
10
10^2
t_p (ms)
10^3


7Z77044.1
S.B. current multiplying factor at the V_{CEOmax} level
BUX84
M_I
δ = 0
0,01
0,02
0,05
0,10
0,20
0,33
0,50
0,75
1
10^2
10
1
10^{-2}
10^{-1}
1
10
10^2
t_p (ms)


7Z77043.1
S.B. current multiplying factor at the V_{CEOmax} level
BUX85
M_I
δ = 0
0,01
0,02
0,05
0,10
0,20
0,33
0,50
0,75
1
10^2
10
1
10^{-2}
10^{-1}
1
10
10^2
t_p (ms)


7Z77045.1
S.B. voltage multiplying factor at the I_Cmax level
M_V
10^2
10
1
δ = 0
0,01
0,02
0,05
0,10
0,20
0,33
0,50
0,75
1
10^−2
10^−1
1
10
t_p (ms)
10^2


7Z77039
V_CE = 5 V
T_j = 25 °C
10^2
h_FE
10
1
typ
10
10^2
10^3
I_C (mA)
10^4

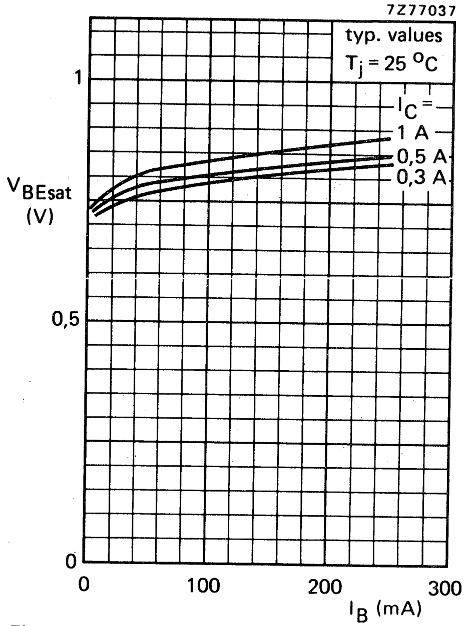


Fig. 14 Typical values saturation voltage, $T_j = 25\ ^oC$.

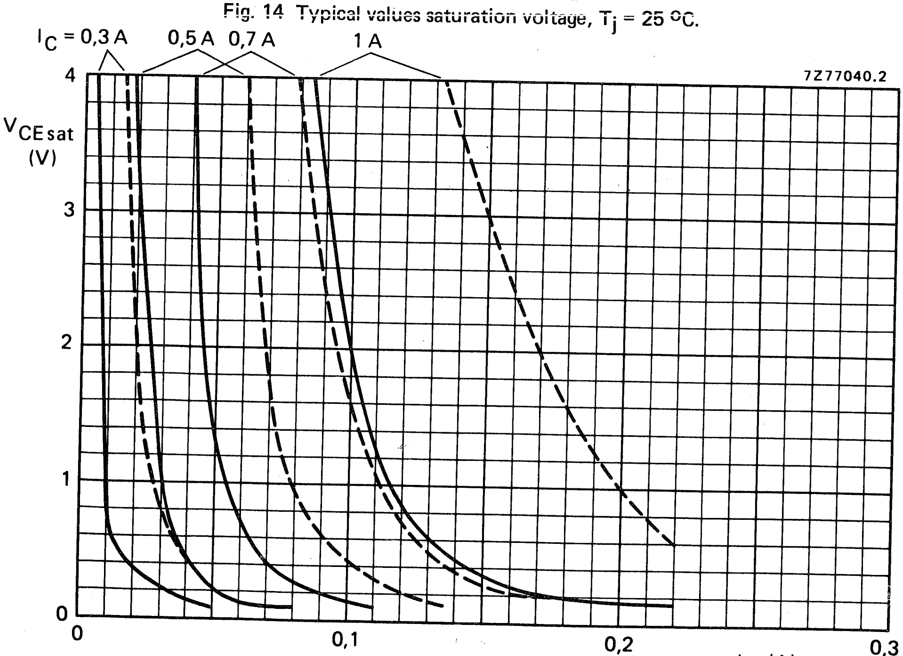


Fig. 15 Typical (——) and maximum (– – –) values saturation voltage at $T_j = 25\ ^oC$.

APPLICATION INFORMATION ON BUX84 (detailed information on request)

Important factors in the design of SMPS circuits are the power losses and heatsink requirements of the supply output transistor and the base drive conditions during turn-off. In most SMPS circuits with mains isolation the duty factor of the collector current generally varies between 0,25 and 0,5.

The operating frequency lies between 15 kHz and 50 kHz and the shape of the collector current varies from rectangular in a forward converter to a sawtooth in a flyback circuit.

Information on optimum base drive and device dissipation of the BUX84 in a flyback converter is given in Figs 3 to 5. Figs 6 to 8 apply to a forward converter. In these figures I_{CM} represents the highest repetitive peak collector current that can occur in the given circuit, e.g. during overload.

The total power dissipation for a limit-case transistor is given in Figs 5 and 8 which apply for a mounting base temperature of 100 °C. The required thermal resistance for the heatsink can be calculated from

$$R_{th\ mb\text{-}a} = \frac{100 - T_{amb\ max}}{P_{tot}}.$$

To ensure thermal stability the minimum value of T_{amb} in the above equation is 40 °C.

A practical SMPS output circuit for an output power in the order of 50 W is given in Fig. 2.

At a collector current of 0,7 A and a base current of 70 mA in this circuit the following turn-off times can be expected.

			T_{mb} = 25 °C	100 °C	
Storage time	t_s	typ	2,2	2,8	μs
Fall time	t_f	typ	0,25	0,85	μs

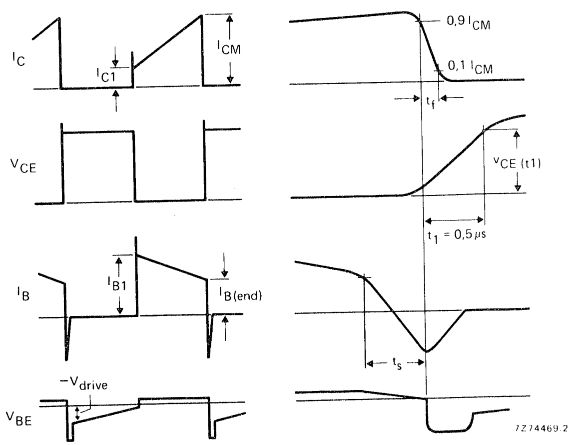


Fig. 1 Relevant waveforms of switching transistor.

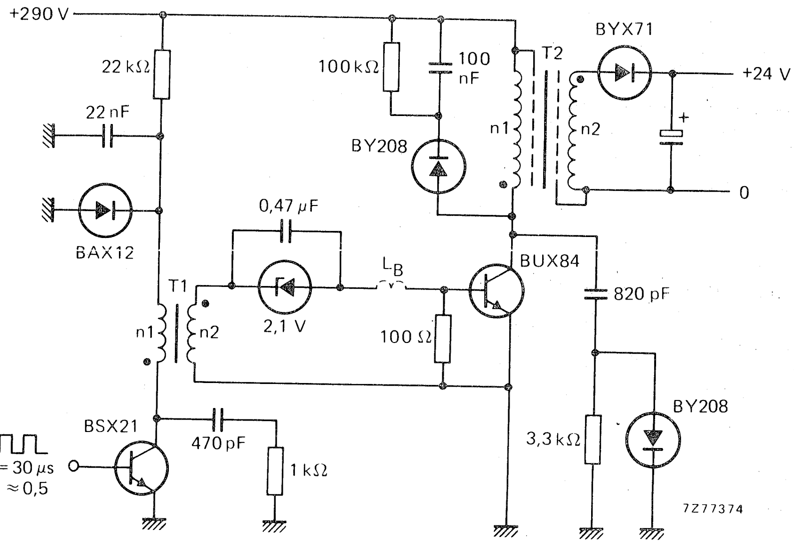


Fig. 2 Practical SMPS output circuit.

T1 (driver transformer): Core U15; n1 = 360 turns; n2 = 60 turns
total inductance in base circuit ≈ 15 µH

T2 (output transformer): Core E55; primary inductance L_p = 16 mH
n1 = 116 turns; n2 = 12 turns

$v_{CE(t1)}$ < 300 V (see Fig. 1)

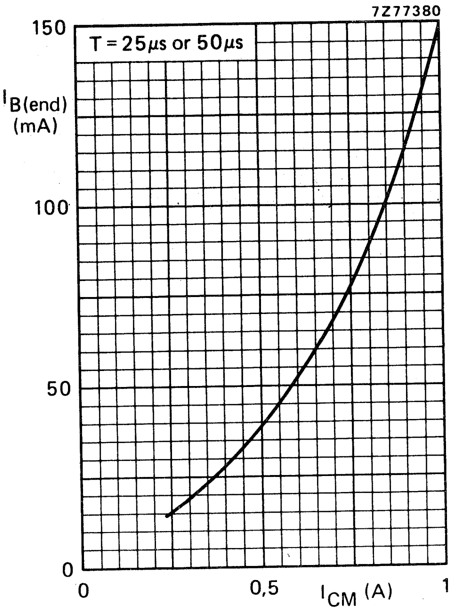


Fig. 3.

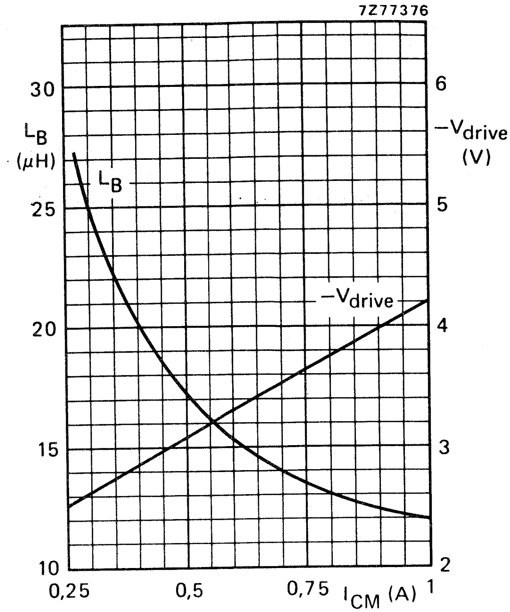


Fig. 4.

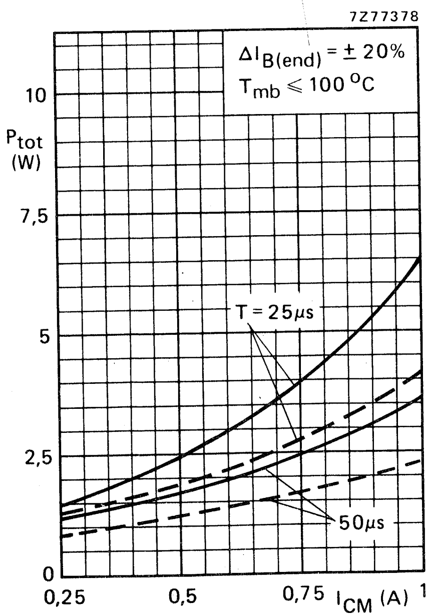


Fig. 5.

Fig. 3 Recommended nominal "end" value of the base current versus maximum peak collector current in a **flyback** converter.

Fig. 4 Minimum required base inductance and recommended negative drive voltage versus maximum peak collector current.

Fig. 5 Maximum total power dissipation of a limit-case transistor if the base current is chosen in accordance with Fig. 3. Solid lines for I_{C1}/I_{CM} = 0,4 and dotted lines for I_{C1}/I_{CM} = 0.

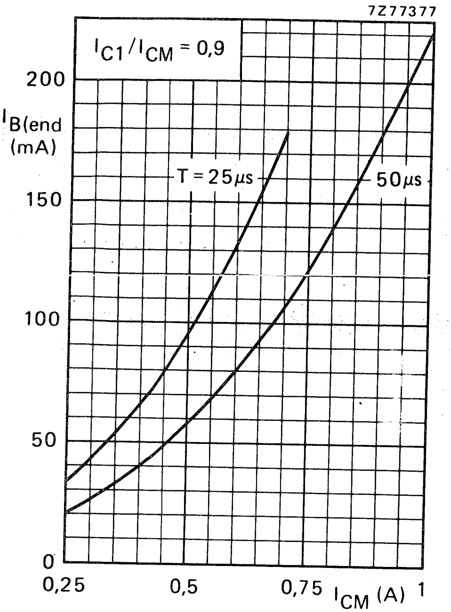


Fig. 6.

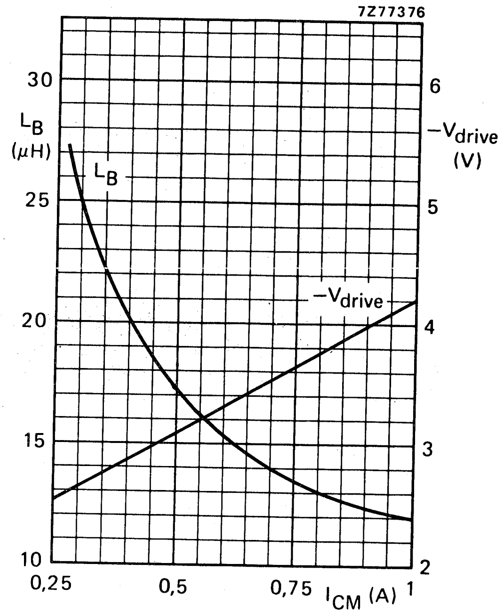


Fig. 7.

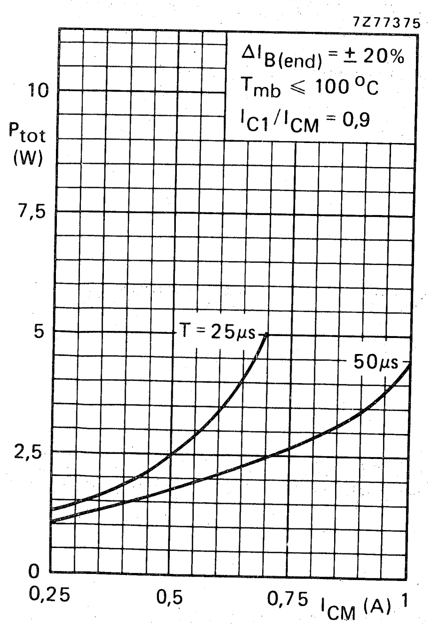


Fig. 8.

Fig. 6 Recommended nominal "end" value of the base current versus maximum peak collector current in a **forward** converter.

Fig. 7 Minimum required base inductance and recommended negative drive voltage versus maximum peak collector current.

Fig. 8 Maximum total power dissipation of a limit-case transistor if the base current is chosen in accordance with Fig. 6.

SILICON DIFFUSED POWER TRANSISTORS

High-voltage, high-speed, glass-passivated n-p-n power transistors in SOT-32 envelopes, for use in converters, inverters, switching regulators, motor control systems and switching applications.

QUICK REFERENCE DATA

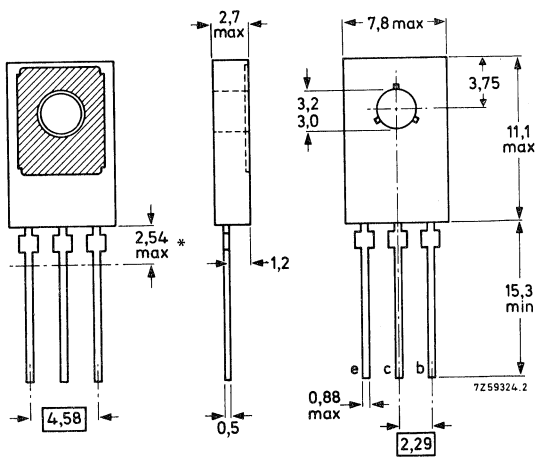
			BUX86	BUX87	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max	800	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max	400	450	V
Collector current (d.c.)	I_C	max	0,5		A
Collector current (peak value): t_p = 2 ms	I_{CM}	max	1		A
Total power dissipation up to T_{mb} = 60 °C	P_{tot}	max	20		W
Collector-emitter saturation voltage: I_C = 0,2 A; I_B = 20 mA	V_{CEsat}	<	1		V
Fall time: I_{Con} = 0,2 A; I_{Bon} = 20 mA; $-I_{Boff}$ = 40 mA	t_f	typ	0,4		μs

MECHANICAL DATA

Dimensions in mm

TO-126 (SOT-32)

Collector connected to metal part of mounting surface



* Within this region the cross-section of the leads is uncontrolled.

See chapters Mounting Instructions and Accessories.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

			BUX86	BUX87	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	800	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
→ Emitter-base voltage (open collector)	V_{EBO}	max.	5	5	V

Currents

Collector current (d.c.)	I_C	max.	0,5	A
Collector current (peak value) t_p = 2 ms	I_{CM}	max.	1	A
Base current (d.c.)	I_B	max.	0,2	A
Base current (peak value)	I_{BM}	max.	0,3	A
Reverse base current (peak value) (note 1)	$-I_{BM}$	max.	0,3	A

Power dissipation

Total power dissipation up to T_{mb} = 60 °C	P_{tot}	max.	20	W

Temperatures

Storage temperature	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	4,5	K/W
From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	100	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector-cut-off current (note 2)

$V_{CEM} = V_{CESMmax}$; $V_{BE} = 0$	I_{CES}	<	100	μA
$V_{CEM} = V_{CESMmax}$; $V_{BE} = 0$; T_j = 125 °C	I_{CES}	<	1	mA

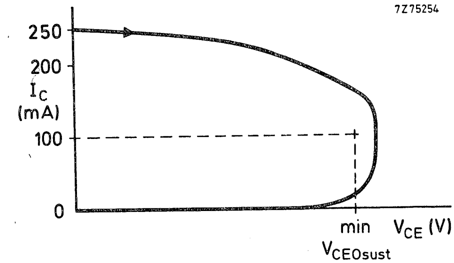
D.C. current gain

I_C = 50 mA; V_{CE} = 5 V	h_{FE}	typ.	50	

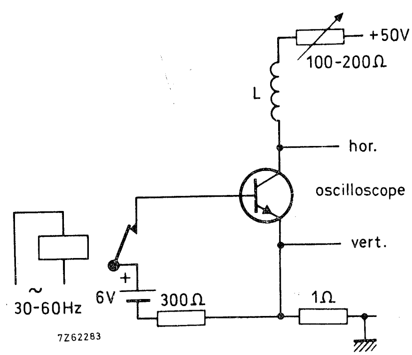
Notes
1. Turn-off current.
2. Measured with a half sine-wave voltage (curve tracer).

CHARACTERISTICS (continued) T_j = 25 °C unless otherwise specified

Emitter cut-off current					
$I_C = 0$; $V_{EB} = 5$ V	I_{EBO}	<	1		mA
Saturation voltage					
$I_C = 0{,}1$ A; $I_B = 10$ mA	V_{CEsat}	<	0,8		V ←
$I_C = 0{,}2$ A; $I_B = 20$ mA	V_{CEsat}	<	1,0		V ←
$I_C = 0{,}2$ A; $I_B = 20$ mA	V_{BEsat}	<	1,0		V
			BUX86	BUX87	
Collector-emitter sustaining voltages					
$I_C = 100$ mA; $I_{Boff} = 0$; L = 25 mH	$V_{CEOsust}$	>	400	450	V



Oscilloscope display for sustaining voltage

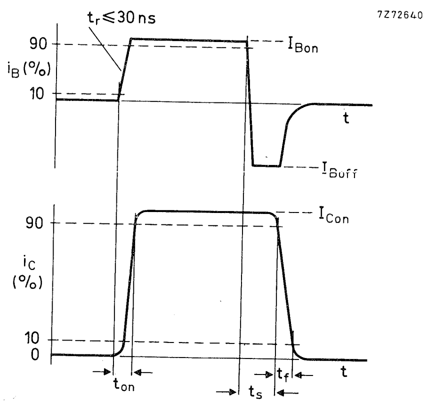


Test circuit for $V_{CEOsust}$

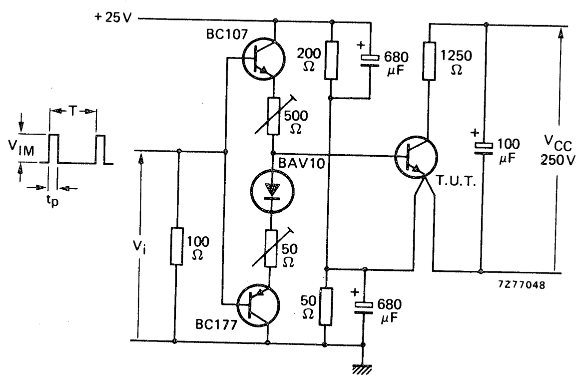
CHARACTERISTICS (continued) $T_j = 25\ ^oC$ unless otherwise specified

Transition frequency at f = 1 MHz				
$I_C = 50$ mA; $V_{CE} = 10$ V	f_T	typ	20	MHz
Switching times				
$I_{Con} = 0{,}2$ A; $V_{CC} = 250$ V				
$I_{Bon} = 20$ mA; $-I_{Boff} = 40$ mA				
Turn-on time	t_{on}	typ	0,25	μs
		$<$	0,5	μs
Turn-off: Storage time	t_s	typ	2	μs
		$<$	3,5	μs
Fall time	t_f	typ	0,4	μs
Fall time, $T_{mb} = 95\ ^oC$	t_f	$<$	1,3	μs

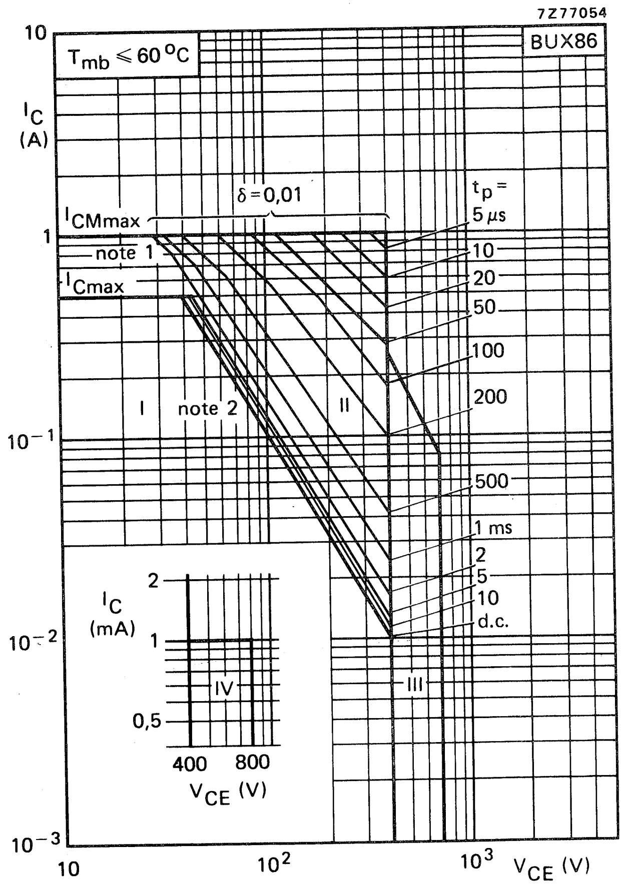
Waveform



Test circuit



$t_p = 20\ \mu s$
$T = 2$ ms
$V_{IM} = 15$ V



Safe Operating ARea

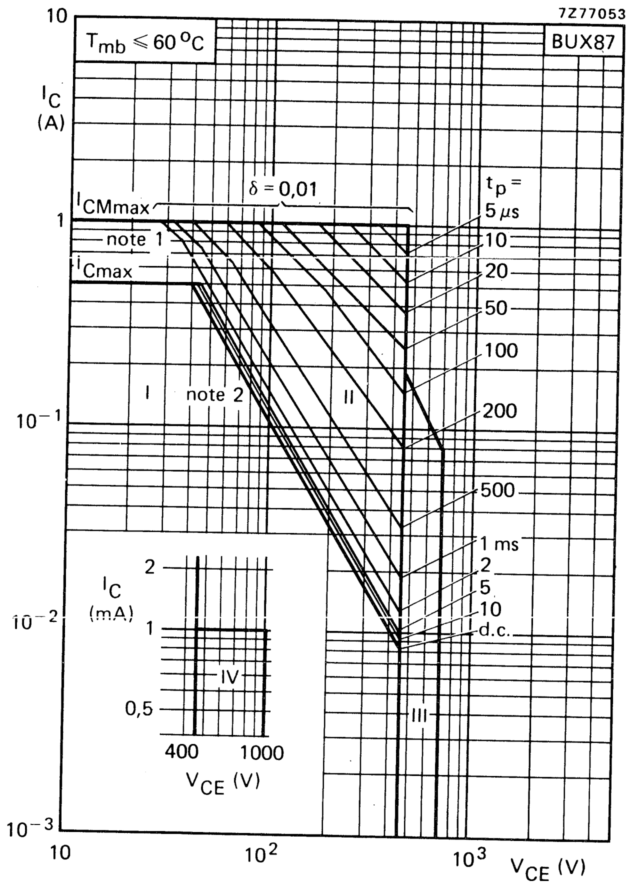
I Region of permissible d.c. operation

II Permissible extension for repetitive pulse operation

III Area of permissible operation during turn-on in single-transistor converters, provided $R_{BE} \leq 100\ \Omega$ and $t_p \leq 0{,}6\ \mu s$

IV Repetitive pulse operation in this region is permissible, provided $V_{BE} \leq 0$ and $t_p \leq 2$ ms

Notes
1. $P_{peak\ max}$ lines.
2. Second-breakdown limits (independent of temperature).



Safe Operating ARea

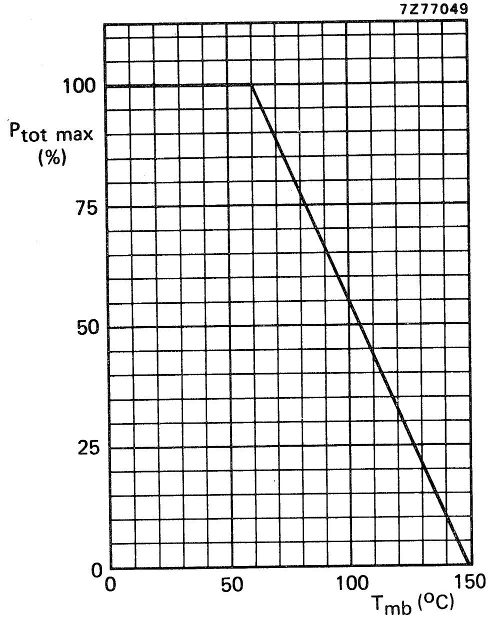
I Region of permissible d.c. operation

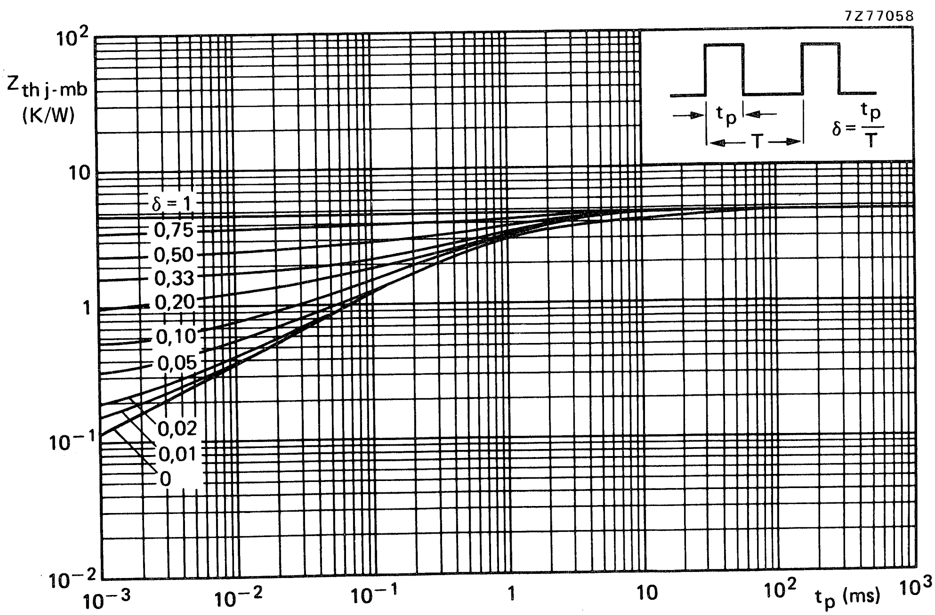
II Permissible extension for repetitive pulse operation

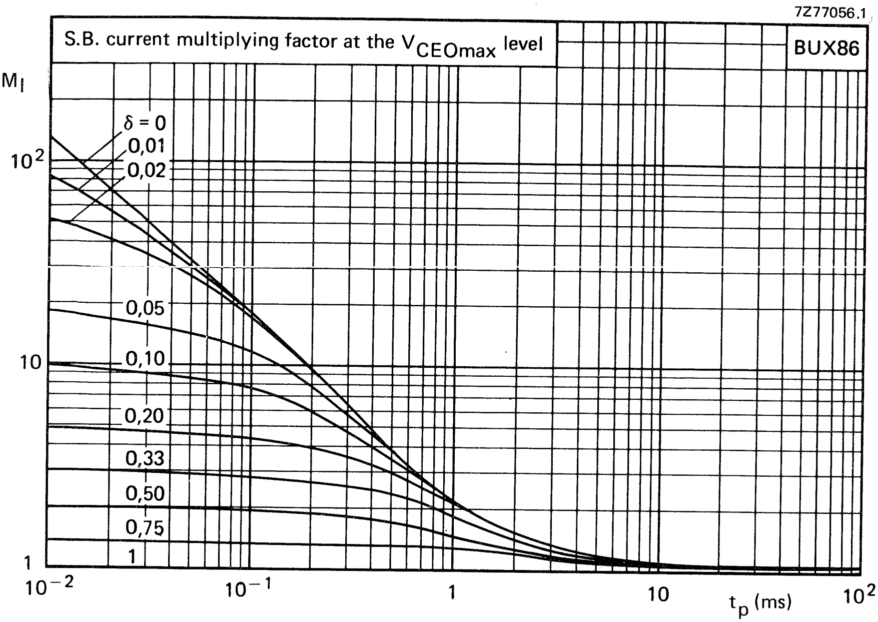
III Area of permissible operation during turn-on in single-transistor converters, provided $R_{BE} \leqslant 100\ \Omega$ an $t_p \leqslant 0{,}6\ \mu s$

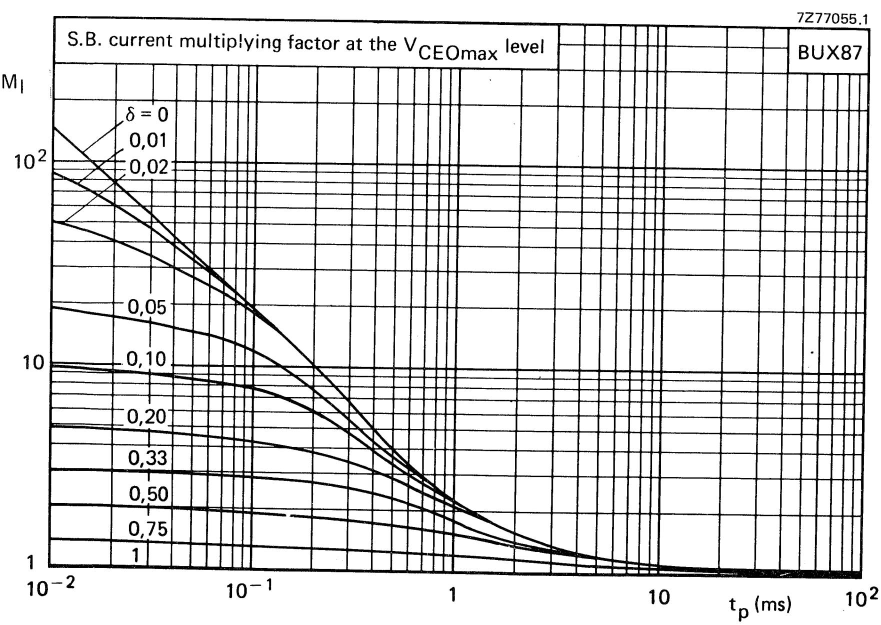
IV Repetitive pulse operation in this region is permissible, provided $V_{BE} \leqslant 0$ and $t_p \leqslant 2$ ms

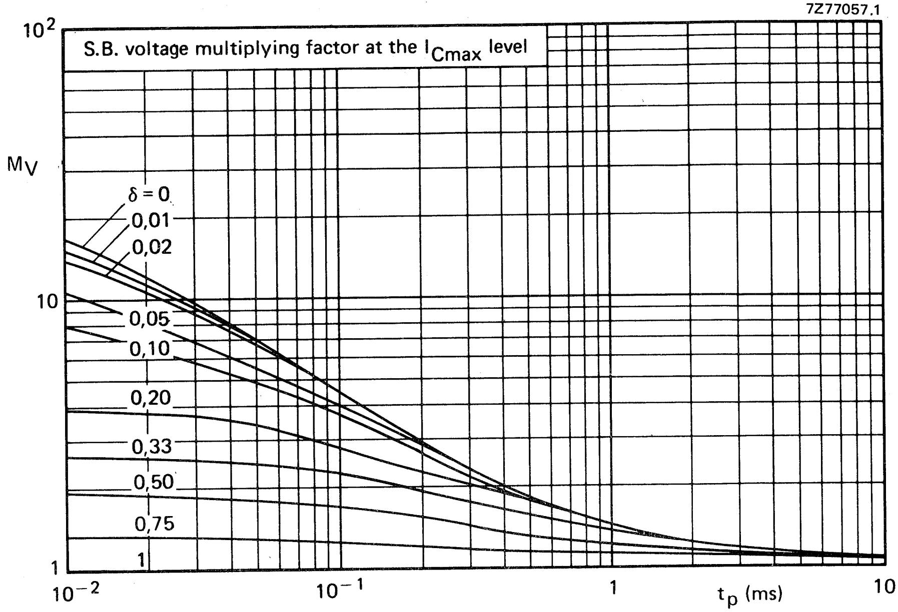
Notes
1. $P_{peak\ max}$ lines.
2. Second-breakdown limits (independent of temperature).

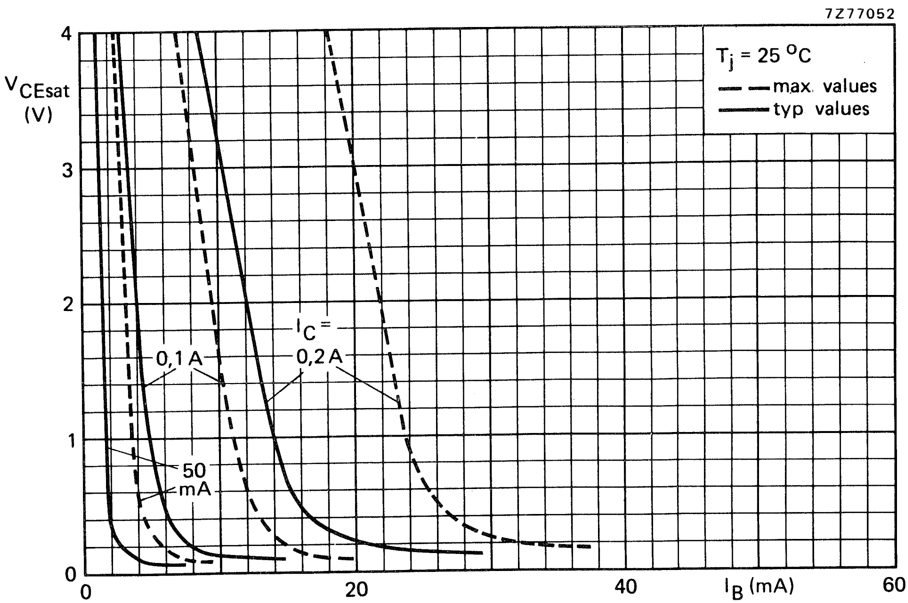

7Z77049
100
$P_{tot\ max}$
(%)
75
50
25
0
0
50
100
150
T_{mb} (°C)

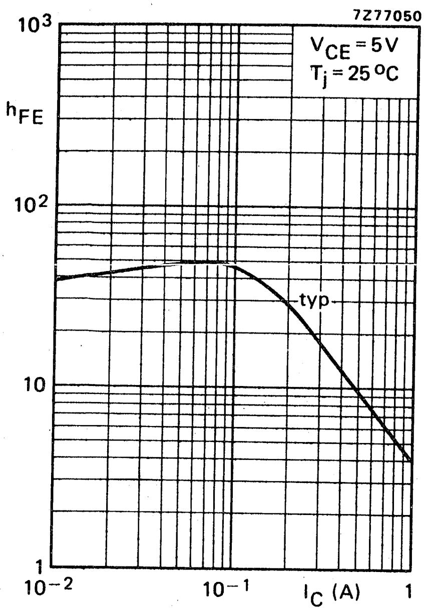

7Z77058
10^2
$Z_{th\ j\text{-}mb}$
(K/W)
10
1
10^{-1}
10^{-2}
$\delta = 1$
0,75
0,50
0,33
0,20
0,10
0,05
0,02
0,01
0
t_p
T
$\delta = \frac{t_p}{T}$
10^{-3}
10^{-2}
10^{-1}
1
10
10^2
t_p (ms)
10^3

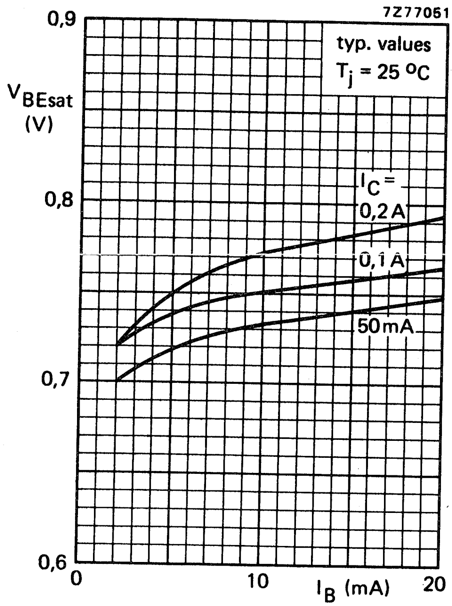

7Z77056.1
S.B. current multiplying factor at the V_{CEOmax} level
BUX86
M_I
δ = 0
0,01
0,02
0,05
0,10
0,20
0,33
0,50
0,75
1
10^2
10
1
10^{-2}
10^{-1}
1
10
t_p (ms)
10^2


7Z77055.1
S.B. current multiplying factor at the V_{CEOmax} level
BUX87
M_I
δ = 0
0,01
0,02
0,05
0,10
0,20
0,33
0,50
0,75
1
10^2
10
1
10^{-2}
10^{-1}
1
10
t_p (ms)
10^2


7Z77057.1
S.B. voltage multiplying factor at the I_{Cmax} level
10^2
M_V
10
1
δ = 0
0,01
0,02
0,05
0,10
0,20
0,33
0,50
0,75
1
10^{-2}
10^{-1}
1
t_p (ms)
10


7Z77052
T_j = 25 °C
max. values
typ values
V_{CEsat}
(V)
4
3
2
1
0
I_C =
0,1 A
0,2 A
50
mA
0
20
40
I_B (mA)
60


7Z77050
V_{CE} = 5 V
T_j = 25 °C
h_{FE}
10^3
10^2
10
1
typ
10^{-2}
10^{-1}
I_C (A)
1


7Z77061
typ. values
T_j = 25 °C
V_{BEsat}
(V)
0,9
0,8
0,7
0,6
I_C =
0,2 A
0,1 A
50 mA
0
10
I_B (mA)
20

APPLICATION INFORMATION ON BUX86 (detailed information on request)

Important factors in the design of SMPS circuits are the power losses and heatsink requirements of the supply output transistor and the base drive conditions during turn-off. In SMPS circuits with mains isolation the duty factor of the collector current generally varies between 0,25 to 0,5.

The operating frequency lies between 15 kHz and 50 kHz and the shape of the collector current varies from rectangular in a forward converter to a sawtooth in a flyback circuit.

As the BUX86 will mainly be used in low-power flyback converters the information on optimum base drive and device dissipation given in the graphs on page 13 is concentrated on this application. In these figures I_{CM} represents the highest repetitive peak collector current that can occur in the given circuit, e.g. during overload.

The total power dissipation for a limit-case transistor is given in Fig. 5 which applies for a mounting base temperature of 100 °C. The required thermal resistance for the heatsink can be calculated from

$$R_{th\ mb\text{-}a} = \frac{100 - T_{amb\ max}}{P_{tot}}.$$

To ensure thermal stability the minimum value of T_{amb} in the above equation is 40 °C.

A practical SMPS output circuit for an output of power in the order of 15 W is given in Fig. 2.

At a collector current of 200 mA and a base current of 20 mA in this circuit the following turn-off times can be expected.

			T_{mb} = 25 °C	100 °C	
Storage time	t_s	typ	1,3	1,8	μs
Fall time	t_f	typ	0,2	0,8	μs

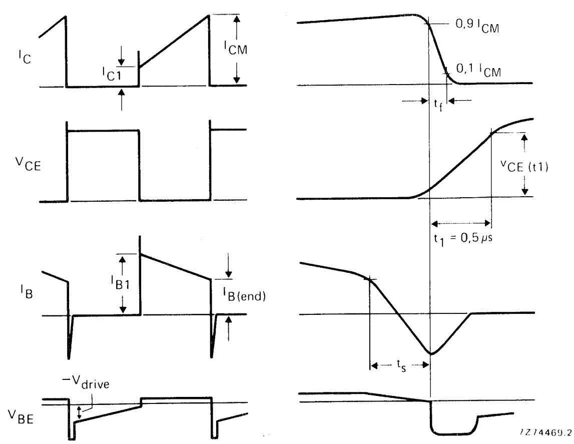


Fig. 1 Relevant waveforms of switching transistor.

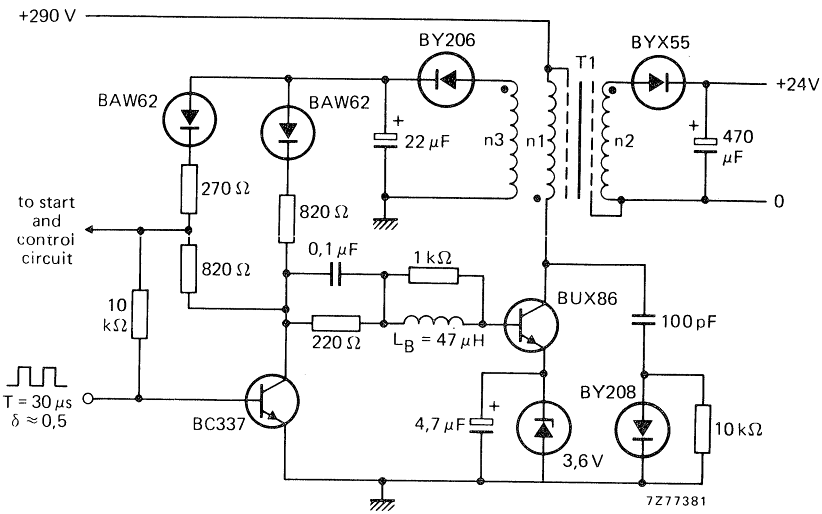


Fig. 2 Practical SMPS output circuit.

T1 (output transformer): Core U20; primary inductance L_p = 23 mH
n1 = 252 turns; n2 = 27 turns; n3 = 22 turns

$v_{CE(t1)} < 300$ V (see Fig. 1)

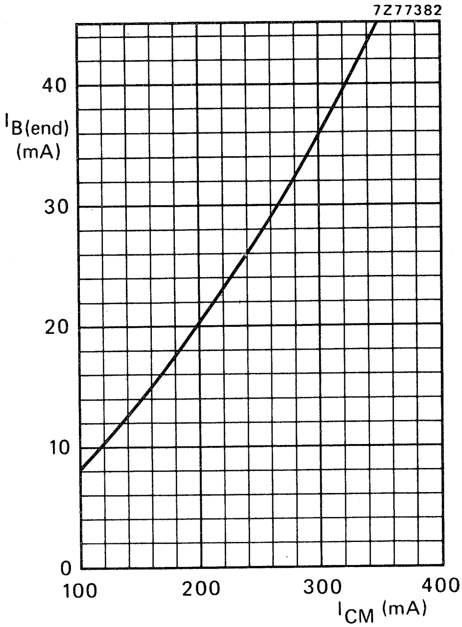


Fig. 3.

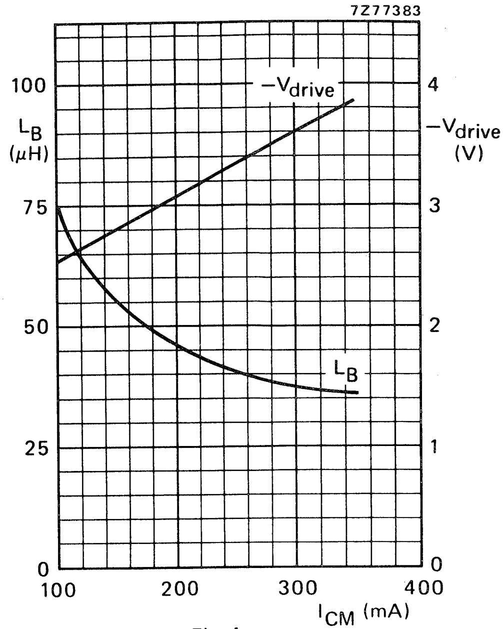


Fig. 4.

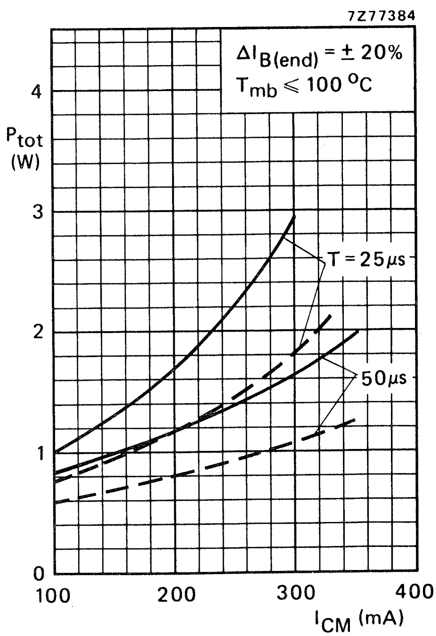


Fig. 5.

Fig. 3 Recommended nominal "end" value of the base current versus maximum peak collector current.

Fig. 4 Minimum required base inductance and recommended negative drive voltage versus maximum peak collector current.

Fig. 5 Maximum total power dissipation of a limit-case transistor if the base current is chosen in accordance with Fig. 3. Solid lines for I_{C1}/I_{CM} = 0,4 and dotted lines for I_{C1}/I_{CM} = 0.

SILICON DIFFUSED POWER TRANSISTOR

High-voltage, high-speed, glass-passivated n-p-n switching transistor in a TO-3 envelope, intended for use in three-phase a.c. motor control systems.

QUICK REFERENCE DATA

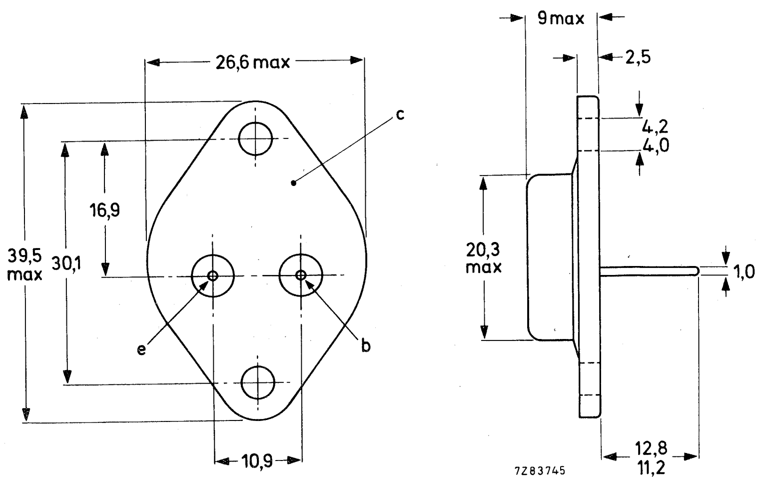
Collector-emitter voltage (peak value; $V_{BE} = 0$)	V_{CESM}	max.	1200	V
Collector-emitter voltage (open base)	V_{CEO}	max.	800	V
Collector current (d.c.)	I_C	max.	12	A
Collector current (peak value) $t_p < 2$ ms	I_{CM}	max.	20	A
Total power dissipation up to $T_{mb} = 25\ ^oC$	P_{tot}	max.	160	W
Collector-emitter saturation voltage $I_C = 9$ A; $I_B = 4$ A	V_{CEsat}	<	1	V
Collector saturation current	I_{Csat}	=	9	A
Fall time $I_{Con} = 9$ A; $I_{Bon} = -I_{Boff} = 4$ A	t_f	typ.	0,5	μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Collector connected to case.



See also chapters Mounting instructions and Accessories.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage (peak value; $V_{BE} = 0$)	V_{CESM}	max.	1200 V
Collector-emitter voltage (open base)	V_{CEO}	max.	800 V
Collector current (d.c.)	I_C	max.	12 A
Collector current (peak value); $t_p < 2$ ms	I_{CM}	max.	20 A
Base current (d.c.)	I_B	max.	8 A
Base current (peak value); $t_p < 2$ ms	I_{BM}	max.	12 A
Total power dissipation up to $T_{mb} = 25$ °C	P_{tot}	max.	160 W
Storage temperature	T_{stg}	−65 to + 150 °C	
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	0,78 K/W

CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified

Collector cut-off current*			
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$	I_{CES}	<	1 mA
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$; $T_j = 125$ °C	I_{CES}	<	4 mA
Emitter cut-off current			
$I_C = 0$; $V_{EB} = 5$ V	I_{EBO}	<	10 mA
Saturation voltages			
$I_C = 9$ A; $I_B = 4$ A	V_{CEsat}	<	1 V
	V_{BEsat}	<	1,5 V
$I_C = 12$ V; $I_B = 6$ A	V_{CEsat}	<	3 V
Collector-emitter sustaining voltage			
$I_C = 200$ mA; $I_B = 0$; $L = 25$ mH	$V_{CEOsust}$	>	800 V
Second breakdown collector current			
$V_{CE} = 100$ V; $t_p = 1$ s	$I_{(SB)C}$	>	0,4 A
Transition frequency at f = 5 MHz			
$I_C = 0{,}1$ A; $V_{CE} = 5$ V	f_T	typ.	7 MHz
Collector capacitance at f = 1 MHz			
$I_E = I_e = 0$; $V_{CB} = 10$ V	C_C	typ.	200 pF

* Measured with a half sine-wave voltage (curve tracer).

Switching times resistive load (Figs 2 and 3)

$I_{Con} = 9$ A; $I_{Bon} = -I_{Boff} = 4$ A

Turn-on time	t_{on}	typ.	1,5	μs
Turn-off: Storage time	t_s	typ.	4,5	μs
Fall time	t_f	typ.	0,5	μs

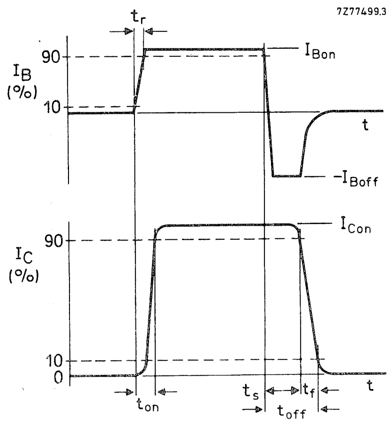


Fig. 2 Switching times waveforms with resistive load.

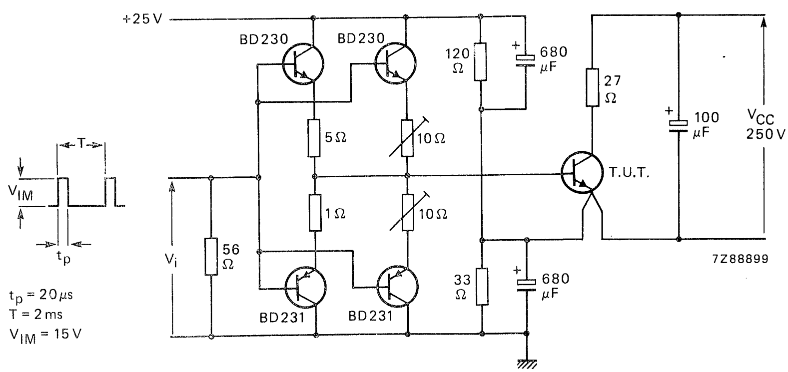


Fig. 3 Test circuit resistive load.

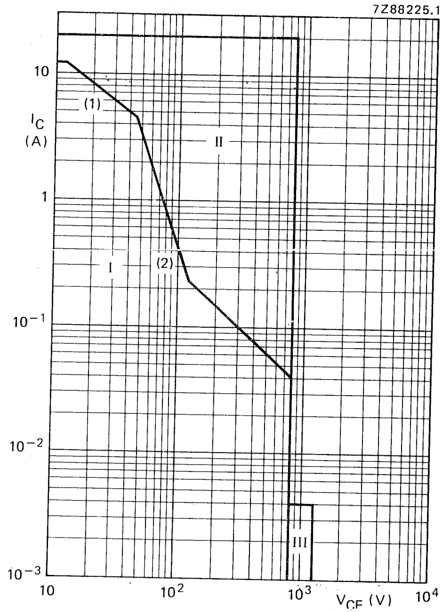


Fig. 4 Safe Operating ARea at $T_{mb} \leqslant 25\ ^oC$.

(1) $P_{tot\ max}$ line.

(2) Second-breakdown limits (independent of temperature).

I Region of permissible d.c. operation.

II Permissible extension for repetitive pulse operation.

III Repetitive pulse operation in this region is permissible, provided $V_{BE} \leqslant 0$ and $t_p \leqslant 5$ ms.

DARLINGTON POWER TRANSISTOR

High voltage, N-P-N monolithic Darlington power transistor, primarily intended for use in car ignition systems.

QUICK REFERENCE DATA

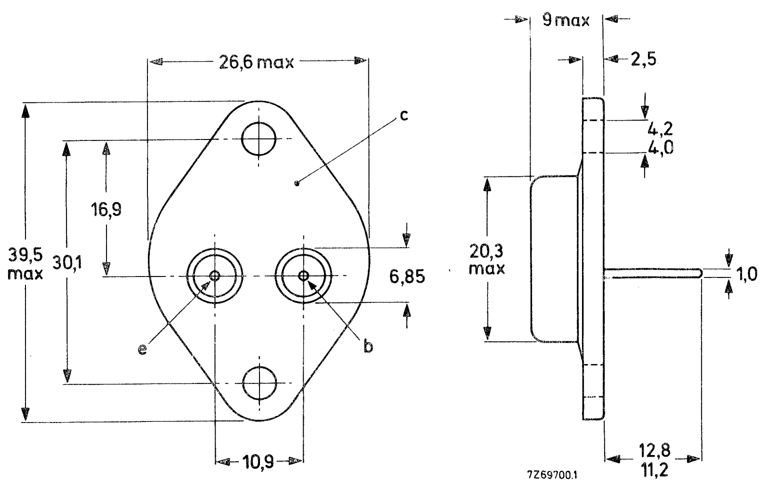
Collector-emitter voltage (V_{BE} = 0; peak value)	V_{CESM}	max.	650 V
Collector-emitter voltage (open base)	V_{CEO}	max.	400 V
Collector current (d.c.)	I_C	max.	12 A
Collector current (peak value) $t_p \leqslant 5$ ms	I_{CM}	max.	30 A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	125 W
Junction temperature	T_j	max.	200 °C
Collector-emitter saturation voltage			
I_C = 5 A; I_B = 50 mA	V_{CEsat}	<	1,5 V
I_C = 10 A; I_B = 300 mA	V_{CEsat}	<	2,0 V
Collector saturation current	I_{Csat}	typ.	10 A

MECHANICAL DATA

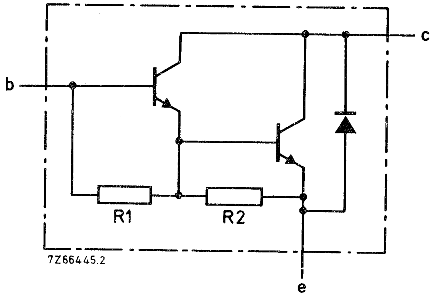
Dimensions in mm

Fig. 1 TO-3.

Collector connected to case.



See also chapters Mounting instructions and Accessories.



R1 typ. 500 Ω
R2 typ. 300 Ω

Fig. 2 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage (V_{EB} = 0); peak value	V_{CESM}	max.	650	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	V
Emitter-base voltage (open collector)	V_{EBO}	max.	6	V
Collector current (d.c.)	I_C	max.	12	A
Collector current (peak value); $t_p < 5$ ms	I_{CM}	max.	30	A
Base current (d.c.)	I_B	max.	4	A
Base current (peak value); $t_p \leqslant 5$ ms	I_{BM}	max.	6	A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	125	W
Storage temperature	T_{stg}	−65 to + 200		°C
Junction temperature*	T_j	max.	200	°C

THERMAL RESISTANCE*

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1,4	K/W

* Based on maximum average junction temperature in line with common industrial practice. The resulting higher junction temperature of the output transistor part is taken into account.

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current*			
V_{BE} = 0; V_{CE} = $V_{CESMmax}$	I_{CES}	<	1 mA
V_{BE} = 0; V_{CE} = $V_{CESMmax}$; T_j = 125 °C	I_{CES}	<	3 mA
Emitter cut-off current			
I_C = 0; V_{EB} = 6 V	I_{EBO}	<	20 mA
Collector-emitter sustaining voltage			
I_C = 5 A; I_{Boff} = 0; L = 8 mH	$V_{CEOsust}$	>	400 V
Saturation voltages			
I_C = 5 A; I_B = 50 mA	V_{CEsat}	<	1,5 V
	V_{BEsat}	<	2,0 V
I_C = 5 A; I_B = 60 mA; T_j = −40 °C	V_{CEsat}	<	1,5 V
	V_{BEsat}	<	2,0 V
I_C = 6 A; I_B = 100 mA; T_j = 150 °C	V_{CEsat}	<	1,5 V
	V_{BEsat}	<	2,0 V
I_C = 10 A; I_B = 300 mA	V_{CEsat}	<	2,0 V
	V_{BEsat}	<	2,5 V
Turn-off breakdown energy with inductive load (Fig. 3)			
$-I_{Boff}$ = 0; I_{CC} = 10 A; L = 8 mH; I_{Bon} = 300 mA; V_{CL} = 400 V	$E_{(BR)}$	>	400 mJ
Collector-emitter diode, forward voltage			
I_F = 8 A; I_B = 0	V_F	<	3,0 V

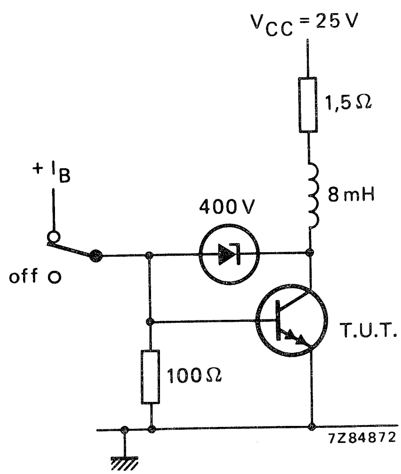


Fig. 3 Energy test circuit.

* Measured with a half sine-wave voltage (curve tracer).

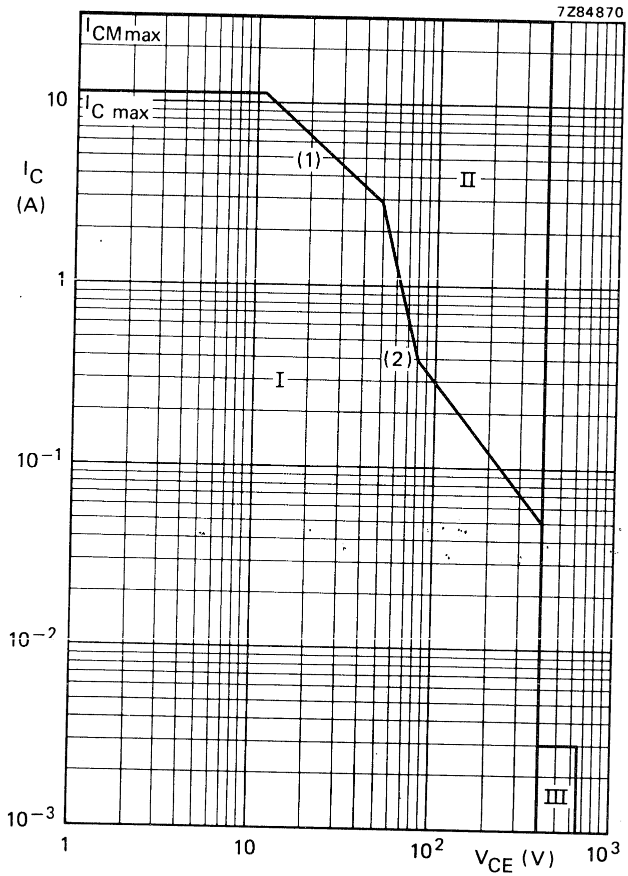


Fig. 4 Safe Operating ARea at $T_{mb} \leqslant 25$ °C.
(1) $P_{tot\,max}$ and $P_{tot\,peak\,max}$ lines.
(2) Second-breakdown limits (independent of temperature).

I Region of permissible d.c. operation
II Permissible extension for repetitive pulse operation
III Repetitive pulse operation in this region is permissible, provided $V_{BE} \leqslant 0$ and $t_p \leqslant 5$ ms.

SILICON DIFFUSED POWER TRANSISTORS

High-voltage, high-speed, glass-passivated n-p-n power transistors in a TO-3 envelope, intended for use in converters, inverters, switching regulators, motor control systems etc.

QUICK REFERENCE DATA

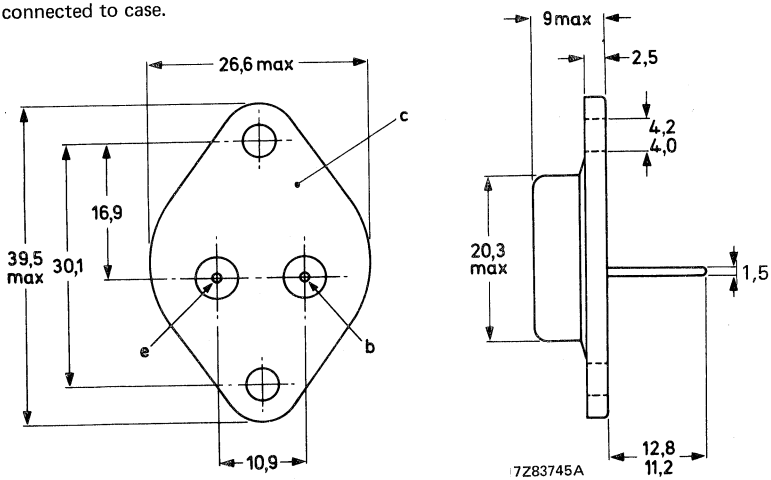
			BUX98	BUX98A	
Collector-emitter voltage (V_{EB} = 3 V)	V_{CEX}	max.	850	1000	V
Collector-emitter voltage (R_{BE} < 5 Ω)	V_{CER}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	30		A
Collector current (peak value) $t_p \leq 5$ ms	I_{CM}	max.	60		A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	250		W
Collector-emitter saturation voltage					
I_C = 20 A; I_B = 4 A	V_{CEsat}	<	1,5	–	V
I_C = 16 A; I_B = 3,2 A	V_{CEsat}	<	–	1,5	V
Fall time (resistive load)					
I_{Con} = 20 A; I_{Bon} = $-I_{Boff}$ = 4 A	t_f	<	0,8	–	μs
I_{Con} = 16 A; I_{Bon} = $-I_{Boff}$ = 3,2 A	t_f	<	–	0,8	μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Collector connected to case.



See also chapters Mounting instructions and Accessories.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BUX98	BUX98A	
Collector-emitter voltage (V_{EB} = 3 V)	V_{CEX}	max.	850	1000	V
Collector-emitter voltage ($R_{BE} \leqslant 5\ \Omega$)	V_{CER}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	30		A
Collector current (peak value); $t_p < 5$ ms	I_{CM}	max.	60		A
Base current (d.c.)	I_B	max.	8		A
Base current (peak value); $t_p < 5$ ms	I_{BM}	max.	30		A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	250		W
Storage temperature	T_{stg}		−65 to + 200		°C
Junction temperature	T_j	max.	200		°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	0,7	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			BUX98	BUX98A	
Collector cut-off current*					
$V_{CE} = V_{CERmax}$; $R_{BE} \leqslant 5\ \Omega$	I_{CER}	<	1		mA
$V_{CE} = V_{CERmax}$; $R_{BE} \leqslant 5\ \Omega$; T_j = 125 °C	I_{CER}	<	8		mA
Collector cut-off current					
$V_{CE} = V_{CEXmax}$; V_{EB} = 2,5 V	I_{CEX}	<	0,4		mA
$V_{CE} = V_{CEXmax}$; V_{EB} = 2,5 V; T_j = 125 °C	I_{CEX}	<	4		mA
Emitter cut-off current					
I_C = 0; V_{EB} = 5 V	I_{EBO}	<	2		mA
Saturation voltages					
I_C = 20 A; I_B = 4 A	V_{CEsat}	<	1,5	–	V
	V_{BEsat}	<	1,6	–	V
I_C = 30 A; I_B = 8 A	V_{CEsat}	<	3,5	–	V
I_C = 16 A; I_B = 3,2 A	V_{CEsat}	<	–	1,5	V
	V_{BEsat}	<	–	1,6	V
I_C = 24 A; I_B = 5 A	V_{CEsat}	<	–	5	V
Collector-emitter sustaining voltage					
I_C = 200 mA; I_{Boff} = 0; L = 25 mH	$V_{CEOsust}$	>	400	450	V
Transition frequency at f = 1 MHz					
I_C = 1 A; V_{CE} = 10 V	f_T	typ.	5		MHz
Emitter-base breakdown voltage					
I_C = 0; I_B = 0,1 A	$V_{(BR)EBO}$		7 to 30		V
Collector capacitance at f = 1 MHz					
V_{CE} = 10 V	C_C	typ.	500		pF

* Measured with a half sine-wave voltage (curve tracer).

CHARACTERISTICS (continued)

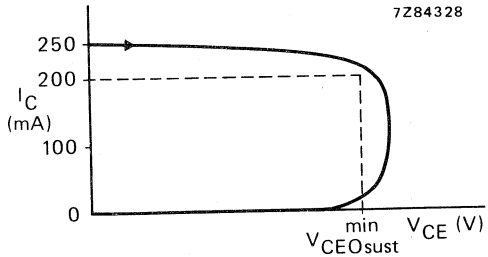


Fig. 2 Oscilloscope display for sustaining voltage.

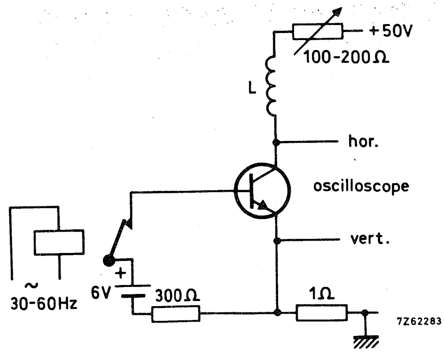
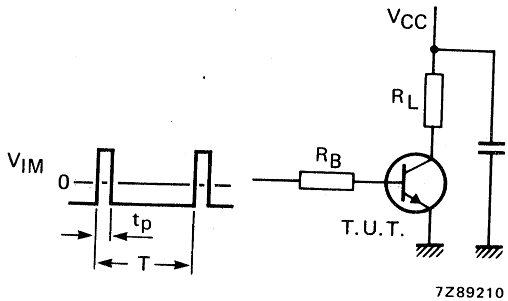


Fig. 3 Test circuit for $V_{CEOsust}$.

			BUX98	BUX98A	
Switching times resistive load					
I_{Con} = 20 A; I_{Bon} = $-I_{Boff}$ = 4 A					
Turn-on time	t_{on}	typ.	0,55	—	µs
		<	1	—	µs
Turn-off: Storage time	t_s	typ.	1,5	—	µs
		<	3	—	µs
Fall time	t_f	typ.	0,3	—	µs
		<	0,8	—	µs
I_{Con} = 16 A; I_{Bon} = $-I_{Boff}$ = 3,2 A					
Turn-on time	t_{on}	typ.	—	0,55	µs
		<	—	1	µs
Turn-off: Storage time	t_s	typ.	—	1,5	µs
		<	—	3	µs
Fall time	t_f	typ.	—	0,3	µs
		<	—	0,8	µs
Switching times inductive load					
I_{Con} = 20 A; I_B = 4 A					
Turn-off: Storage time	t_s	typ.	3,5	—	µs
Fall time	t_f	typ.	80	—	ns
I_{Con} = 20 A; I_B = 4 A; T_j = 100 °C					
Storage time	t_s	<	5	—	µs
Fall time	t_f	<	400	—	ns
I_{Con} = 16 A; I_B = 3,2 A					
Turn-off: Storage time	t_s	typ.	—	3,5	µs
Fall time	t_f	typ.	—	80	ns
I_{Con} = 16 A; I_B = 3,2 A; T_j = 100 °C	t				
Turn-off: Storage time	t_s	<	—	5	µs
Fall time	t_f	<	—	400	ns



$V_{CC} = 250$ V
$V_{IM} = -6$ to $+8$ V
$\frac{t_p}{T} = 0{,}01$
$t_p = 20\ \mu s$

Fig. 4 Test circuit resistive load.

The values of R_B and R_L are selected in accordance with I_{Con} and I_B requirements.

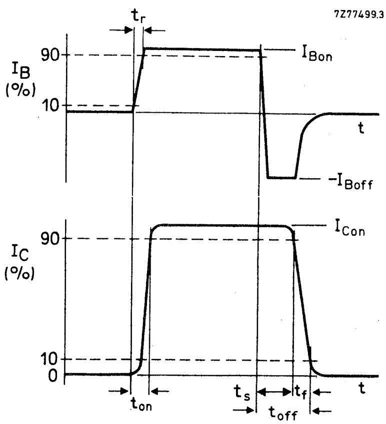


Fig. 5 Switching times waveforms with resistive load.

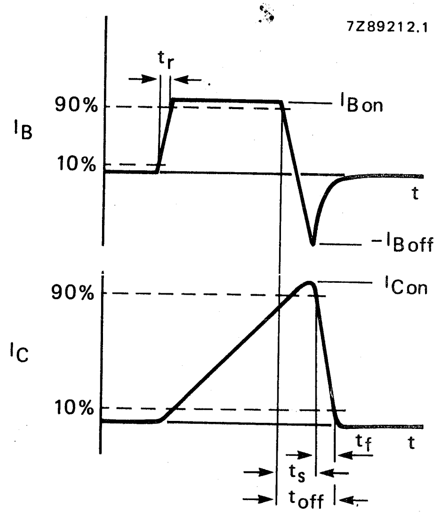
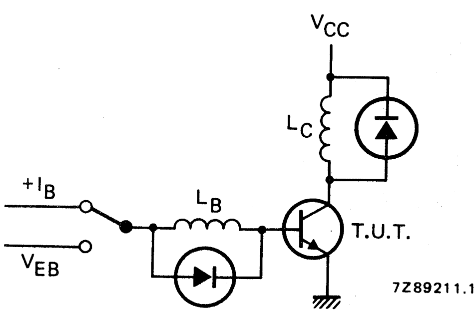


Fig. 6 Switching times waveforms with inductive load.



$V_{CC} = 300$ V
$L_B = 3\ \mu H$
$L_C = 1{,}5$ mH
$V_{EB} = 5$ V

Fig. 7 Test circuit inductive load.

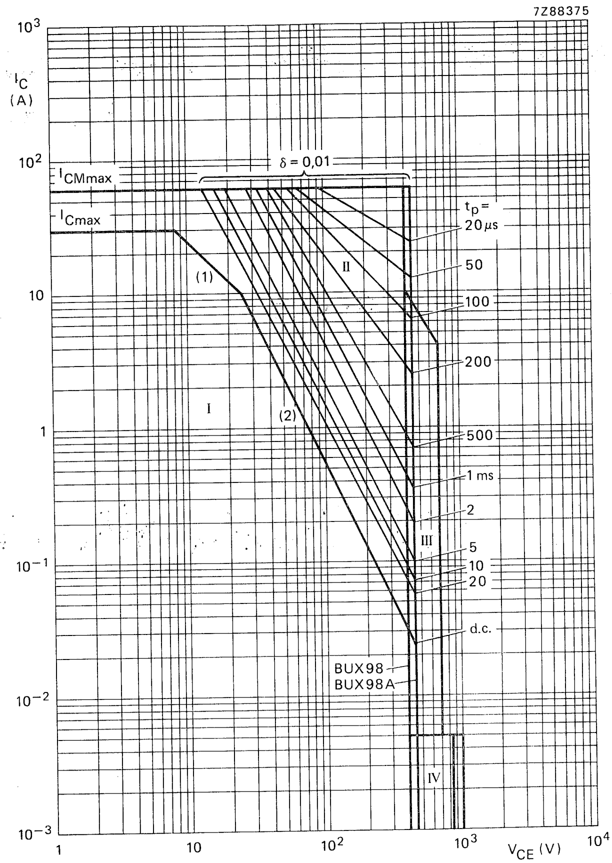


Fig. 8 Safe Operating ARea at $T_{mb} \leqslant 25$ °C.

(1) $P_{tot\ max}$ and $P_{peak\ max}$ lines.
(2) Second-breakdown limits (independent of temperature).

I Region of permissible d.c. operation.
II Permissible extension for repetitive pulse operation.
III Area of permissible operation during turn-on in single transistor converters, provided $R_{BE} \leqslant 100\ \Omega$ and $t_p \leqslant 0,6\ \mu s$.
IV Repetitive pulse operation in this region is permissible, provided $V_{BE} \leqslant 0$ and $t_p \leqslant 2$ ms.

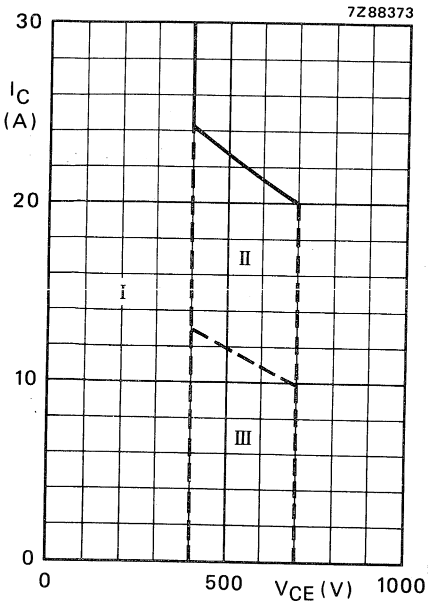


Fig. 9 Forward bias safe operation area, $T_j \leqslant 125\ ^oC$.
I Safe operation area during turn-off and during turn-on.
For BUX98A the right-hand limit is 450 V.
II Safe operation are during turn-on only provided $t_r < 0{,}2\ \mu s$.
III Safe operation area during turn-on only; provided $t_r < 0{,}5\ \mu s$ and $R_{BE} < 50\ \Omega$.

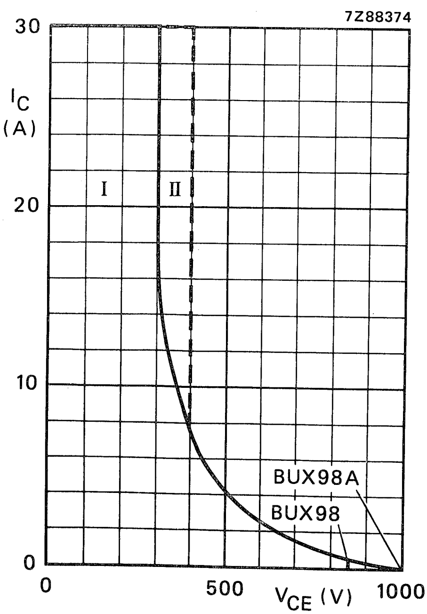


Fig. 10 Reverse bias safe operation area, $I_{Cend}/I_{Bend} \geqslant 5$; $-V_{BE} = 3$ V.
I Normal reverse bias safe operation area $V_{BE} < 0$ V.
II Extension of the reverse bias safe operation area provided a desaturation network (Baker clamp) is used.
For BUX98A V_{CE} limit = 450 V.

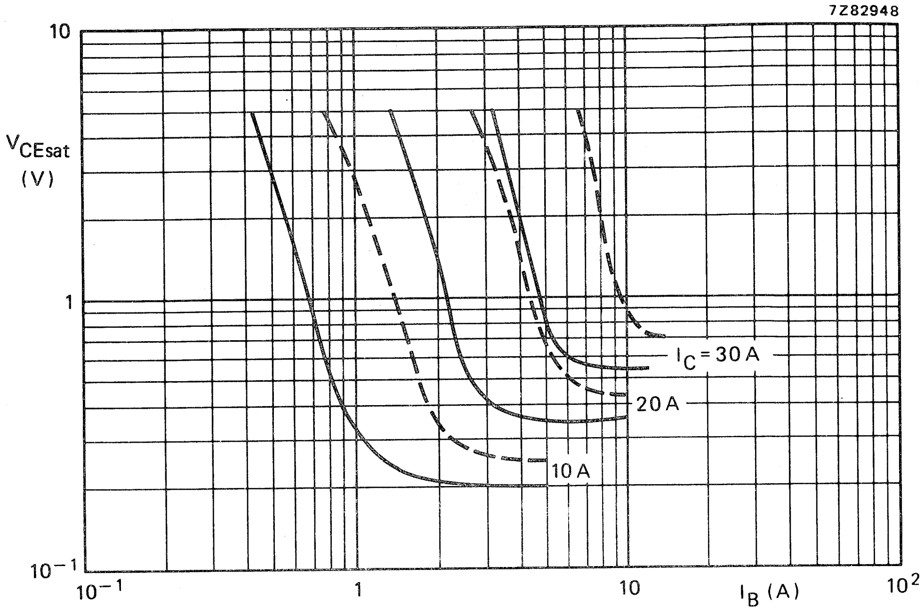


Fig. 11 Typical (——) and maximum (– – –) values saturation voltage. T_j = 25 °C.

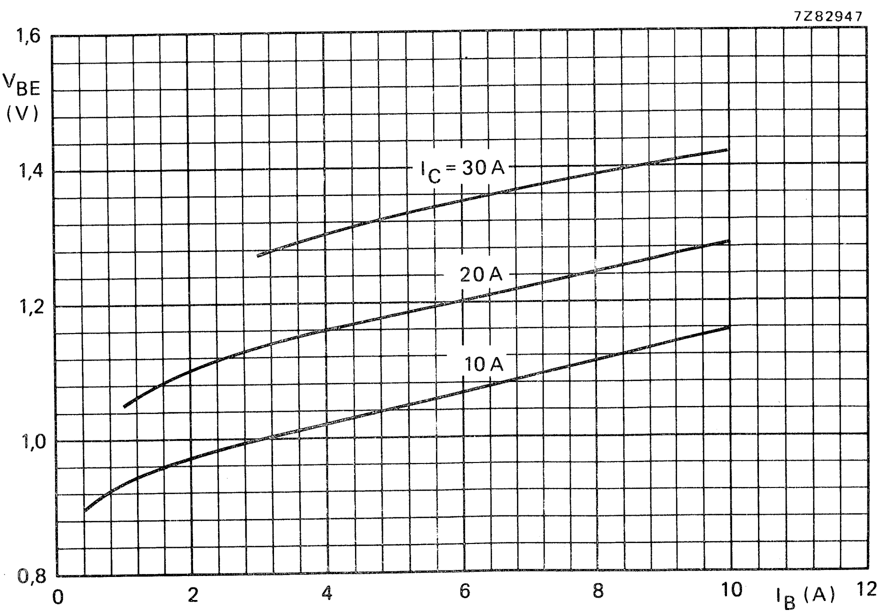


Fig. 12 Typical values at T_j = 25 °C.

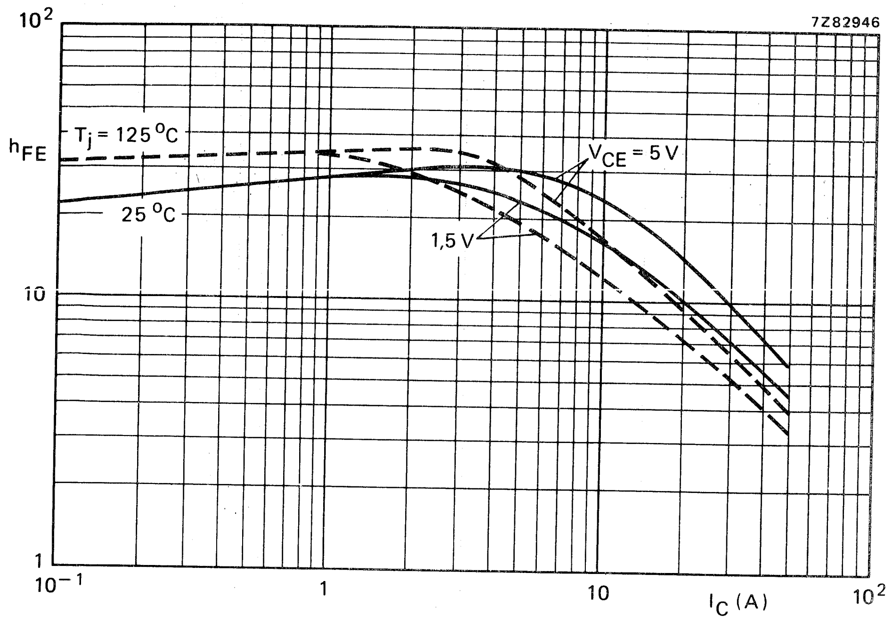


Fig. 13 Typical values d.c. current gain.

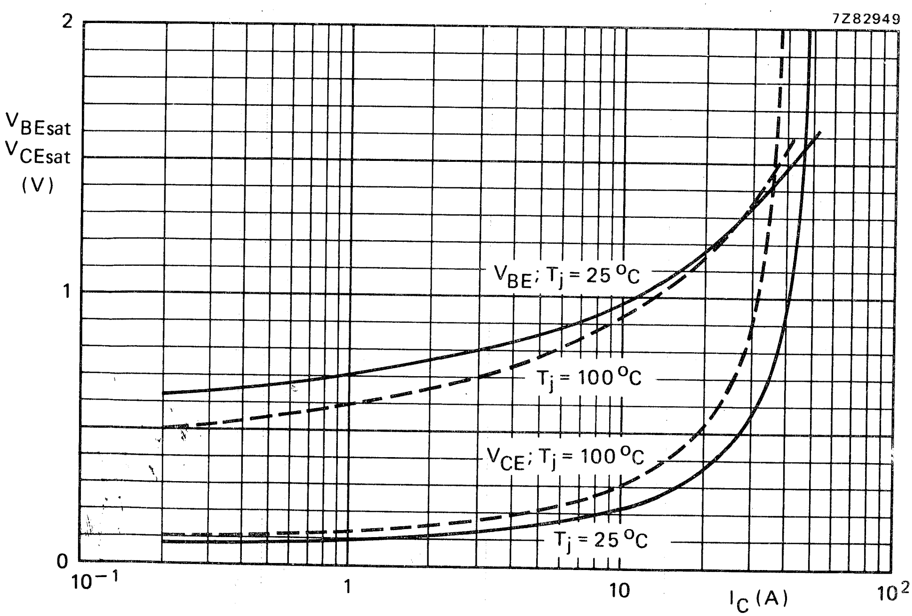


Fig. 14 Typical values base and collector voltage. $I_C/I_B = 5$.

SILICON DIFFUSED POWER TRANSISTOR

High-voltage, high-speed switching n-p-n transistor in a TO-3 envelope especially intended for use in a.c. motor control systems from three-phase mains.

QUICK REFERENCE DATA

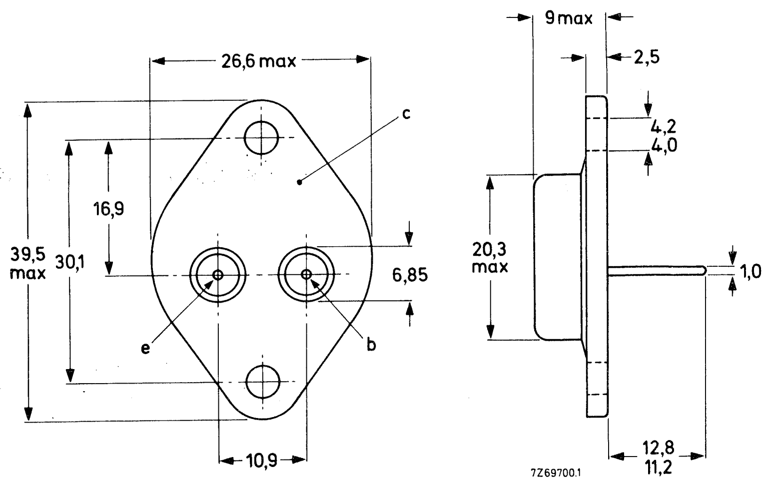
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	1500	V
Collector-emitter voltage (open base)	V_{CEO}	max.	800	V
Collector current (d.c.)	I_C	max.	6	A
Total power dissipation up to T_{mb} = 60 °C	P_{tot}	max.	80	W
Collector-emitter saturation voltage I_C = 4,5 A; I_B = 2 A	V_{CEsat}	<	1	V
D.C. current gain I_C = 4,5 A; V_{CE} = 5 V	h_{FE}	>	2,5	

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Collector connected to case.



See also chapters Mounting instructions and Accessories.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	1500	V
Collector-emitter voltage (open base)	V_{CEO}	max.	800	V
Collector current (d.c.)	I_C	max.	6	A
Collector current (peak value)	I_{CM}	max.	10	A
Collector current (non-repetitive peak)	I_{CSM}	max.	15	A
Base current (d.c.)	I_B	max.	4	A
Base current (peak value)	I_{BM}	max.	6	A
Reverse base current (d.c. or average over any 20 ms period)	$-I_{B(AV)}$	max.	100	mA
Reverse base current (peak value) *	$-I_{BM}$	max.	4	A
Total power dissipation up to T_{mb} = 60 °C	P_{tot}	max.	80	W
Storage temperature	T_{stg}	−65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	max.	1,12	K/W

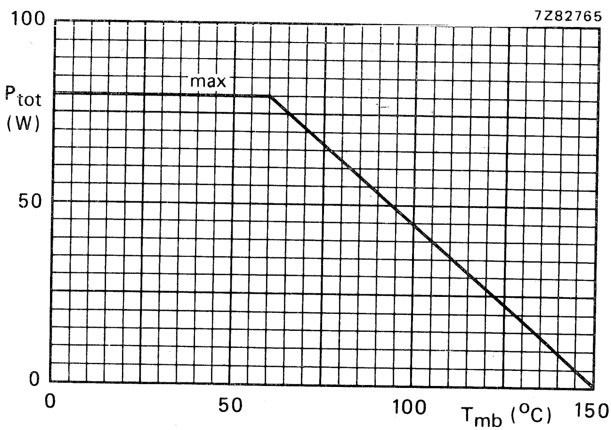


Fig. 2 Power derating curve.

* Turn-off current.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current $V_{BE} = 0$; $V_{CE} = V_{CESMmax}$; T_j = 125 °C	I_{CES}	<	1,0 mA
D.C. current gain I_C = 4,5 A; V_{CE} = 5 V	h_{FE}	>	2,5
Emitter cut-off current $I_C = 0$; V_{EB} = 5 V	I_{EBO}	<	10 mA
Saturation voltage I_C = 4,5 A; I_B = 2 A	V_{CEsat}	<	1 V
I_C = 4,5 A; I_B = 2 A	V_{BEsat}	<	1,5 V
Collector-emitter sustaining voltage $I_B = 0$; I_C = 100 mA; L = 25 mH	$V_{CEOsust}$	>	800 V

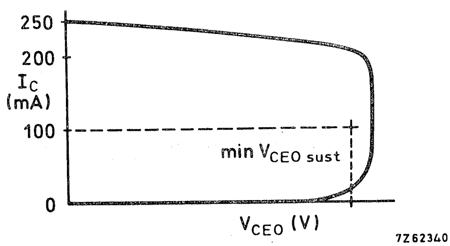


Fig. 3 Oscilloscope display for $V_{CEOsust}$.

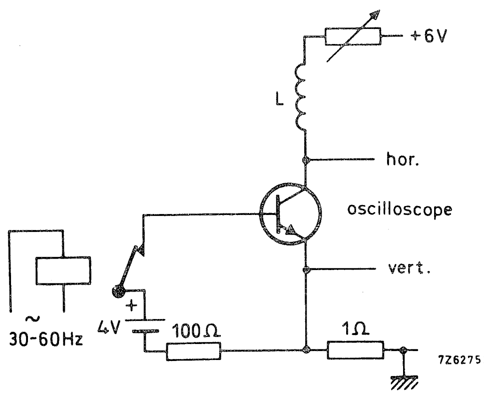


Fig. 4 Test circuit for $V_{CEOsust}$.

Second-breakdown collector current V_{CE} = 100 V; t_p = 1 s	$I_{(SB)}$	>	0,3 A
Transition frequency at f = 5 MHz I_C = 0,1 A; V_{CE} = 5 V	f_T	typ.	7 MHz
Collector capacitance at f = 1 MHz $I_E = I_e = 0$; V_{CB} = 10 V	C_c	typ.	125 pF

CHARACTERISTICS (continued)

Switching times (between 10% and 90% levels)
in resistive switching circuit
I_{Con} = 4,5 A; V_{CC} = 250 V; R_L = 56 Ω
$I_{Bon} = -I_{Boff}$ = 2 A

→ Turn-on time	t_{on}	typ.	1,5 μs
→ Storage time ($t_s = t_{off} - t_f$)	t_s	typ.	4,5 μs
Fall time	t_f	typ.	0,5 μs

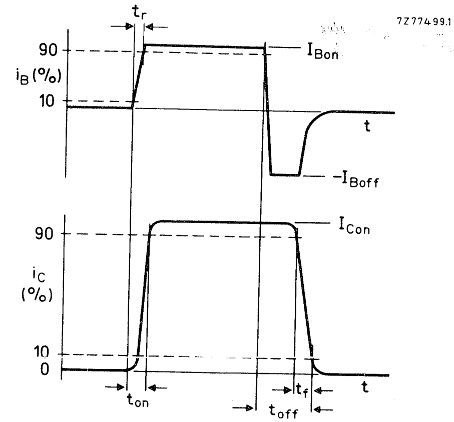


Fig. 5 Waveforms.

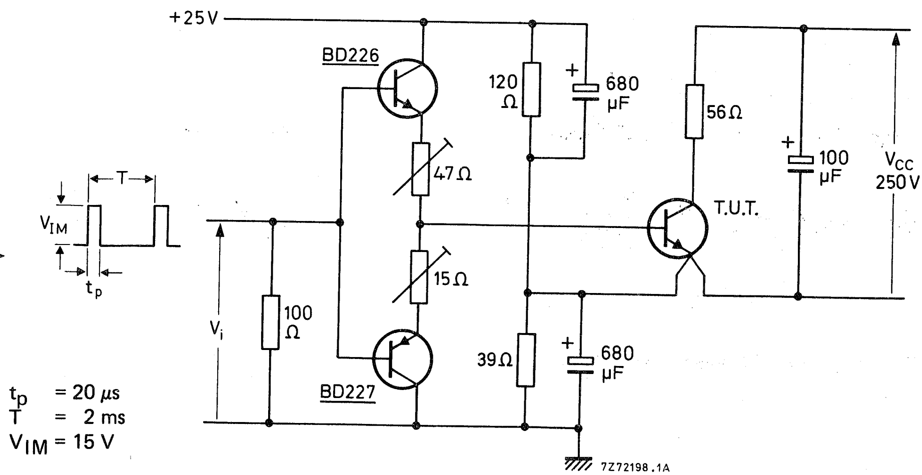


Fig. 6 Test circuit.

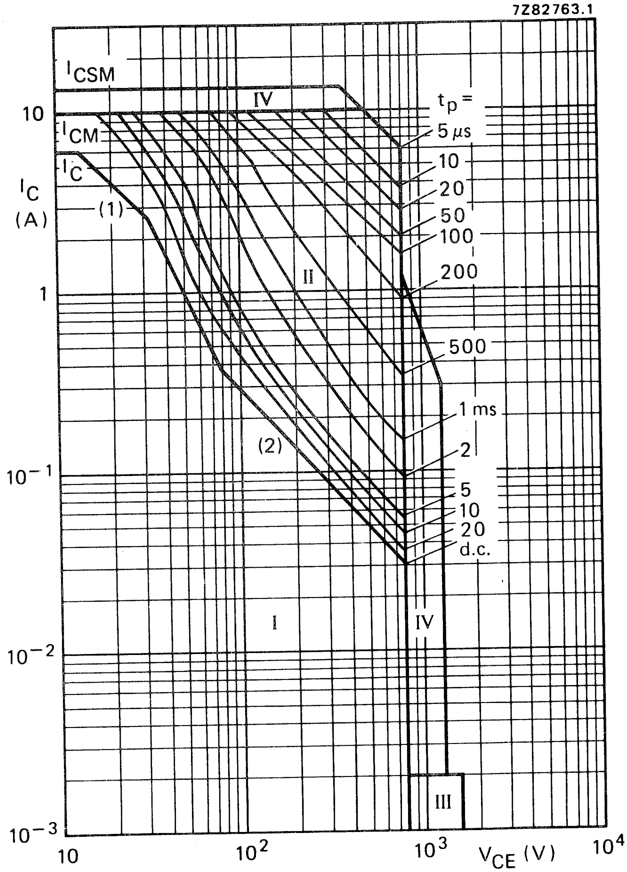


Fig. 7 Safe Operating ARea with the transistor forward biased.
$T_{mb} \leqslant 60\ ^oC$; $\delta = 0,01$.

1. $P_{tot\ max}$ and $P_{peak\ max}$ lines.
2. Second-breakdown limits (independent of temperature).

I Region of permissible d.c. operation.
II Permissible extension for repetitive pulse operation.
III Repetitive pulse operation in this region is permissible, provided $V_{BE} \leqslant 0$ V; $t_p \leqslant 20\ \mu s$; $\delta \leqslant 0,25$.
IV Transient I_C/V_{CE} limit
for V_{CE} less than 700 V then t_p less than or equal to 25 μs
for V_{CE} greater than 700 V then t_p less than 5 μs.

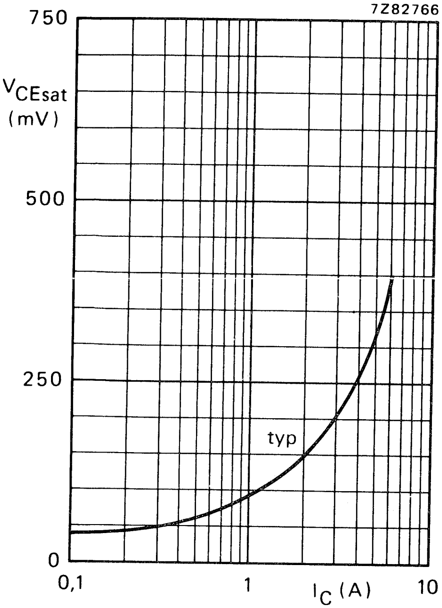


Fig. 8 Collector-emitter saturation voltage at $I_C/I_B = 2$; $T_j = 25\ ^oC$.

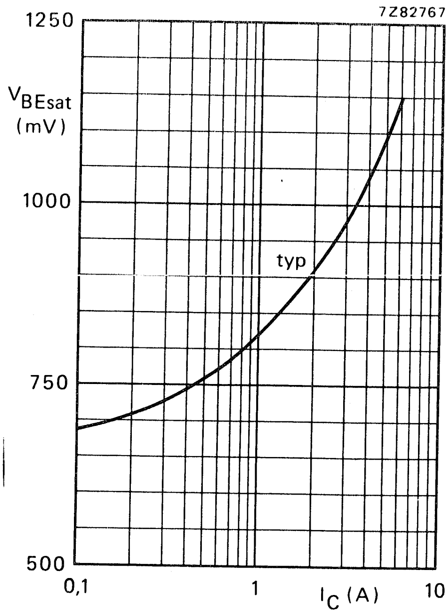


Fig. 9 Base-emitter saturation voltage at $I_C/I_B = 2$; $T_j = 25\ ^oC$.

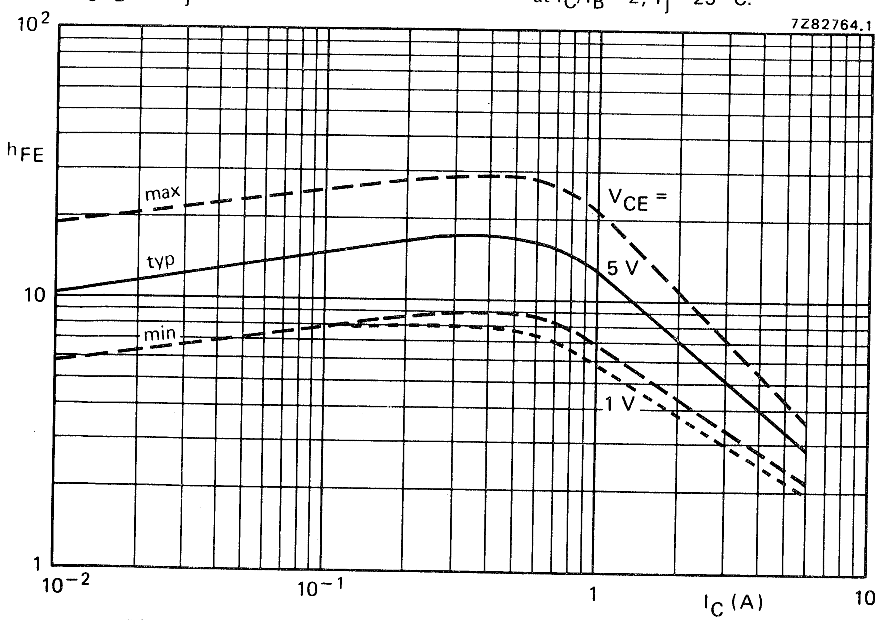


Fig. 10 D.C. current gain at $V_{CE} = 5$ V; $T_j = 25\ ^oC$; . . . . at $V_{CE} = 1$ V.

MOUNTING INSTRUCTIONS

General note on flat heatsinks

All information on thermal resistances of the accessories combined with flat heatsinks is valid for *square* heatsinks of *1,5 mm blackened aluminium.*

For a few variations the thermal resistance may be derived as follows:

- Rectangular heatsinks (sides a and 2a)
  When mounted with long side horizontal, multiply by 0,95.
  When mounted with short side horizontal, multiply by 1,10.
- Unblackened or thinner heatsinks
  Multiply by the factor given in Fig. 1 as a function of the heatsink size A.

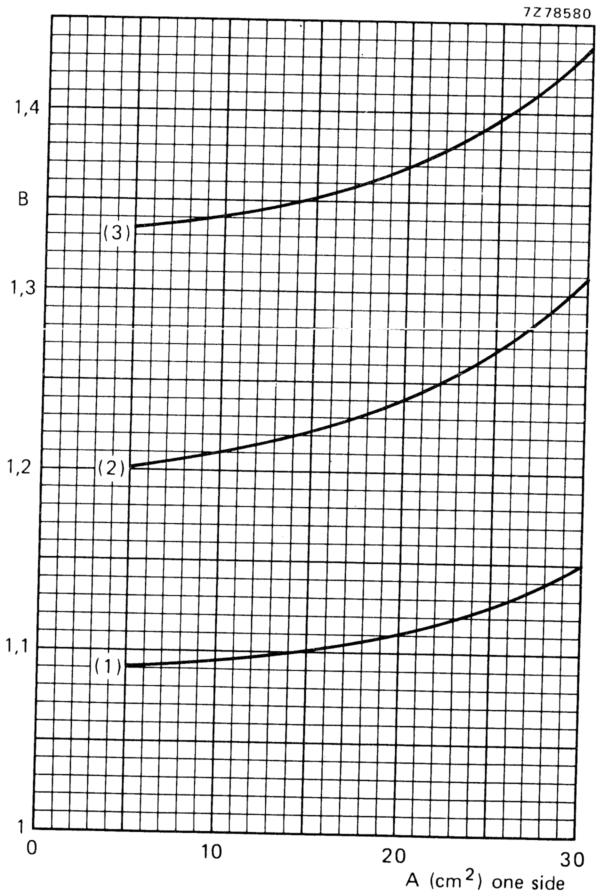


Fig. 1 Multiplication factor (B) as a function of heatsink area (A).
(1) 1 mm blackened aluminium.
(2) 1,5 mm unblackened aluminium.
(3) 1 mm unblackened aluminium.

MOUNTING INSTRUCTIONS
FOR TO-126 AND SOT-82 ENVELOPES

GENERAL DATA AND INSTRUCTIONS

General rules

1. First fasten the devices to the heatsink before soldering the leads.
2. Avoid axial stress to the leads.
3. Keep mounting tool (e.g. screwdriver) clear of the plastic body.

Heatsink requirements

Minimum thickness: 2 mm.
Flatness in the mounting area: 0,02 mm maximum per 10 mm.
Mounting holes must be deburred and should also be perpendicular to the plane of the heatsink, within 10^{o} tolerance for M2,5 thread and within 2^{o} tolerance for M3 thread. If the hole in the heatsink is threaded, it should be counter-sunk and free of burrs.

Heatsink compound

Values of the thermal resistance from mounting base to heatsink ($R_{th\ mb-h}$) given for mounting with heatsink compound refer to the use of a metallic oxide-loaded compound. Ordinary silicone grease is not recommended.

For insulated mounting, the compound should be applied to the bottom of both device and insulator.

Mounting methods for power transistors

1. Clip mounting (TO-126 and SOT-82)

   Mounting by means of spring clip offers:

   a. A good thermal contact under the crystal area.
   b. Safe insulation for mains and high voltage operation

2. M2,5 and M3 screw mounting. (TO-126 only).

   The spacing washer should be inserted between screw head and body.

   Mounting torque for screw mounting:

Minimum torque (for good heat transfer)	0,4 Nm (4 kgcm)
Maximum torque (to avoid damaging the device)	0,6 Nm (6 kgcm)

   N.B. when the driven nut or screw is in direct contact with a toothed lock washer the torques are as follows:

Minimum torque (for good heat transfer)	0,55 Nm (5,5 kgcm)
Maximum torque (to avoid damaging the device)	0,80 Nm (8,0 kgcm)

3. Body mounting (SOT-82).

   A SOT-82 envelope can be adhesive mounted or soldered into a hybrid circuit.
   For soldering a copper plate or an anodized aluminium plate with copper layer is recommended.
   When adhesive mounting is applied also a ceramic substrate may be used.

Thermal data

From mounting base to heatsink

	$R_{th\ mb\text{-}h}$ (K/W)			
	clip mounting		screw mounting	
	direct	insulated	direct	insulated
TO-126, with heatsink compound	1,0	3,0	0,5	3,0
TO-126, without heatsink compound	3,0	6,0	1,0	6,0
SOT-82, with heatsink compound	0,4	2,0	–	–
SOT-82, without heatsink compound	2,0	5,0	–	–

Lead bending

Maximum permissible tensile force on the body, for 5 seconds is 20 N (2 kgf).

The leads can be bent through 90° maximum, twisted or straightened. To keep forces within the above-mentioned limits, the leads are generally clamped near the body, using pliers. The leads should neither be bent nor twisted less than 2,4 mm from the body.

Lead soldering

For devices with a maximum junction temperature ⩽ 150 °C.

a. Dip or wave soldering
   Temperature ⩽ 260 °C at a distance from the body > 5 mm and for a total contact time with soldering bath or waves < 7 s.
b. Hand soldering
   Temperature at a distance from the body > 3 mm for a total contact time < 5 s is < 275 °C or < 250 °C for a total contact time of < 10 s.

The body of the device must be kept clear of anything with a temperature > 200 °C.
Avoid any force on body and leads during or after soldering; do not correct the position of the device or of its leads after soldering.

Mounting base soldering

Recommended metal-alloy of solder paste (85% metal weight)
62 Sm/36 Pb/2 Ag or 60 Sn/40 Pb.
Maximum soldering temperature ⩽ 200 °C (tab-temperature).
Soldering cycle duration including pre-heating ⩽ 30 sec.

For good soldering and avoiding damage to the encapsulation pre-heating is recommended to a temperature ⩽ 165 °C at a duration ⩽ 10 s.

INSTRUCTIONS FOR CLIP MOUNTING

Direct mounting with clip 56353

1. Place the device on the heatsink, applying heatsink compound to the mounting base.
2. Push the short end of the clip into the narrow slot in the heatsink with the clip at an angle of 10° to 30° to the vertical (see Figs 1 and 2).
3. Push down the clip over the device until the long end of the clip snaps into the wide slot in the heatsink. The clip should bear on the plastic body (see Fig. 3).

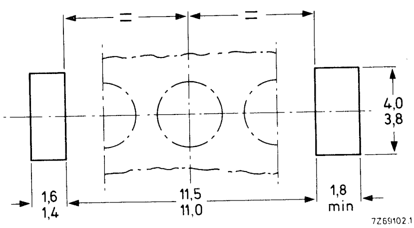


Fig. 1 Heatsink requirements.

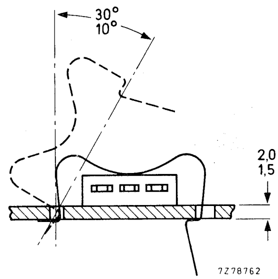


Fig. 2 Mounting spring clip.

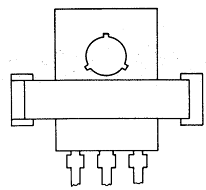


Fig. 3 Position of transistor (top view).

Insulated mounting with clip 56353 and mica 56354 (up to 1000 V insulation)

1. Place the device with the insulator on the heatsink, applying heatsink compound to the bottom of both device and insulator.
2. Push the short end of the clip into the narrow slot in the heatsink with the clip at an angle of 10° to 30° to the vertical (see Figs 4 and 5).
3. Push down the clip over the device until the long end of the clip snaps into the wide slot in the heatsink. The clip should bear on the plastic body (Fig. 6). Ensure that the device is centred on the mica insulator to prevent creepage.

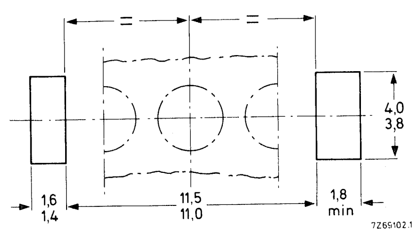


Fig. 4 Heatsink requirements.

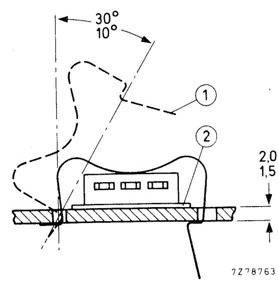


Fig. 5 Mounting.
(1) spring clip 56353.
(2) insulator 56354.

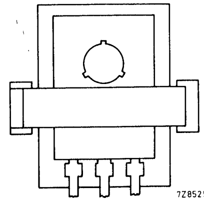


Fig. 6 Position of transistor (top view).

INSTRUCTIONS FOR SCREW MOUNTING

Dimensions in mm

Direct mounting with screw and spacing washer

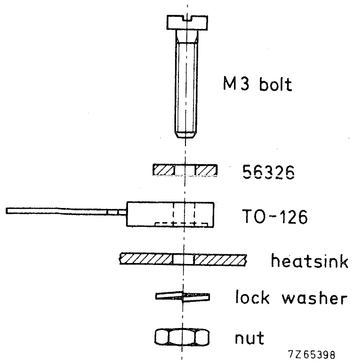


Fig. 7 Assembly through heatsink with nut.

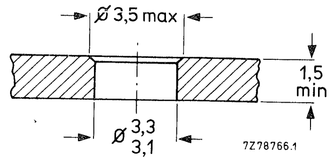


Fig. 8 Heatsink requirements.

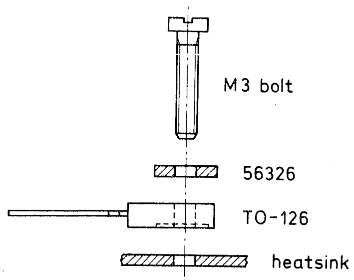


Fig. 9 Assembly into tapped heatsink.

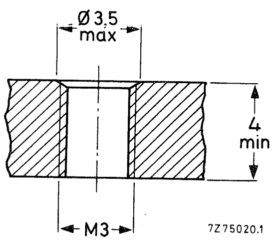


Fig. 10 Heatsink requirements.

INSTRUCTIONS FOR SCREW MOUNTING

Insulated mounting with 56326, 56387a and 56387b (up to 300 V)

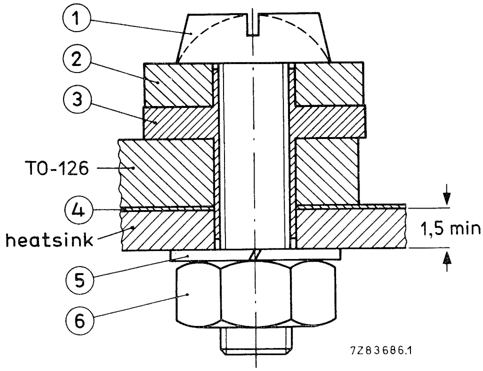


Fig. 15 Assembly through heatsink with nut.

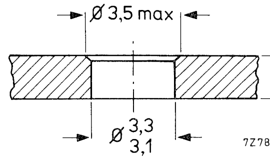


Fig. 16 Heatsink requirements.

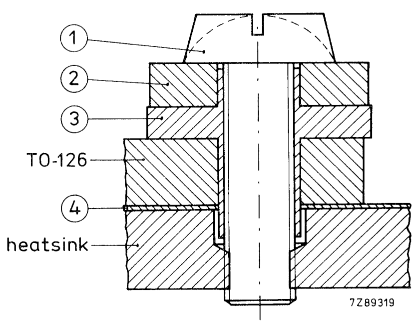


Fig. 17 Assembly with tapped heatsink.

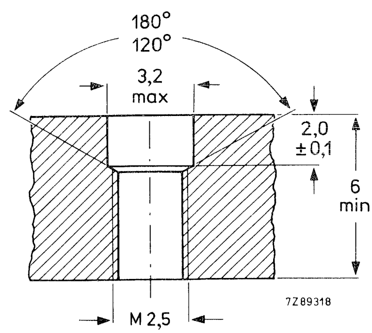


Fig. 18 Heatsink requirements.

Legend

1 M2,5 screw
2 metal washer 56326
3 insulating bush 56387b
4 mica washer 56387 a
5 lock washer
6 M2,5 nut

MOUNTING INSTRUCTIONS FOR TO-220 ENVELOPES

GENERAL DATA AND INSTRUCTIONS

General rules

1. First fasten the device to the heatsink before soldering the leads.
2. Avoid axial stress to the leads.
3. Keep mounting tool (e.g. screwdriver) clear of the plastic body.
4. The rectangular washer may only touch the plastic part of the body; it should not exert any force on that part (screw mounting).

Heatsink requirements

Flatness in the mounting area: 0,02 mm maximum per 10 mm.
Mounting holes must be deburred, see further mounting instructions.

Heatsink compound

Values of the thermal resistance from mounting base to heatsink ($R_{th\ mb\text{-}h}$) given for mounting with heatsink compound refer to the use of a metallic oxide-loaded compound. Ordinary silicone grease is not recommended.

For insulated mounting, the compound should be applied to the bottom of both device and insulator.

Mounting methods for power transistors

1. Clip mounting

   Mounting with a spring clip gives:

   a. A good thermal contact under the crystal area, and slightly lower $R_{th\ mb\text{-}h}$ values than screw mounting.
   b. Safe insulation for mains operation.

2. M3 screw mounting

   It is recommended that the rectangular spacing washer is inserted between screw head and mounting tab.

   Mounting torque for screw mounting:

   (For thread-forming screws these are final values. Do not use self-tapping screws.)

Minimum torque (for good heat transfer)	0,55 Nm (5,5 kgcm)
Maximum torque (to avoid damaging the device)	0,80 Nm (8,0 kgcm)

   N.B.: When a nut or screw is not driven direct against a curved spring washer or lock washer (not for thread-forming screw), the torques are as follows:

Minimum torque (for good heat transfer)	0,4 Nm (4 kgcm)
Maximum torque (to avoid damaging the device)	0,6 Nm (6 kgcm)

N.B.: Data on accessories are given in separate data sheets.

3. Rivet mounting non-insulated

The device should not be pop-rivetted to the heatsink. However, it is permissible to press-rivet providing that eyelet rivets of soft material are used, and the press forces are slowly and carefully controlled so as to avoid shock and deformation of either heatsink or mounting tab.

Thermal data

From mounting base to heatsink			clip mounting	screw mounting	
with heatsink compound, direct mounting	$R_{th\ mb\text{-}h}$	=	0,3	0,5	K/W
without heatsink compound, direct mounting	$R_{th\ mb\text{-}h}$	=	1,4	1,4	K/W
with heatsink compound and 0,1 mm maximum mica washer	$R_{th\ mb\text{-}h}$	=	2,2	–	K/W
with heatsink compound and 0,25 mm maximum alumina insulator	$R_{th\ mb\text{-}h}$	=	0,8	–	K/W
with heatsink compound and 0,05 mm mica washer insulated up to 500 V	$R_{th\ mb\text{-}h}$	=	–	1,4	K/W
with heatsink compound and 0,05 mm mica washer insulated up to 800 V/1000 V	$R_{th\ mb\text{-}h}$	=	–	1,6	K/W
without heatsink compound and 0,05 mm mica washer insulated up to 500 V	$R_{th\ mb\text{-}h}$	=	–	3,0	K/W
without heatsink compound and 0,05 mm mica washer insulated up to 800 V/1000 V	$R_{th\ mb\text{-}h}$	=	–	4,5	K/W

Lead bending

Maximum permissible tensile force on the body, for 5 seconds is 20 N (2 kgf).

The leads can be bent through 90° maximum, twisted or straightened. To keep forces within the above-mentioned limits, the leads are generally clamped near the body, using pliers. The leads should neither be bent nor twisted less than 2,4 mm from the body.

Soldering

Lead soldering temperature at > 3 mm from the body; $t_{sld} < 5$ s:

Devices with $T_{j\ max} \leq 175$ °C, soldering temperature $T_{sld\ max} = 275$ °C.
Devices with $T_{j\ max} \leq 110$ °C, soldering temperature $T_{sld\ max} = 240$ °C.

Avoid any force on body and leads during or after soldering: do not correct the position of the device or of its leads after soldering.

It is not permitted to solder the metal tab of the device to a heatsink, otherwise its junction temperature rating will be exceeded.

Mounting base soldering

Recommended metal-alloy of solder paste (85% metal weight)
62 Sm/36 Pb/2 Ag or 60 Sn/40 Pb.
Maximum soldering temperature ≤ 200 °C (tab-temperature).
Soldering cycle duration including pre-heating ≤ 30 sec.

For good soldering and avoiding damage to the encapsulation pre-heating is recommended to a temperature ≤ 165 °C at a duration ≤ 10 s.

INSTRUCTIONS FOR CLIP MOUNTING

Direct mounting with clip 56363

1. Apply heatsink compound to the mounting base, then place the transistor on the heatsink.
2. Push the short end of the clip into the narrow slot in the heatsink with the clip at an angle of 10° to 30° to the vertical (see Figs 1 and 2).
3. Push down the clip over the device until the long end of the clip snaps into the wide slot in the heatsink. The clip should bear on the plastic body, not on the tab (see Fig. 2a).

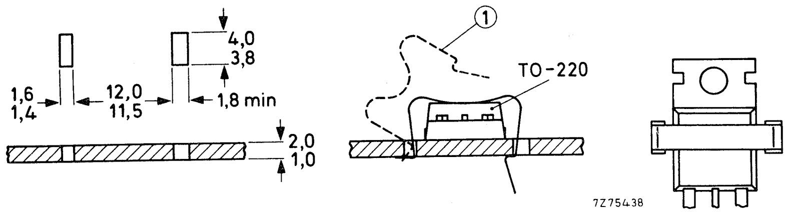


Fig. 1 Heatsink requirements.

Fig. 2 Mounting.
(1) spring clip 56363.

Fig. 2a Position of transistor (top view).

Insulated mounting with clip 56364

With the insulators 56367 or 56369 insulation up to 2 kV is obtained.

1. Apply heatsink compound to the bottom of both transistor and insulator, then place the transistor with the insulator on the heatsink.
2. Push the short end of the clip into the narrow slot in the heatsink with the clip at an angle of 10° to 30° to the vertical (see Figs 3 and 4).
3. Push down the clip over the device until the long end of the clip snaps into the wide slot in the heatsink. The clip should bear on the plastic body, not on the tab. Ensure that the device is centred on the mica insulator to prevent creepage.

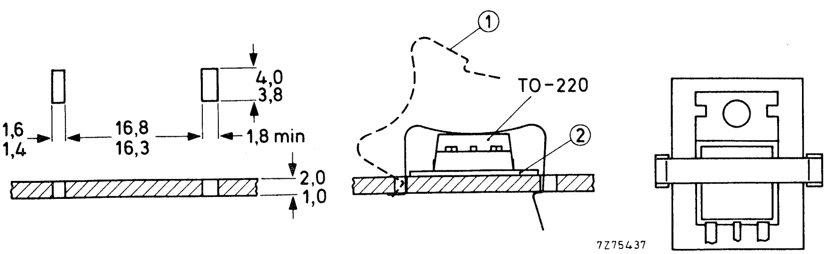


Fig. 3 Heatsink requirements.

Fig. 4 Mounting.
(1) spring clip 56364.
(2) insulator 56369 or 56367.

Fig. 4a Position of transistor (top view).

INSTRUCTIONS FOR SCREW MOUNTING

Dimensions in mm

Direct mounting with screw and spacing washer

- *through heatsink with nut*

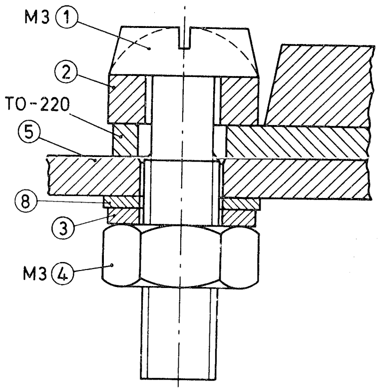


Fig. 5 Assembly.

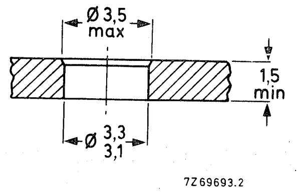


Fig. 6 Heatsink requirements.

(1) M3 screw.
(2) rectangular washer (56360a).
(3) lock washer.
(4) M3 nut.
(5) heatsink.
(8) plain washer.

- *into tapped heatsink*

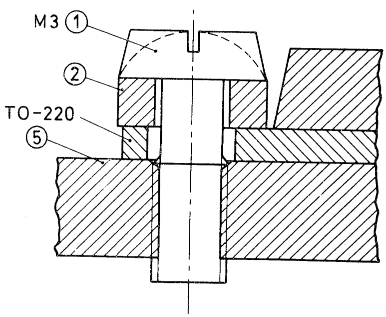


Fig. 7 Assembly.

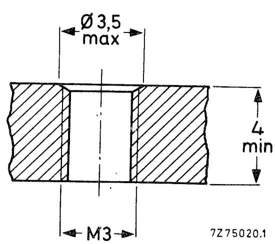


Fig. 8 Heatsink requirements.

(1) M3 screw.
(2) rectangular washer 56360a.
(5) heatsink.

Insulated mounting with screw and spacing washer
(not recommended where mounting tab is on mains voltage)

Dimensions in mm

- *through heatsink with nut*

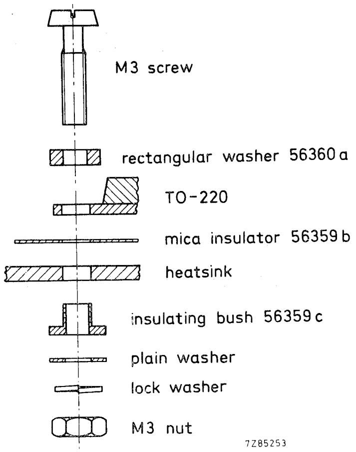


Fig. 9 Insulated screw mounting with rectangular washer. Known as a "bottom mounting".

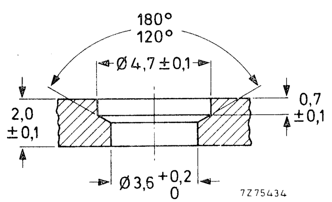


Fig. 10 Heatsink requirements for 500 V insulation.

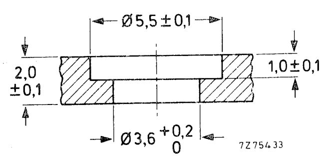


Fig. 11 Heatsink requirements for 800 V insulation.

- *into tapped heatsink*

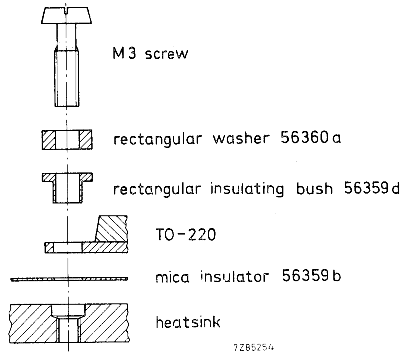


Fig. 12 Insulated screw mounting with rectangular washer into tapped heatsink. Known as a "top mounting".

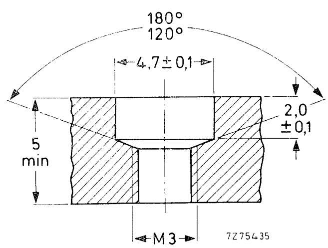


Fig. 13 Heatsink requirements for 500 V insulation.

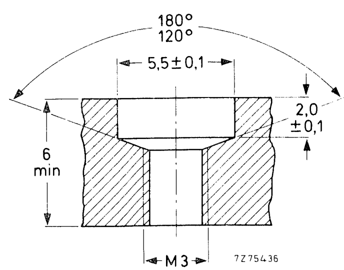


Fig. 14 Heatsink requirements for 1000 V insulation.

MOUNTING INSTRUCTIONS FOR SOT-93 ENVELOPES

GENERAL DATA AND INSTRUCTIONS

General rule

Avoid any sudden forces on leads and body; these forces, such as from falling on a hard surface, are easily underestimated. In the direct screw mounting an M4 screw must be used; an M3 screw in the insulating mounting.

Heatsink requirements

Flatness in the mounting area: 0,02 mm maximum per 10 mm.
The mounting hole must be deburred.

Heatsink compound

The thermal resistance from mounting base to heatsink ($R_{th\ mb\text{-}h}$) can be reduced by applying a metallic-oxide heatsink compound between the contact surfaces. For insulated mounting the compound should be applied to the bottom of both device and insulator.

Maximum play

The bush or the washer may only just touch the plastic part of the body, but should not exert any force on that part. Keep mounting tool (e.g. screwdriver) clear of the plastic body.

Mounting torques

For M3 screw (insulated mounting):	
Minimum torque (for good heat transfer)	0,4 Nm (4 kgcm)
Maximum torque (to avoid damaging the device)	0,6 Nm (6 kgcm)
For M4 screw (direct mounting only):	
Minimum torque (for good heat transfer)	0,4 Nm (4 kgcm)
Maximum torque (to avoid damaging the device)	1,0 Nm (10 kgcm)

Note: The M4 screw head should not touch the plastic part of the envelope.

Lead bending

Maximum permissible tensile force on the body for 5 s — 20 N (2 kgf)

No torsion is permitted at the emergence of the leads.

Bending or twisting is not permitted within a lead length of 0,3 mm.

The leads can be bent through 90° maximum, twisted or straightened; to keep forces within the above-mentioned limits, the leads are generally clamped near the body.

N.B.: Data on accessories are given in chapter Accessories.

Soldering

Recommendations for devices with a maximum junction temperature rating $\leqslant$ 175 °C:

a. Dip or wave soldering

Maximum permissible solder temperature is 260 °C at a distance from the body of > 5 mm and for a total contact time with soldering bath or waves of < 7 s.

b. Hand soldering

Maximum permissible temperature is 275 °C at a distance from the body of > 3 mm and for a total contact time with the soldering iron of < 5 s.

The body of the device must not touch anything with a temperature > 200 °C.

it is not permitted to solder the metal tab of the device to a heatsink, otherwise the junction temperature rating will be exceeded.

Avoid any force on body and leads during or after soldering; do not correct the position of the device or of its leads after soldering.

Thermal data

			clip mounting	screw mounting
Thermal resistance from mounting base to heatsink				
direct mounting				
with heatsink compound	$R_{th\ mb-h}$	=	0,3	0,3 K/W
without heatsink compound	$R_{th\ mb-h}$	=	1,5	0,8 K/W
with 0,05 mm mica washer				
with heatsink compound	$R_{th\ mb-h}$	=	0,8	0,8 K/W
without heatsink compound	$R_{th\ mb-h}$	=	3,0	2,2 K/W

INSTRUCTIONS FOR CLIP MOUNTING

Direct mounting with clip 56379

1. Place the device on the heatsink, applying heatsink compound to the mounting base.
2. Push the short end of the clip into the narrow slot in the heatsink with the clip at an angle of 10° to 20° to the vertical (see Fig. 1b).
3. Push down the clip over the device until the long end of the clip snaps into the wide slot in the heatsink. The clip should bear on the plastic body, not on the tab (see Fig. 1(c)).

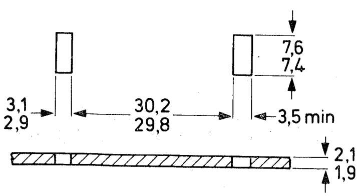


Fig. 1a Heatsink requirements.

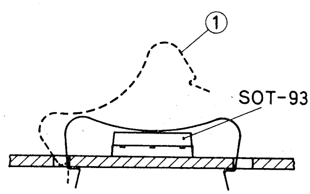


Fig. 1b Mounting.
(1) = spring clip 56379.

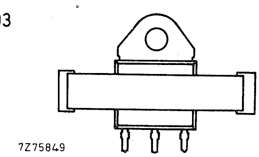


Fig. 1c Position of the device.

Insulated mounting with clip 56379

With the mica 56378 insulation up to 1500 V is obtained.

1. Place the device with the insulator on the heatsink, applying heatsink compound to the bottom of both device and insulator.
2. Push the short end of the clip into the narrow slot in the heatsink with the clip at an angle of 10° to 20° to the vertical (see Figs 2a and 2b).
3. Push down the clip over the device until the long end of the clip snaps into the wide slot in the heatsink. The clip should bear on the plastic body, not on the tab (see Fig. 2c). There should be minimum 3 mm distance between the device and the edge of the insulator for adequate creepage.

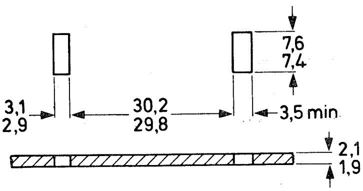


Fig. 2a Heatsink requirements.

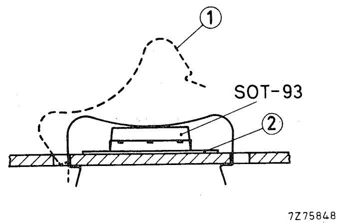


Fig. 2b Mounting.
(1) = spring clip 56379
(2) = insulator 56378

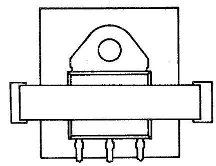


Fig. 2c Position of the device.

INSTRUCTIONS FOR SCREW MOUNTING

Direct mounting

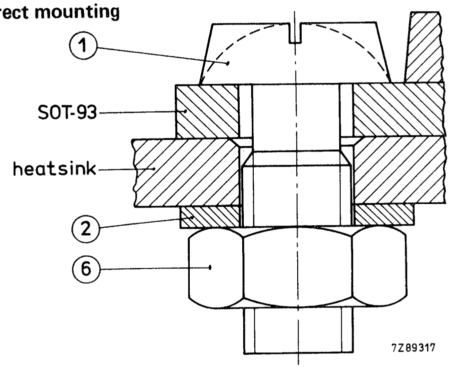


Fig. 3a Assembly through heatsink with nut.

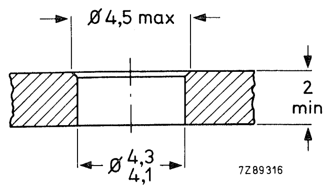


Fig. 3b Heatsink requirements.

When screw mounting the SOT-93 envelope, it is particularly important to apply a thin, even layer of heatsink compound to the mounting base, and to apply torque to the screw slowly so that the compound has time to flow and the mounting base is not deformed. Most SOT-93 envelopes contain a crystal larger than that in the other plastic envelopes, and it is more likely to crack if the mounting base is deformed.

Legend: (1) M4 screw; (2) plain washer; (6) M4 nut.
Where vibrations are to be expected the use of a lock washer or of a curved spring washer is recommended, with a plain washer between aluminium heatsink and spring washer.

Insulated screw mounting with nut; up to 800 V.

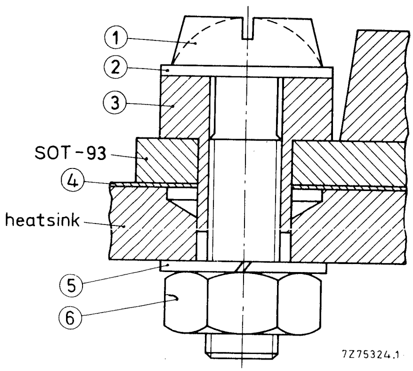


Fig. 4 Assembly.
See also Fig. 9.

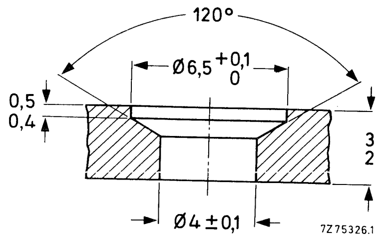


Fig. 5 Heatsink requirements up to 800 V insulation.

(1) M3 screw
(2) plain washer
(3) insulating bush (56368b)
(4) mica insulator (56368a)
(5) lock washer
(6) M3 nut

Insulated screw mounting with tapped hole; up to 800 V.

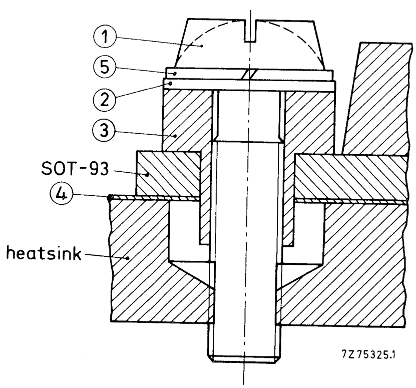


Fig. 6 Assembly.
See also Fig. 9.

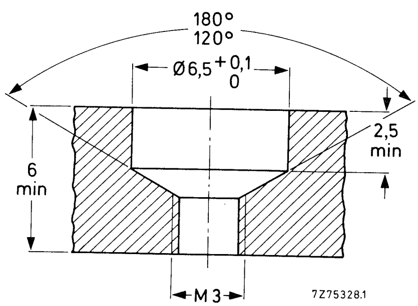


Fig. 7 Heatsink requirements up to 800 V insulation.

(1) M3 screw
(2) plain washer
(3) insulating bush (56368b)
(4) mica insulator (56368a)
(5) lock washer

Insulated screw mounting with insert nut; up to 500 V

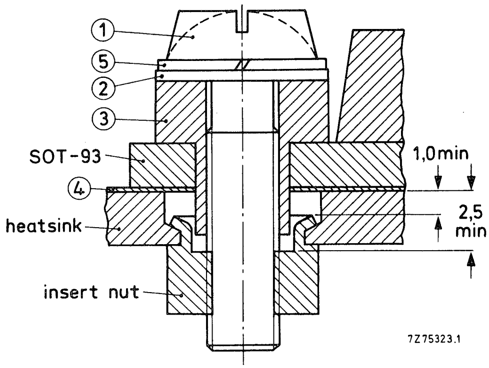


Fig. 8 Assembly and heatsink requirements for 500 V insulation. See also Fig. 3.

(1) M3 screw
(2) plain washer
(3) insulating bush (56368b)
(4) mica insulator (56368a)
(5) lock washer

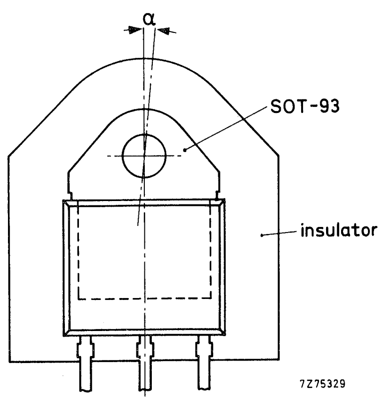


Fig. 9 Mica insulator.

The axial deviation (α) between SOT-93 and mica should not exceed 5^{o}.

MOUNTING INSTRUCTIONS FOR TO-3 ENVELOPES

GENERAL DATA AND INSTRUCTIONS

Instructions for direct mounting.

Mounting instructions for up to 500 V insulation.
Using insulating bushes 56201j or 56261a and mica washer 56201d.

Mounting instructions for 500 to 2000 V insulation.
Using mounting support 56352 and mica washer 56339.

Heatsink requirements

Flatness in the mounting area: 0,05 mm per 40 mm

Mounting holes must be deburred.

Mounting torques

Minimum torque (for good heat transfer)	0,4 Nm (4 kgcm)
Maximum torque (to avoid damaging the transistor)	0,6 Nm (6 kgcm)

N.B.: When the driven nut or screw is in direct contact with a toothed lock washer (e.g. Fig. 10), the torques are as follows:

Minimum torque	0,55 Nm (5,5 kgcm)
Maximum torque	0,8 Nm (8 kgcm)

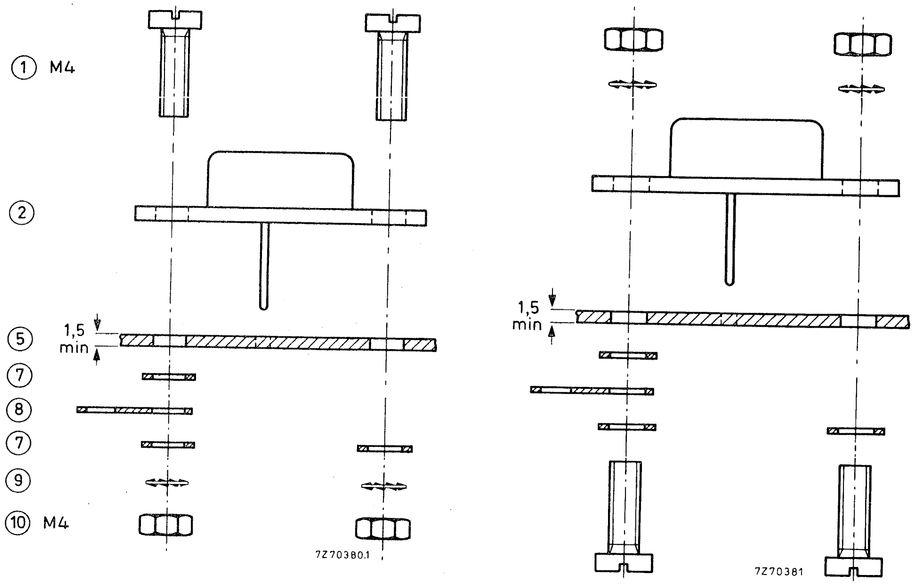
Thermal data

The thermal resistance from mounting base to heatsink ($R_{th\ mb\text{-}h}$) can be reduced by applying a heat conducting compound between transistor and heatsink. For insulated mounting the compound should be applied to the bottom of both device and insulator.

		Direct mounting	Insulated mounting 500 V mica	Insulated mounting 2000 V mica	
From mounting base to heatsink					
without heatsink compound	$R_{th\ mb\text{-}h}$	0,6	1,0	1,25	K/W
with heatsink compound	$R_{th\ mb\text{-}h}$	0,1	0,3	0,5	K/W

INSTRUCTIONS FOR DIRECT MOUNTING

The transistors should be mounted with M4 screws, see Figs 1 and 2. Minimum heatsink thickness (for good heat transfer) 1,5 mm. Hole pattern: Fig. 3.
A heatsink with tapped holes or insert nuts can also be used, but a torque washer is necessary between metal washer and transistor. See Fig. 4.



Figs 1 and 2. Direct mounting with nuts.

Legend
(1) = screw
(2) = TO-3
(4) = mica
(5) = heatsink
(6) = insulating bush
(7) = metal washer
(8) = soldering tag
(9) = lock washer
(10) = nut
(11) = tapped hole
(12) = insert nut
Dimensions in mm

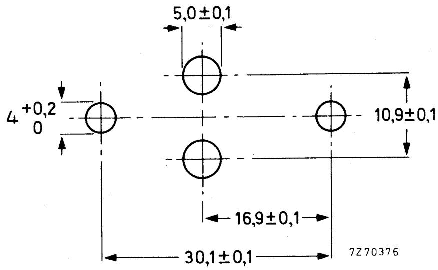


Fig. 3 Hole pattern for direct mounting with nuts.

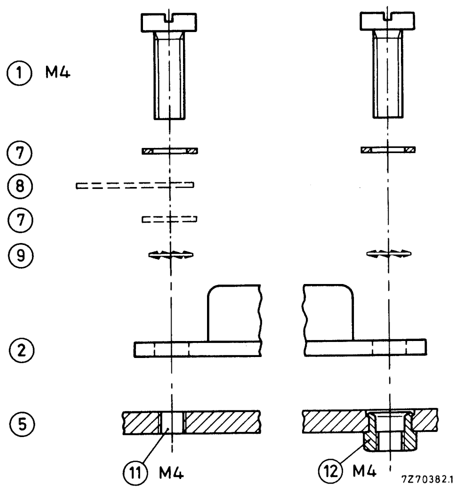


Fig. 4 Direct mounting with tapped holes or insert nuts.

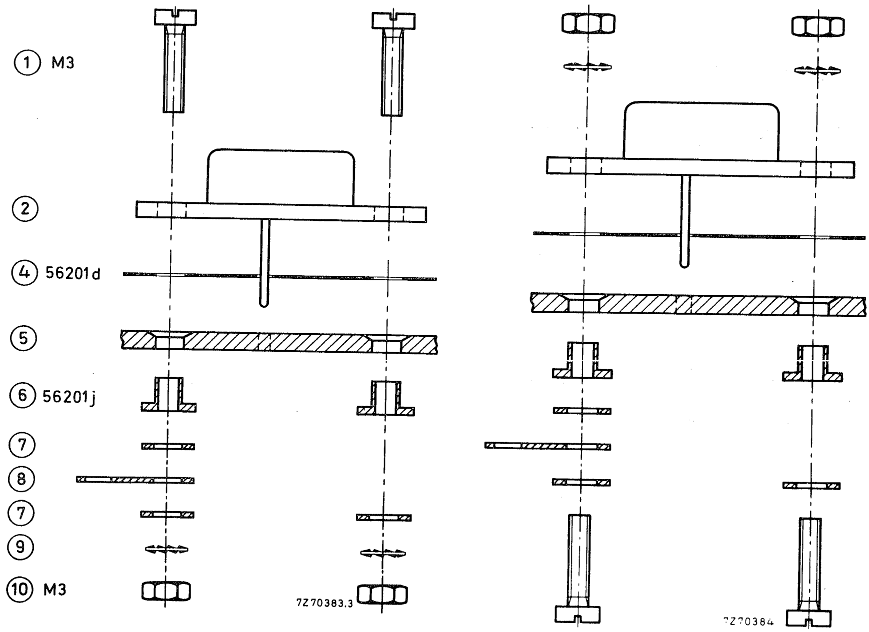
MOUNTING INSTRUCTIONS FOR UP TO 500 V INSULATION

Using insulating bushes 56201j and mica washer 56201d

For the component arrangement with minimum heatsink thickness see Figs 5 and 6. For hole pattern and shape of holes see Figs 7 and 8.

Using insulating bush 56261a and mica washer 56201d

For an arrangement with M3 screws and nuts see Fig. 9, mounting holes are given in Figs 7 and 8. The accessories can also be used in combination with M3 screws and heatsinks provided with tapped holes or insert nuts. Lock washers are necessary between screw-head and metal washer, see Fig. 10. For an assembly drawing with tapped holes see Fig. 11, with insert nuts see Fig. 12.



Figs 5 and 6. Insulated mounting (500 V) with 56201j and 56201d. Heatsink thickness: 1,5 to 2,5 mm.

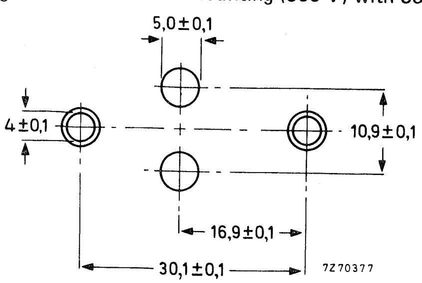


Fig. 7 Hole pattern for 500 V insulation, nut fastening.

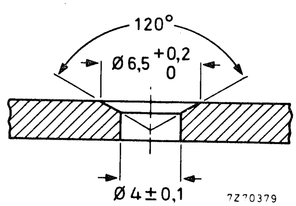


Fig. 8 Shape of hole for 500 V insulation, nut fastening.

For legend see page 378.

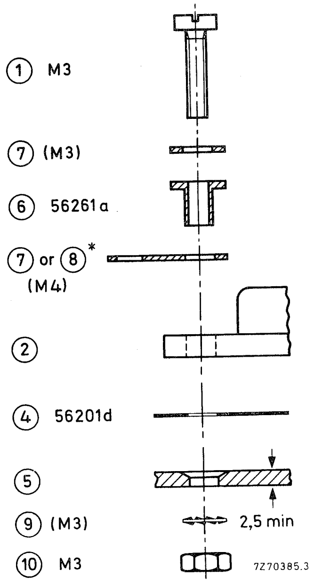


Fig. 9 Insulated mounting (500 V) with nuts.

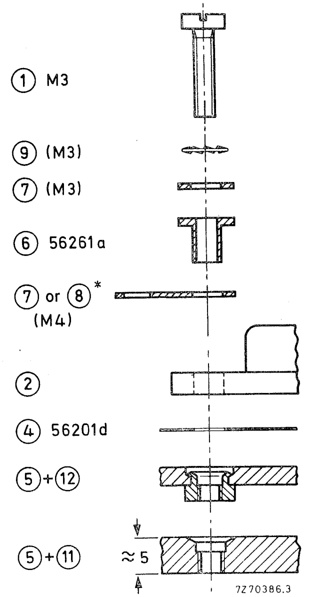


Fig. 10 Insulated mounting (500 V) with tapped holes or insert nuts.

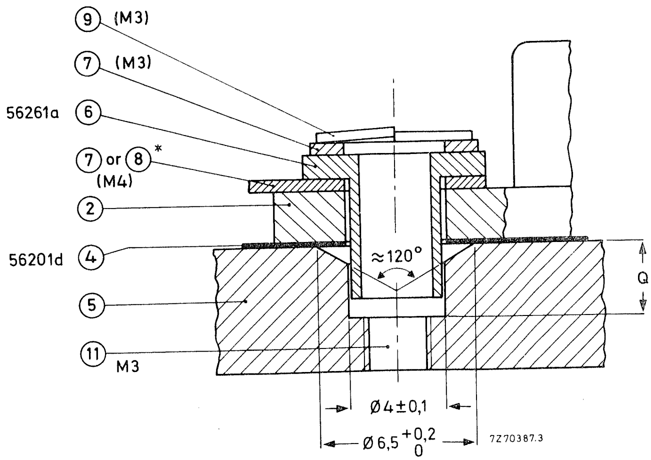


Fig. 11 Assembly (partial) for Fig. 10 - tapped holes.
Q minimum 2,5 mm.

For legend see page 378.

* Thickness approximately 0,6 mm, outer diameter 7,5 mm.

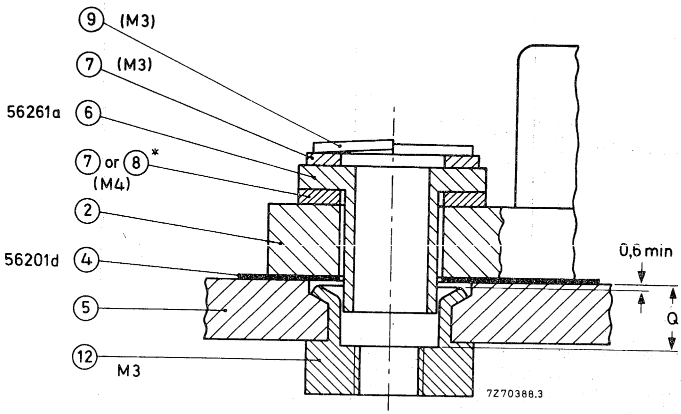


Fig. 12 Assembly (partial) for Fig. 10 - insert nuts Q minimum 2,5 mm.

For legend see page 378.

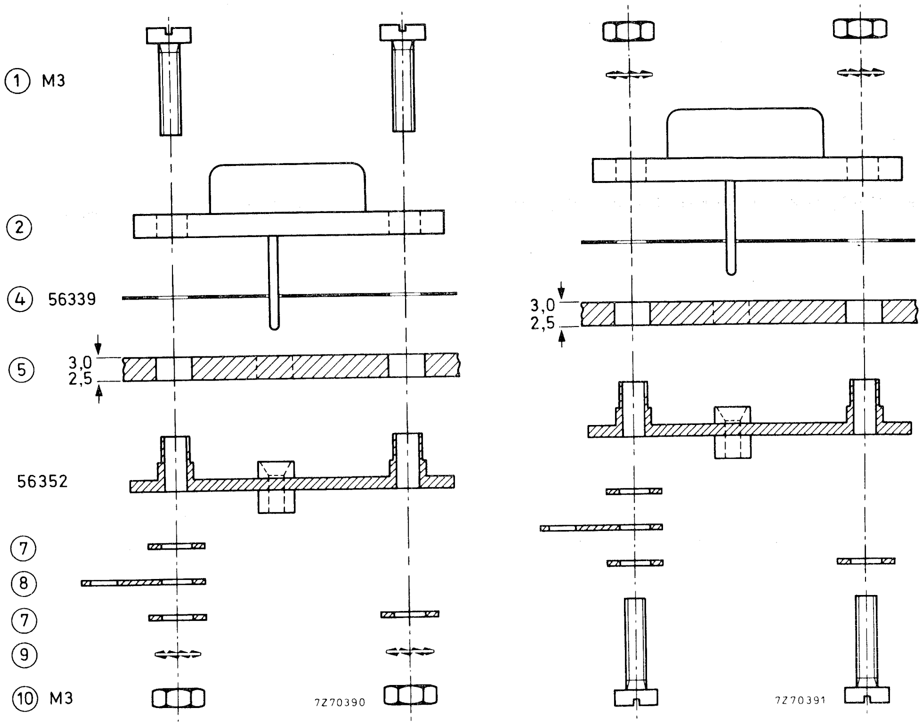
Dimensions in mm

* Thickness approximately 0,6 mm, outer diameter 7,5 mm.

MOUNTING INSTRUCTIONS FOR 500 V TO 2000 V INSULATION

Using mounting support 56352 and mica washer 56339

The transistor should be mounted with M3 screws. For component arrangement see Figs 13 and 14. For hole pattern see Fig. 15. Thickness of heatsink 2,5 mm to 3 mm.



Figs 13 and 14. Insulated mounting (500 V–2000 V).

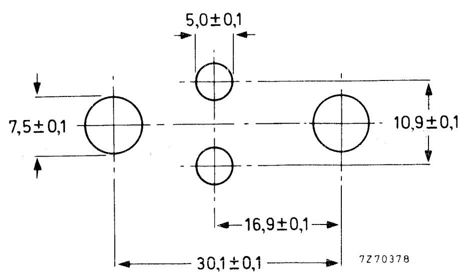


Fig. 15 Hole pattern for Figs 13 and 14.

For legend see page 378.

ACCESSORIES

TYPE NUMBER SURVEY ACCESSORIES

type number	description	envelope
56201d	mica washer (up to 500 V)	TO-3
56201j	insulating bushes (up to 500 V)	TO-3
56261a	insulating bushes (up to 500 V)	TO-3
56326	metal washer	TO-126
56339	mica washer (500 to 2000 V)	TO-3
56352	insulating mounting support	TO-3
56353	spring clip	TO-126/SOT-82
56354	mica insulator	TO-126/SOT-82
56359b	mica washer (up to 1000 V)	TO-220
56359c	insulating bush (up to 800 V)	TO-220
56359d	rectangular insulating bush (up to 1000 V)	TO-220
56360a	rectangular washer (brass)	TO-220
56363	spring clip (direct mounting)	TO-220
56364	spring clip (insulated mounting)	TO-220
56367	alumina insulator (up to 2000 V)	TO-220
56368a	mica insulator (up to 800 V)	SOT-93
56368b	insulating bush (up to 800 V)	SOT-93
56369	mica insulator (up to 2 kV)	TO-220
56378	mica insulator (up to 1500 V)	SOT-93
56379	spring clip	SOT-93
56387a	mica insulator (up to 300 V)	TO-126
56387b	insulating bush (up to 300 V)	TO-126

SELECTION GUIDE

CLIP MOUNTING

envelope	direct mounting		insulated mounting			
	clip		mica	alumina	clip	
TO-126 (SOT-32)	56353		56354		56353	
SOT-82	56353		56354		56353	
TO-220 (SOT-78)	56363		56369 or	56367	56364	
SOT-93	56379		56378		56379	

SCREW MOUNTING

envelope	direct mounting		insulated mounting			
	metal washer	mounting material	mica washer	insul. bush	metal washer	mounting material
TO-126 (SOT-32)	56326	M3				
up to 300 V			56387a	56387b	56326	M2,5
TO-220 (SOT-78)	56360a	M3				
up to 800 V			56359b	56359c	56360a	M3
up to 1000 V			56359b	56359d	56360a	M3
SOT-93	–	M4	56368a	56368b		M3
TO-3 (SOT-3)	–	M4				
up to 500 V			56201d	56201j or 56261a		M3
up to 2000 V			56339	56352		M3

The accessories mentioned can be supplied on request.

See also chapter Mounting Instructions.

Mounting TO-126 and SOT-82 envelopes.

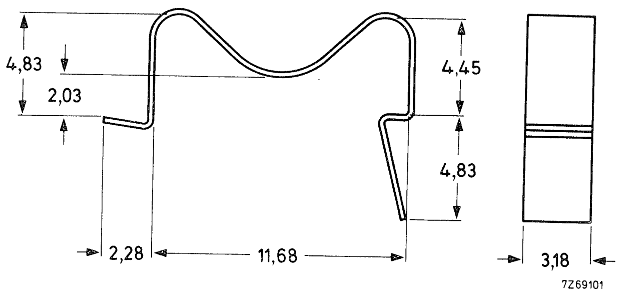
56353 CLIP

for TO-126 and SOT-82 envelopes

MECHANICAL DATA

Material: high carbon spring steel

Dimensions in mm



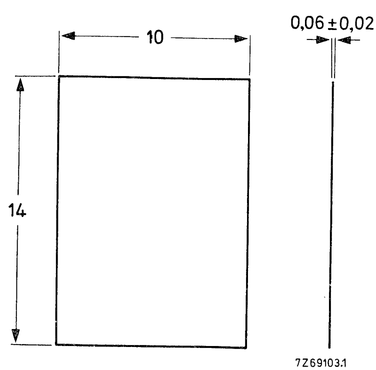
Spring clip suitable for heatsink of 1,5 to 2 mm.

56354 MICA INSULATOR

for TO-126 and SOT-82 envelopes

MECHANICAL DATA

Dimensions in mm



Mounting of TO-126 envelopes

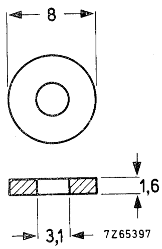
56326 WASHER

for direct mounting of TO-126 envelopes

Dimensions in mm

MECHANICAL DATA

Material: brass, nickel plated

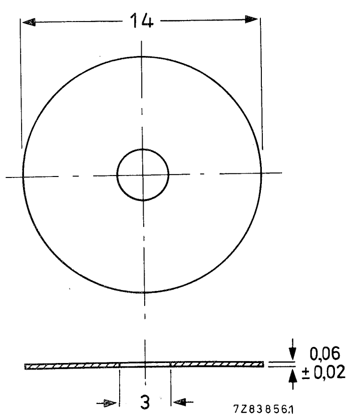


56387a MICA WASHER

for insulated screw mounting of TO-126 envelopes (up to 300 V)

MECHANICAL DATA

Dimensions in mm



Mounting of TO-126 envelopes

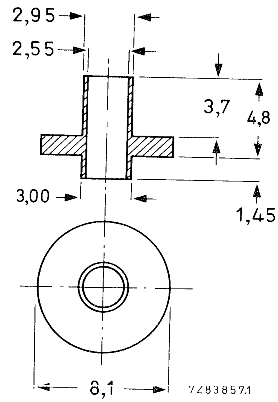
56387b INSULATING BUSH

for insulated screw mounting of TO-126 envelopes (up to 300 V)

MECHANICAL DATA

Dimensions in mm

Material: polyester



TEMPERATURE

Maximum permissible temperature T_{max} 150 °C

Clip mounting TO-220 envelopes

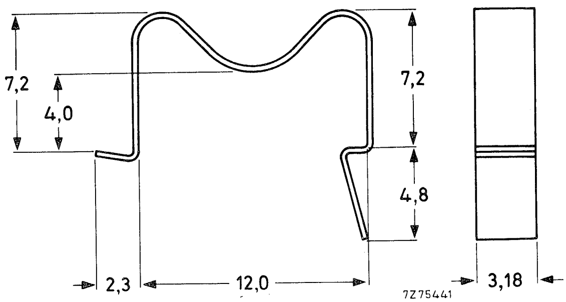
56363 SPRING CLIP

for direct mounting of TO-220 envelopes

MECHANICAL DATA

Dimensions in mm

Material: steel, zinc-chromate passivated.



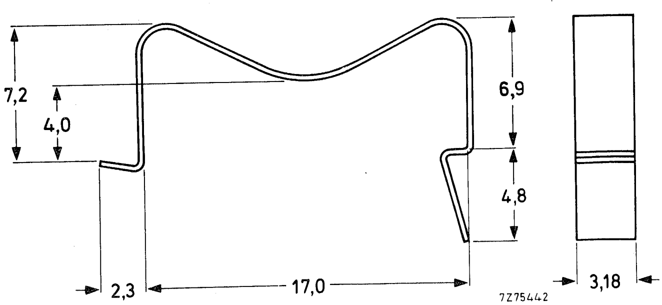
56364 SPRING CLIP

for insulated mounting of TO-220 envelopes

MECHANICAL DATA

Dimensions in mm

Material: steel, zinc-chromate passivated.



to be used in conjunction with **56367** or **56369.**

Clip mounting TO-220 envelopes

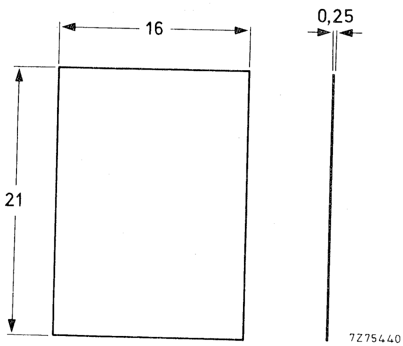
56367 ALUMINA INSULATOR

for insulated clip mounting of TO-220 envelopes (up to 2 kV)

MECHANICAL DATA

Material: 96-alumina.

Dimensions in mm



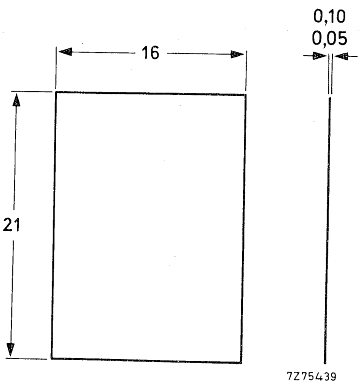
* Because alumina is brittle, extreme care must be taken when mounting devices not to crack the alumina, particularly when used without heatsink compound.

56369 MICA INSULATOR

for insulated clip mounting of TO-220 envelopes (up to 2 kV)

MECHANICAL DATA

Dimensions in mm



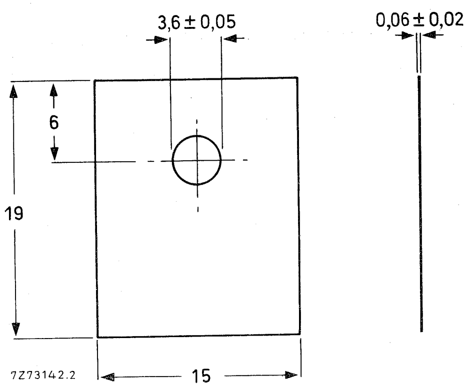
Mounting TO-220 envelopes

56359b MICA WASHER

for TO-220 envelopes (up to 1000 V)

MECHANICAL DATA

Dimensions in mm



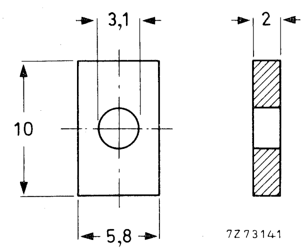
56360a RECTANGULAR WASHER

for direct and insulated mounting of TO-220 envelopes

MECHANICAL DATA

Material: brass; nickel plated

Dimensions in mm



Mounting TO-220 envelopes

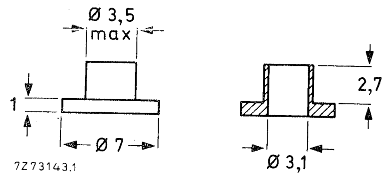
56359c INSULATING BUSH

for TO-220 envelopes (up to 800 V)

MECHANICAL DATA

Material: polyester

Dimensions in mm



TEMPERATURE

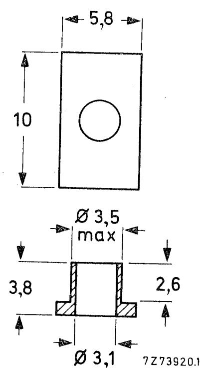
Maximum permissible temperature T_{max} = 150 °C

56359d RECTANGULAR INSULATING BUSH

for TO-220 envelopes (up to 1000 V)

MECHANICAL DATA

Dimensions in mm



TEMPERATURE

Maximum permissible temperature T_{max} = 150 °C

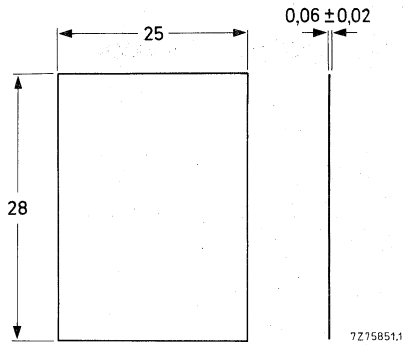
Clip mounting of SOT-93 envelopes

56378 MICA INSULATOR

for SOT-93 clip mounting (up to 1500 V)

MECHANICAL DATA

Dimensions in mm



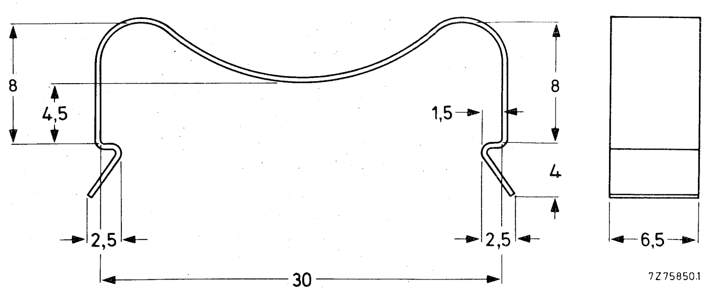
56379 SPRING CLIP

for direct and insulated mounting of SOT-93 envelopes

MECHANICAL DATA

Dimensions in mm

Material:
CrNi steel NLN-939;
thickness 0,4 ± 0,04.



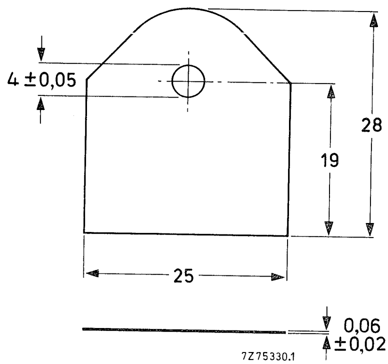
Screw mounting of SOT-93 envelopes

56368a MICA INSULATOR

for insulated screw mounting of SOT-93 envelopes (up to 800 V)

MECHANICAL DATA

Dimensions in mm



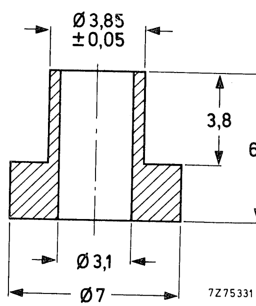
56368b INSULATING BUSH

for insulated screw mounting of SOT-93 envelopes (up to 800 V)

MECHANICAL DATA

Dimensions in mm

Material: polyester



TEMPERATURE

Maximum permissible temperature T_{max} = 150 °C

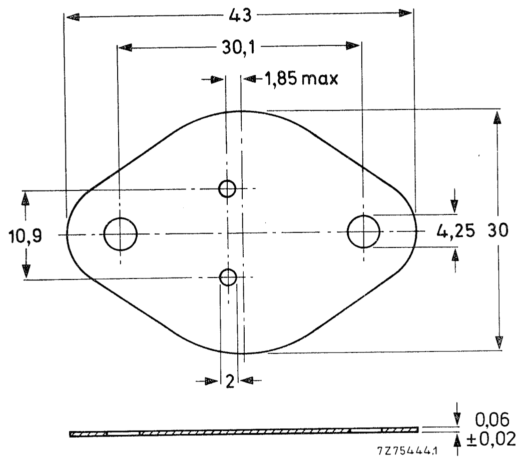
Mounting TO-3 envelopes

56201d MICA WASHER

Mica washer for up to 500 V insulation of **TO-3** envelopes.

MECHANICAL DATA

Dimensions in mm



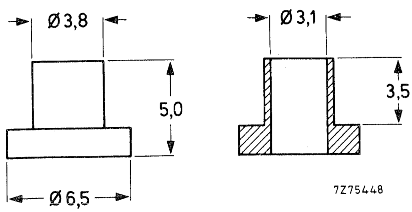
56201j 2 INSULATING BUSHES

Two insulating bushes for up to 500 V insulation of **TO-3** envelopes.

MECHANICAL DATA

Dimensions in mm

Material: polyester



TEMPERATURE

Maximum permissible temperature T_{max} 150 °C

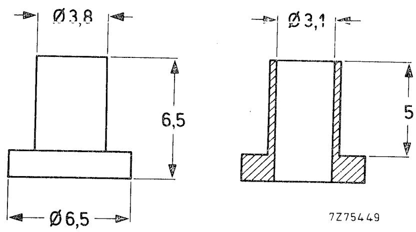
Mounting TO-3 envelopes

56261a 2 INSULATING BUSHES

Two insulating bushes for up to 500 V insulation of TO-3 envelopes.

MECHANICAL DATA
Material: polyester

Dimensions in mm



TEMPERATURE

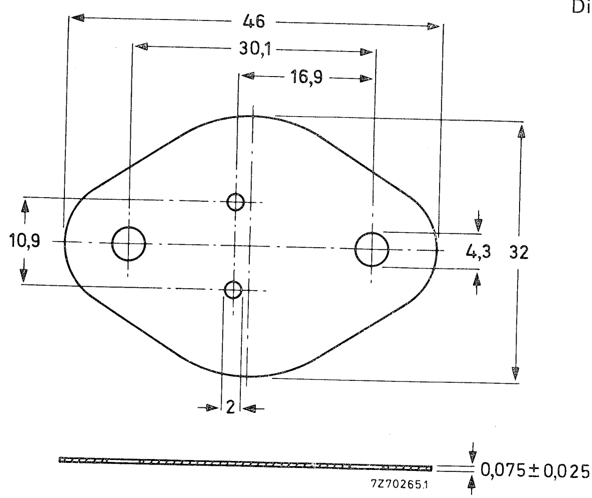
Maximum permissible temperature T_{max} 150 °C

56339 MICA WASHER

Mica washer for 500 to 2000 V insulation of TO-3 envelopes, for which it should be combined with mounting support 56352.

MECHANICAL DATA

Dimensions in mm



Mounting TO-3 envelopes

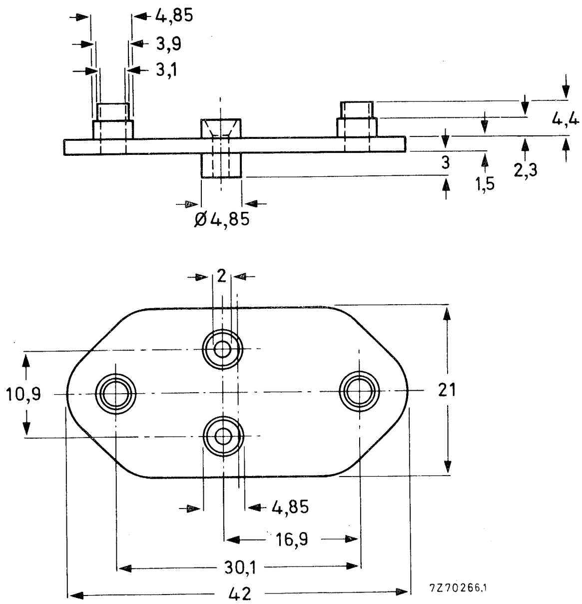
56352 MOUNTING SUPPORT

Mounting support for 500 to 2000 V insulation of TO-3 envelopes, for which it should be combined with mica washer 56339.

MECHANICAL DATA

Dimensions in mm

Material: polyester



TEMPERATURE

Maximum permissible temperature T_{max} 125 °C

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